

electrically conductive material. Conductive layer 164 is formed as a laminated sheet or a tape on carrier 160 and interface layer 162. Conductive layer 164 can include a patterned lead frame, patterned Cu foil, resin coated (RCC) tape with patterned Cu, or prepreg with patterned Cu. Alternatively, conductive layer 164 is formed over carrier 160 and interface layer 162 using PVD, CVD, electrolytic plating, electroless plating process, or other suitable metal deposition process.

In FIG. 3c, semiconductor die 124 from FIG. 2d are mounted to carrier 160 and interface layer 162 using, for example, a pick and place operation with active surface 130 oriented toward carrier 160. Conductive layer 164 is disposed in a peripheral region of semiconductor die 124. Alternatively, conductive layer 164 can be formed after semiconductor die 124 are mounted to carrier 160 and interface layer 162. FIG. 3d shows semiconductor die 124 and conductive layer 164 mounted to carrier 160 as reconstituted or reconfigured wafer 166.

FIG. 3e shows a plan view of semiconductor die 124 and conductive layer 164 mounted to interface layer 162 and carrier 160. Conductive layer 164 includes three portions 164a, 164b, and 164c. Portions 164a-164c are disposed adjacent to three side surfaces of semiconductor die 124. Alternatively, conductive layer 164 may include two portions disposed adjacent to two side surfaces of semiconductor die 124, four portions disposed around four side surfaces of semiconductor die 124, or two portions disposed adjacent to one side surface of semiconductor die 124. Any number and/or configuration of conductive layers 164 may be disposed adjacent to semiconductor die 124 depending on the routing design and function of the semiconductor package.

In FIG. 3f, an encapsulant or molding compound 168 is

and reduces an overall thickness of reconstituted wafer 266. A surface 272 of encapsulant 268 opposite surface 270 is disposed over carrier 260 and interface layer 262 such that surface 272 of encapsulant 268 is substantially coplanar with active surface 130 of semiconductor die 124 and conductive layer 252 of dummy die 250.

In FIG. 7c, carrier 260 and interface layer 262 are removed by chemical etching, mechanical peeling, CMP, mechanical grinding, thermal bake, UV light, laser scanning, or wet stripping. Removing carrier 260 and interface layer 262 exposes surface 272 of encapsulant 268, active surface 130 of semiconductor die 124, and conductive layers 252a-252c of dummy die 250a-250c.

An insulating or passivation layer 280 is formed over surface 272 of encapsulant 268, active surface 130 of semiconductor die 124, and conductive layers 252a-252c of dummy die 250a-250c using PVD, CVD, printing, lamination, spin coating, spray coating, sintering, or thermal oxidation. Insulating layer 280 contains one or more layers of SiO₂, Si₃N₄, SiON, Ta₂O₅, Al₂O₃, or other material having similar insulating and structural properties. A portion of insulating layer 280 is removed by LDA, etching, or other suitable process to expose conductive layer 132 and conductive layers 252a-252c.

An electrically conductive layer or RDL 282 is formed over insulating layer 280 using a patterning and metal deposition process such as sputtering, electrolytic plating, or electroless plating. Conductive layer 282 can be one or more layers of Al, Cu, Sn, Ni, Au, Ag, or other suitable electrically conductive material. One portion of conductive layer 282 is electrically connected to conductive layer 132. Other portions of conductive layer 282 can be electrically common or

semiconductor die 124, is designed to extend over conductive layer 252c such that the power network, insulating layer 280, and conductive layer 252c form the decoupling capacitor. Incorporating a decoupling capacitor into Fo-eWLB 300 reduces voltage fluctuation and increases the electrical performance of Fo-eWLB 300.

Conductive layers 252a-252c are formed over dummy die 250a-250c on a wafer level, i.e., prior to singulation of wafer 240. Conductive layers 252a-252c can be formed and dummy die 250a-250c can be singulated to any shape or size depending on the design and routing requirements of semiconductor die 124 and Fo-eWLB 300. Dummy die 250a-250c are mounted to carrier 260 using a pick and place method. Mounting preformed dummy die 250a-250c with conductive layers 252a-252c to carrier 260 is faster, less expensive, and lower risk than forming additional RDLs, which require complex, highly controlled, expensive, and time-consuming manufacturing steps. Providing an additional conductive layer and ground and power planes by embedding dummy die 250a-250c reduces manufacturing time, increases throughput, and decreases an overall cost of Fo-eWLB 300. Embedded dummy die 250a-250c increase the electrical performance and functionality of Fo-eWLB 300, without increasing package thickness.

FIG. 9 shows a Fo-eWLB 310 including semiconductor die 124 and embedded three-dimensional (3D) interconnection units or interposers 312. Interconnect units 312 include insulating layers 314, 318, and 322, and conductive layers 316, 320, and 324. In one embodiment, interconnect unit 312 contains one or more laminated layers of prepreg, FR-4, FR-1, CEM-1, or CEM-3 with a combination of phenolic cotton paper, epoxy, resin, woven glass, matte glass, polyester, and other reinforcement fibers or

Claims

What is claimed:

1. A semiconductor device, comprising:
 - a semiconductor die;
 - a first ground plane including a first side surface extending laterally along an entire length of a first side surface of the semiconductor die outside a footprint of the semiconductor die;
 - a second ground plane including a first side surface extending laterally along an entire length of a second side surface of the semiconductor die and further extending laterally along a length of the first side surface of the first ground plane; and
 - a conductive layer formed over the semiconductor die and extending to the first ground plane outside the footprint of the semiconductor die.
2. The semiconductor device of claim 1, further including a substrate comprising a plurality of vertical interconnect structures formed through the substrate disposed adjacent to the semiconductor die.
3. The semiconductor device of claim 2, wherein the first ground plane is formed over the substrate.
4. The semiconductor device of claim 1, further including a power plane disposed adjacent to the semiconductor die.

5. The semiconductor device of claim 1, further including a dummy die disposed adjacent to the first side surface of the semiconductor die, wherein the first ground plane is formed over the dummy die.

6. The semiconductor device of claim 1, further including an insulating layer disposed between the first ground plane and the conductive layer, wherein the first ground plane, insulating layer, and conductive layer form a capacitor.