

A LOGIC L.S.I. CIRCUIT

The present invention relates to a logic integrated circuit technique and, more particularly, to a technique which may effectively be applied to the control of the input and output of data to and from a flip-flop in a logic LSI circuit, for example, a technique which may effectively be utilized for a method of divisionally diagnosing logic LSI circuits such as gate arrays.

As a method of diagnosing large-scale integration circuits (LSIs), one in which an LSI is divided into a plurality of combination circuits and each of the combination circuits undergoes a diagnosis is known.

For example, a master-slave flip-flop which consists of series-connected master and slave latches is connected to each of the input and output sides of each of the combination circuits. Test data is written into the flip-flop at the data input side and input to the combination circuit, and the output of the combination circuit is latched by the flip-flop at its output side. This operation is repeated and the latched output is compared with an expected value

which has been obtained in advance to thereby
diagnose the LSI (see "Nikkei Electronics", Nikkei
McGraw-Hill, April 16, 1979, pp. 57 to 63).

5 The above-described master-slave flip-flop for
the divisional diagnosis is arranged such that data
which is latched therein is output to the corresponding
combination circuit through a master latch. Further,
all the master latches in the logic LSI are controlled
by means of in-phase system clock signals so that they
10 can be accessed from external terminals.

After exhaustive study, we have
found that the above-described diagnostic method
involves the following problems. Namely, there is a
15 possibility of causing an undesirable phenomenon,
known as "in-phase transfer", in which data which
is output from a master latch provided at the input
side of a combination circuit and which is supplied
to the combination circuit is changed by means of a
20 clock used to latch data into a master latch provided
at the output side of the combination circuit.
Further, in the above-described diagnostic method,
the normal operation mode and the test mode are set
by alternately switching over two different clocks
25 from one to the other. Therefore, even when data

for testing is desired to be latched into a flip-flop in the test mode for testing a combination circuit, there is a fear of a clock (system clock) for latching data in the normal operation mode being erroneously supplied to the flip-flop, which causes undesirable data to be latched. For this reason, it has previously been necessary to design a logic LSI while taking into consideration the logical restriction that, once the test mode is set, the system clock for latching data in the normal operation mode must be held at the low level at all times.

It is an object of the present invention to reduce the restriction on the logic design and facilitate the diagnosis of a logic integrated circuit.

In its broadest form, a logic L.S.I. circuit includes:

- (a) a first external terminal;
- (b) a second external terminal; and
- (c) combination circuit blocks and a plurality of flip-flops coupled to said combination circuit blocks, said plurality of flip-flops being coupled in series between said first and second external terminals so that test data is serially inputted to the flip-flop coupled to said first external terminal and transferred by being shifted to the subsequent flip-flops, each flip-flop including switching means coupled to receive a control signal and for inhibiting reception of a normal mode clock signal in response to said control signal during a period when said test data is inputted thereto.

Each flip-flop may include a master latch circuit coupled in series with a slave latch circuit. The master latch circuit may be coupled to receive a first clock signal for controlling latching of said test data. The slave latch
5 may be coupled for receiving a second clock signal for controlling latching of said test data output from the master latch circuit.

By virtue of the above-described means, the master latch is provided with the operation control signal input
10 terminal, so that it is possible to set either the normal operation mode or the test mode in accordance with the level of the operation control signal supplied thereto. Once the test mode is set, the normal mode clock signal for latching data in the normal operation mode is invalidated, and there
15 is therefore no fear of any undesirable data being latched into the flip-flop. Accordingly, it is possible to ignore the logical restriction that the normal mode clock signal must be held at the low level at all times during the test mode in order to prevent any undesirable data from being
20 latched into the flip-flop.

The present invention will now be described in greater detail by way of examples with references to the accompanying drawings wherein.

Fig. 1 is a block diagram of one embodiment of the present invention;

5 Fig. 2 is a block diagram of one of the flip-flops shown in Fig. 1;

Fig. 3 is a circuit diagram of the flip-flop shown in Fig. 2;

10 Fig. 4 is a block diagram of another embodiment of the present invention; and

Fig. 5 is a waveform chart showing the operation of the arrangement shown in Fig. 4.

15 Fig. 1 schematically shows the arrangement of a logic LSI such as a gate array to which the present invention may be applied.

Referring to Fig. 1, circuits which are surrounded with the two-dot chain line 10 are fabricated on a single semiconductor chip such as a single crystal silicon substrate, although not
20 necessarily limitative thereto.

The diagnosis of a logic LSI is efficiently carried out by dividing it into a plurality of relatively small-sized combination circuits and
25 diagnosing each combination circuit. In this embodi-

ment, therefore, flip-flops 1, 2 are connected to the data input side of a combination circuit block 7, and flip-flops 3, 4 are connected to the data output side of the block 7.

5 Similarly, the flip-flops 3, 4 are connected to the data input side of a combination circuit block 8, and flip-flops 5, 6 are connected to the data output side of the block 8.

10 The term "combination circuit" is used to refer to any logic circuit the output signal therefrom is primarily determined by the input signal at that time. Examples of such logic circuits include an AND circuit, OR circuit, NOT circuit, NAND circuit, NOR circuit, XOR circuit and circuits obtained by combining these logic
15 circuits (e.g., a half-adder, full adder, sign converter, encoder, decoder, etc.), together with wirings (on which input and output signals are the same).

20 The above-described flip-flops (denoted by the reference numerals 1 to 6) are, for example, arranged as shown in Fig. 2. Referring to Fig. 2, each of the flip-flops illustrated in Fig. 1 is a master-slave flip-flop consisting of a master latch 11 and a slave latch 12.

25 In the master latch 11, when an operation control signal SCAN is at a low level (the normal mode), switches S1, S2 are operated in such a manner that

normal mode data D and a normal mode clock signal CK are validated, respectively. Although not necessarily limitative, in this normal mode, the normal mode data D is supplied and, when the normal mode clock signal CK is raised to a high level, the data is latched by the master latch circuit 11. When a test mode clock signal SCK2 is at a low level, the data latched by the master latch 11 is held therein, whereas, when the test mode clock signal SCK2 is raised to a high level, the latched data is output to the corresponding combination circuit through an output terminal Q₂ of the slave latch 12.

On the other hand, when the operation control signal SCAN is at a high level (the test mode), the switches S1 and S2 are operated in such a manner that test mode data SD and a test mode clock signal SCK1 are validated, respectively. Although not necessarily limitative, in this test mode, when the test mode data SD is supplied and the test mode clock signal SCK1 is raised to a high level, test data used to test the combination circuit is latched by the master latch 11. When, the test mode clock signal SCK2 is at the low level, the data latched by the master latch 11 is held therein, whereas, when the test mode clock signal SCK2 is raised to the high level, the latched test data

is output through the output terminal Q_2 of the slave latch 12 in a manner similar to that in the case of the above-described normal mode. In the test mode, the test mode clock signals SCK1 and SCK2 are alternately raised to the high level, and desired testing data is thereby input to all the master-slave flip-flops each of which is provided at the data input side of the corresponding combination circuit block and which consists of series-connected master and slave latches.

A method of diagnosing a logic LSI will be explained below.

Referring to Fig. 1, first, test data for testing the combination circuit block 7 is set in the flip-flops 1 and 2. More specifically, the operation control signal SCAN supplied to the flip-flops 1 and 2 is raised to the high level, and the switches SW1 to SW6 are thereby controlled so that the test mode data SD is input to each flip-flop. Then, the test mode clock signals SCK1 and SCK2 are alternately raised to the high level, and the test data SD for testing the combination circuit blocks 7 and 8 are thus successively set in the flip-flops 1, 2, 3 and 4. The test pattern set in each of the flip-flops 1, 2, 3 and 4 is supplied to the combination circuit block 7

or 8 through the associated slave latch.

Then, the operation control signal SCAN is shifted to the low level to control the switches SW1 to SW6 so that the normal mode data D is input
5 to each flip-flop. Thereafter, the test mode clock signals SCK1 and SCK2 are shifted to the low level, and the operation mode is thus changed to the normal mode. In the normal mode, the normal mode data clock signal CK (not shown) supplied to the flip-flops 3 and 4
10 is raised to the high level, and data which is delivered from the combination circuit blocks 7 and 8 is thereby latched by the flip-flops 3, 4 and 5, 6, respectively.

Then, the operation control signal SCAN shifted
15 to the low level is raised to the high level again and the test mode clock signals SCK1 and SCK2 are alternately raised to the high level, and the data latched by the flip-flops 3, 4 and 5, 6 is thus read out. In this way, diagnosis of the combination
20 circuit blocks 7 and 8 is effected. It should be noted that it is also possible to diagnose the combination circuit blocks 7 and 8 separately from each other.

In the above-described embodiment, a logic LSI
25 is divided into a plurality of combination circuits,

and a master-slave flip-flop which consists of series-connected master and slave latches is connected to each of the data input and output sides of each combination block.

5 Further, the master latch which constitutes each of the master-slave flip-flops is provided with an operation control signal (SCAN) input terminal for setting either the normal operation mode or the test mode for testing the combination circuit in accordance with the level of the signal supplied thereto.

10 Accordingly, once the test mode is set, the normal mode clock signal is invalidated, and there is therefore no fear of any undesirable data being input to the flip-flops. Thus, it is advantageously possible to eliminate the restriction on the logic design that it is necessary to hold the normal mode clock signal at the low level at all times during the test mode in order to prevent any undesirable data from being input to the flip-flops.

15 20 Further, the above-described embodiment is so arranged that data which is output from each flip-flop to the corresponding combination circuit is delivered from the slave latch which constitutes the flip-flop, and the latches which are respectively provided at the data input and output sides of one combination circuit

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are controlled by means of clocks having different timings. Accordingly, there is no fear of in-phase transfer occurring during a diagnosis, advantageously.

5 Although the invention accomplished by the present inventors has practically been described by way of one embodiment, the present invention is not necessarily limitative to the above-described embodiment and various changes and modifications may, of course, be imparted thereto without departing from the gist of the
10 invention.

For example, although in the described embodiment a logic LSI is divided into two combination circuit blocks and a diagnosis is carried out for each of the blocks, a logic LSI may be divided into any
15 appropriate number of combination circuits according to the size of the LSI.

Fig. 3 shows a practical example of the arrangement of the switch means S1, S2 and master-slave flip-flop shown in Fig. 2.

20 The master latch ML comprises an inverter N1 supplied with the normal mode data D, an inverter N6 supplied with the test mode data SD, an AND gate A1 supplied with the operation control signal SCAN and the normal mode clock signal CK, inverters N2 and N3
25 series-connected so as to constitute a latch, P-channel

type MOSFETs Q1, Q3, Q5, Q7, N-channel type MOSFETs Q2, Q4, Q6, Q8, etc. MOSFET pairs (Q3, Q4) and (Q7, Q8) whose sources and drains are mutually connected are series-connected between the input side of the inverter N2 and the output side of the inverter N3. The output signal from the inverter N1 is supplied to the inverter N2 through a MOSFET pair (Q1, Q2), while the output signal from the inverter N6 is supplied to the inverter N2 through a MOSFET pair (Q5, Q6) and through the MOSFET pair (Q3, Q4). The switching operations of the MOSFET pairs (Q1, Q2) and (Q3, Q4) are controlled by means of the AND gate A1 and an inverter N4 which inverts the output signal from the AND gate A1. The switching operations of the MOSFET pairs (Q5, Q6) and (Q7, Q8) are controlled by means of the test mode clock signal SCK1 and the output signal from an inverter N5 which inverts the signal SCK1.

The slave latch SL comprises inverters N8 and N9 which are series-connected so as to constitute a latch, MOSFET pairs (Q11, Q12), (Q9, Q10), etc. The output signal from the inverter N9 is fed back to the input side of the inverter N8 through the MOSFET pair (Q11, Q12). The output signal Q_M from the master latch is supplied to the inverter N8 through the

MOSFET pair (Q9, Q10). The switching operations of the MOSFET pairs (Q9, Q10) and (Q11, Q12) are controlled by means of the test mode clock signal SCK2 and the output signal from an inverter N7 which inverts the signal SCK2.

The function tables of the master latch ML and the slave latch SL are respectively shown in TABLES 1 and 2 below.

TABLE 1

FUNCTION TABLE OF THE MASTER LATCH (ML)

INPUTS						OUTPUT
CK	D	SCAN	SCK1	SD		QM
L	X	H	L	X		QMO
H	H	H	L	X		H
H	L	H	L	X		L
X	X	L	L	X		QMO
X	X	L	H	H		H
X	X	L	H	L		L

NORMAL
MODE

SCAN
MODE

TABLE 2

FUNCTION TABLE OF THE SLAVE LATCH (SL)

INPUT	OUTPUT
SCK2	Q
L	QO
H	QM

In these tables, "H" represents a high level, "L" a low level, and "X" a state wherein the output is not affected by the level ("don't care"). "Q_{MO}" represents the output signal from the master latch in its previous state, while "Q_O" represents the output signal from the slave latch in its previous state.

As will be clear from TABLE 1, in SCAN MODE, the normal mode clock signal CK and the normal mode data D are in the "don't care" state. Accordingly, in TEST MODE such as SCAN MODE, the normal mode clock signal and the like can be invalidated. As a result, it is possible to prevent any undesirable data from being input to the flip-flop in TEST MODE. Further, the test mode data SD can be invalidated in the normal mode. As a result, it is possible to prevent any undesirable data from being input to the flip-flop in the normal mode.

Fig. 4 shows an example of an arrangement in which test mode data is scanned in and out by using a plurality of flip-flops shown in Fig. 3.

A plurality of flip-flops FF1, FF2, ..., FF_n are fabricated on a single semiconductor chip together with combination circuits (not shown).

This semiconductor chip is provided with external terminals including an input terminal T1 for the test

input data SID, an input terminal T2 for a mode select signal M, an input terminal T3 for the clock signal SC1, an input terminal T4 for the slave latch clock signal SCK2, and an output terminal T5 for test output data SOD. A built-in logic circuit LC forms the operation control signal SCAN and the test mode clock signal SCK1 on the basis of the mode select signal M and the clock signal SC1. These signals are supplied to the master latches ML1 to MLn in the flip-flops FF1 to FFn. The slave latch clock signal SCK2 is supplied to the slave latches SL1 to SLn.

Fig. 5 is a waveform chart diagram showing the operation of each of the circuit blocks shown in Fig. 4. The operation control signal SCAN is raised to the high level only when both the mode select signal M and the clock signal SC1 are at the high level ($SCAN = M \cdot SC1$). The test mode clock signal SC1 is raised to the high level only when the mode select signal M is at the low level and the clock signal SC1 is at the high level ($SCK1 = \bar{M} \cdot SC1$).

In the scan-in state, the test input data SID is serially input to the flip-flop FF1 and transferred by being successively shifted to the subsequent flip-flops.

In the normal state, the mode select signal M is

raised to the high level, and reception of any test input data is thereby inhibited. Further, in the normal state, the test input data held in each flip-flop is supplied to the corresponding combination circuit (not shown). The resultant output signal from the combination circuit is supplied to the associated flip-flop as normal mode data D and latched by the flip-flop in synchronism with the normal mode clock signal CK.

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In the scan-out state, the output signals from the combination circuits which are held in the associated flip-flops are successively shifted to the subsequent flip-flops and thereby transferred. As a result, test output data SOD is serially delivered from the final flip-flop.

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Although the above described examples refer specifically to a logic LSI such as a gate array it should be noted here that the present invention is not necessarily limited thereto and may generally be applied to logic LSIs.

CLAIMS:

1. A logic L.S.I. circuit including:
 - (a) a first external terminal;
 - (b) a second external terminal; and
 - 5 (c) combination circuit blocks and a plurality of flip-flops coupled to said combination circuit blocks, said plurality of flip-flops being coupled in series between said first and second external terminals so that test data is serially inputted to the flip-flop coupled to
 - 10 said first external terminal and transferred by being shifted to the subsequent flip-flops, each flip-flop including switching means coupled to receive a control signal and for inhibiting reception of a normal mode clock signal in response to said control signal during a period
 - 15 when said test data is inputted thereto.
2. A logic L.S.I. circuit according to claim 1, wherein each flip-flop includes a master latch circuit coupled in series with a slave latch circuit.
3. A logic L.S.I. circuit according to claim 2,
- 20 wherein said master latch circuit is coupled to receive a first clock signal for controlling latching of said test data, said slave latch is coupled for receiving a second clock signal for controlling latching of said test data output from said master latch circuit, and levels of said
- 25 first and second clock signals are alternately raised to



high levels.

4. A logic L.S.I. circuit including:

(a) a first external terminal;

(b) a second external terminal;

5 (c) combination circuit blocks; and

(d) a plurality of latch means coupled to said combination circuit blocks, said plurality of latch means being coupled in series between said first and second external terminals so that in a test mode, test input data
10 are serially inputted to the latch means coupled to said first external terminal and transferred by being shifted to the subsequent latch means and test output data held in said latch means are shifted to the subsequent latch means and transferred and serially delivered from the latch means
15 coupled to said external terminal;

wherein ^{each} said latch means includes an input terminal coupled to receive an output signal provided ^{from} ~~from~~ a predetermined combination circuit block, except the first latch means in the series, a clock signal input terminal
20 supplied with a clock signal for controlling latching of said output signal thereto, and means responsive to a control signal for invalidating said output signal and said clock signal during the test mode.

5. A logic L.S.I. circuit according to claim 4,

25 wherein each of said plurality of latch means includes a master latch and a slave latch.



6. A logic L.S.I. circuit implemented in a single semiconductor chip, said logic circuit including:

- (a) a first external terminal;
- (b) a second external terminal;
- 5 (c) first and second combination circuit blocks;
- (d) a first latch circuit having its normal data input terminal coupled to the output of said first combination circuit block, its test mode data input
10 terminal coupled to said first external terminal and its output terminal coupled to the input of said second combination circuit block; and
- (e) a second latch circuit having its normal data input terminal coupled to output of said second
15 combination circuit block, its test mode data input terminal coupled to said output terminal of said first latch circuit and its output terminal coupled to said second external terminal;
- wherein each of said first and second latch
20 circuits further includes a clock signal input terminal supplied with a clock signal for controlling latching of an output signal provided to its normal data input terminal thereof, and means responsive to a mode control signal for invalidating the clock signal and the output signal when
25 said mode control signal indicates a test mode.

7. A logic L.S.I. circuit according to claim 6,



wherein each of said first and second latch circuits is composed of a master-slave type latch circuit.

8. A logic L.S.I. circuit implemented in a single semiconductor chip said logic circuit including:

- 5 (a) combination circuit blocks;
 - (b) a first external terminal;
 - (c) a second external terminal; and
 - (d) a plurality of latch circuits coupled to said combination circuit blocks, said plurality of latch
 - 10 circuits being coupled in series between said first and second terminals;
- wherein each latch circuit includes:
- (e) a master flip-flop circuit;
 - (f) a slave flip-flop circuit having its input
 - 15 coupled to output of said master flip-flop circuit;
 - (g) an input terminal for receiving output data generated from a predetermined combination circuit block;
 - (h) a normal mode clock signal input terminal for receiving a first clock signal for controlling latching
 - 20 of said output data to said master flip-flop circuit;
 - (i) a test data input terminal for receiving test data;
 - (j) a test mode clock signal input terminal coupled to said master flip-flop circuit for controlling
 - 25 latching of said test data to said master flip-flop circuit;
 - (k) switching means located between said master



flip-flop circuit and said input terminal and said normal mode clock signal input terminal; and

- (1) a mode control signal input terminal for receiving a control signal for controlling the operation of
5 said switching means;

wherein said switching means is in the off state when said control signal indicates a test mode.

9. A logic L.S.I. circuit according to claim 8, wherein said latch circuit further includes another clock
10 input terminal coupled to said slave flip-flop.

10. A logic L.S.I. circuit constructed substantially as herein described with reference to and as illustrated in the accompanying drawings.
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