Abstract of the Disclosure

A structure of a semiconductor device of a CSP structure is provided. In the semiconductor device, the limitation by the bonding tool is small and the bonding pitch of the semiconductor chip can be reduced to 100 μm or less, and the chip shrink technique of a technique for lowering the cost can be employed and in connection with this, compatibility among packages can be kept.

The semiconductor device comprising a semiconductor chip; a TAB tape being used in a manner being directly laminated onto a circuit formed surface of the semiconductor chip or being laminated through a stress moderating elastomer onto the circuit formed surface of the semiconductor chip, the TAB tape having leads made of a metallic film formed on an insulator tape having flexibility; and an externally connecting member formed in an end of the lead of the TAB tape, wherein the TAB tape has holes in the insulator tape, each of the holes corresponding to a bonding pad formed on a circuit formed surface of the semiconductor chip at a position corresponding to a position of the bonding pad; the lead being formed so as to be bridged across over the hole; the lead formed above the hole being joined to the bonding pad of the semiconductor chip.

This Sheet Has Been Replaced



THIS SHEET HAS BEEN REPLACED