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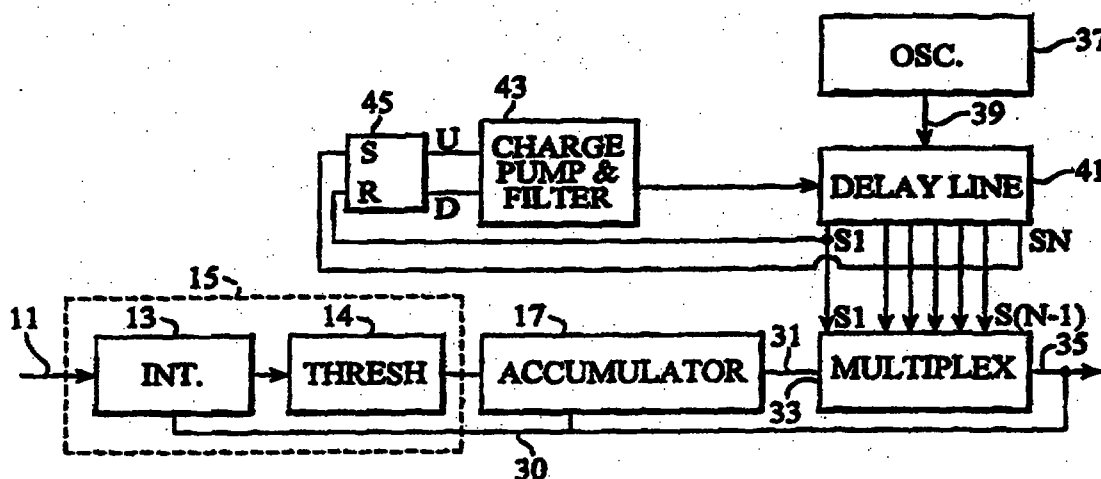


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(54) Title: FREQUENCY SYNTHESIS CIRCUIT TUNED BY DIGITAL WORDS



(57) Abstract

A direct digital frequency synthesizer featuring a modulo accumulator (17; 117) addressing a multiplexer (33; 133). The multiplexer gives a series of delay signals generated from digital circuits (41-45; 141-153). The delay signals establish the phase of a reference oscillator (37; 137). The number of units of delay are sufficient to resolve expected jitter. The accumulator is a digital counter which increments by only a single digit for each count, such as a Gray code counter. In one embodiment, the delay signals are generated by a charge pump (43; Fig. 5) feeding individual logic circuits (41; Figs. 3-4) driving integrated capacitors in a loop. Feedback to the charge pump establishes that the total delay will subdivide a single clock cycle of the reference clock. In a second embodiment, a single shifter (151; 153), with output in phase reversal relation (145), subdivide a single clock cycle. A clock multiplier (141) and (147) are used to assure the synchronism of each clock cycle with the total number of units of delay. The output (33; 155) of the multiplexer (33; 133) is the reference oscillator signal, adjusted by the phase delay, forming a synthesized output frequency.