CLAIMS

I/We claim:

1. A semiconductor device, comprising:

a semiconductor substrate;

first and second metallization layers, the second metallization layer being spaced apart from the semiconductor substrate with the first metallization layer therebetween; and

a conductive interconnect extending at least partially through the semiconductor substrate;

wherein the first metallization layer is in electrical contact with the conductive interconnect via the second metallization layer.

2. The semiconductor device of claim 1 wherein:

the semiconductor substrate includes a first side and a second side;

the second metallization layer includes a first portion generally corresponding to the conductive interconnect and a second portion extending laterally from the first portion; and

the semiconductor device also includes:

an insulation between the first side of the semiconductor substrate and the first metallization layer;

an integrated circuit on or in the semiconductor substrate;

a conductive link at least partially in the insulation, the conductive link being between the integrated circuit and the first metallization layer;

a dielectric between the first and second metallization layers; and

the dielectric includes a conductive via directly between the first metallization layer and the second portion of the second metallization layer;

the conductive interconnect includes a first end and a second end, the first end of the conductive interconnect being in direct contact with the first portion of the second metallization layer; and

a solder ball attached to the second end of the conductive interconnect at the second side of the semiconductor substrate.

3. The semiconductor device of claim 1 wherein:

the semiconductor substrate includes a first side and a second side;

the second metallization layer includes a first portion generally corresponding to the conductive interconnect and a second portion extending laterally from the first portion; and

the semiconductor device also includes:

an insulation between the first side of the semiconductor substrate and the first metallization layer;

an integrated circuit on or in the semiconductor substrate;

a conductive link at least partially in the insulation, the conductive link extending between the integrated circuit and the first metallization layer; and

a dielectric between the first and second metallization layers;

the conductive interconnect includes a first end and a second end opposite the first end;

the dielectric includes a first conductive via and a second conductive via spaced apart from the first conductive via, the first conductive via being directly between the first metallization layer and the second portion of the second metallization layer, the second conductive via being directly between the first portion of the second metallization layer and the first end of the conductive interconnect; and

a solder ball attached to the second end of the conductive interconnect at the second side of the semiconductor substrate.

4. The semiconductor device of claim 1 wherein:

the semiconductor substrate includes a first side and a second side;

the second metallization layer includes a first metallization surface opposite a second metallization surface; and

the semiconductor device also includes:

an insulation between the first side of the semiconductor substrate and the first metallization layer;

an integrated circuit on or in the semiconductor substrate;

a conductive link at least partially in the insulation, the conductive link being between the integrated circuit and the first metallization layer;

a dielectric between the first and second metallization layers; and

the dielectric includes a conductive via directly between the first metallization layer and the second metallization layer;

the conductive interconnect includes:

an aperture extending at least partially between the first and second sides of the semiconductor substrate;

a first section of a conductive material in the aperture;

a second section of the conductive material external to the aperture;

the second section of the conductive material extending laterally on the first section; and

the second section is in direct contact with at least a portion of the second metallization surface of the second metallization layer; and

a solder ball attached to the second end of the conductive interconnect at the second side of the semiconductor substrate.

5. The semiconductor device of claim 1 wherein:

the semiconductor device also includes a dielectric between the first and second metallization layers; and

the conductive interconnect includes a first end and a second end, the first end of the conductive interconnect being generally planar with the second surface of the dielectric, the second end being opposite the first end.

6. The semiconductor device of claim 1 wherein:

the semiconductor device also includes a dielectric between the first and second metallization layers; and

the conductive interconnect includes a first end and a second end, the first end of the conductive interconnect being in direct contact with the second metallization layer, the second end being opposite the first end.

7. The semiconductor device of claim 1 wherein:

the second metallization layer includes a first portion generally corresponding to the conductive interconnect and a second portion extending laterally from the first portion;

the semiconductor device also includes a dielectric between the first and second metallization layers, the dielectric having a first surface in direct contact with the first metallization layer and a second surface in direct contact with the second portion of the second metallization layer; and

the conductive interconnect includes a first end and a second end, the first end of the conductive interconnect being in direct contact with the first portion of the second metallization layer, the second end being opposite the first end.

8. The semiconductor device of claim 1 wherein:

the first metallization layer includes a first metallization surface proximate to the semiconductor substrate and a second metallization surface opposite the first metallization surface; and

the conductive interconnect includes a first end and a second end, the first end of the conductive interconnect being generally flush with the second metallization surface of the first metallization layer, the second end being opposite the first end.

9. The semiconductor device of claim 1 wherein:

the semiconductor device also includes a dielectric between the first and second metallization layers, the dielectric having a first surface in direct contact with the first metallization layer and a second surface opposite the first surface, the second surface being in direct contact with the second metallization layer;

the dielectric includes a first conductive via and a second conductive via spaced apart from the first conductive via;

the first conductive via is directly between the first metallization layer and the second metallization layer; and

the second conductive via is directly between the second metallization layer and the conductive interconnect.

10. The semiconductor device of claim 1 wherein the conductive interconnect includes:

an aperture extending at least partially in the semiconductor substrate;

a first section of a conductive material in the aperture;

a second section of the conductive material external to the aperture; and

the second section of the conductive material extending laterally from the aperture and is in direct contact with the second metallization layer.

11. A semiconductor device, comprising:

a semiconductor substrate;

a plurality of metal routing layers carried by the semiconductor substrate, the plurality of metal routing layers including 1, 2, ..., N (N is a positive integer greater than 3) metal routing layers; and

a conductive interconnect extending at least partially through the semiconductor substrate, the conductive interconnect including an end proximate to the metal routing layers;

wherein the end of the conductive interconnect extends beyond or is generally flush with at least the first metal routing layer.

12. The semiconductor device of claim 11 wherein the end of the conductive interconnect extends beyond or is generally flush with the N-2 metal routing layer.

13. The semiconductor device of claim 11 wherein:

the end of the conductive interconnect extends beyond or is generally flush with the N-2 metal routing layer; and

the N-1 metal routing layer electrically connects the N-2 metal routing layer to the conductive interconnect.

14. The semiconductor device of claim 11 wherein the end of the conductive interconnect is in direct contact with the N-1 metal routing layer.

15. The semiconductor device of claim 11, further comprising a conductive via between the end of the conductive interconnect and the N-1 metal routing layer.

16. The semiconductor device of claim 11 wherein the end of the conductive interconnect includes a first section and a second section extending laterally from the first section, the second section being in direct contact with the N-1 metal routing layer.

17. A method for fabricating a semiconductor device, comprising:

forming a first metallization layer on a semiconductor substrate;

forming an interconnect aperture at least partially in the semiconductor substrate after the first metallization layer is formed;

filling the interconnect aperture with a conductive material; and

forming a second metallization layer on the first metallization layer, the second metallization layer being in electrical contact with the conductive material in the interconnect aperture.

18. The method of claim 17 wherein:

forming an interconnect aperture includes:

depositing a first dielectric on the first metallization layer;

patterning the first dielectric and forming an opening generally corresponding to the interconnect aperture; and

etching the first dielectric and the semiconductor substrate via the opening;

filling the interconnect aperture includes:

introducing a first conductive material in the interconnect aperture; and

removing excess first conductive material external to the interconnect aperture; and

forming a second metallization layer includes:

depositing a second dielectric on the first dielectric and the conductive material in the interconnect aperture;

patterning the deposited second dielectric based on a desired profile of the second metallization layer; and

forming a via and a depression in the patterned second dielectric, the via exposing at least a portion of the first metallization layer, the depression exposing at least a portion of the first conductive material in the interconnect aperture; and

filling the via and the depression with a second conductive material, the second conductive material having a first portion in direct contact with the first conductive material in the interconnect aperture and a second portion in the via in direct contact with the first metallization layer.

19. The method of claim 17 wherein:

forming an interconnect aperture includes:

patterning the semiconductor substrate with the first metallization layer and forming an opening generally corresponding to the interconnect aperture; and

etching the semiconductor substrate via the opening;

filling the interconnect aperture includes:

introducing a first conductive material in the interconnect aperture; and

removing excess first conductive material external to the interconnect aperture; and

forming a second metallization layer includes:

depositing a first dielectric on the first metallization layer and the first conductive material in the interconnect aperture;

forming a first via and a second via in the first dielectric, the first via exposing at least a portion of the first metallization layer, the second via exposing at least a portion of the first conductive material in the interconnect aperture;

depositing a second dielectric on the first dielectric;

patterning the deposited second dielectric based on a desired profile of the second metallization layer;

forming a depression in the patterned second dielectric, the depression generally corresponding the to desired profile of the second metallization layer; and

filling the first and second vias and the depression with a second conductive material.

20. The method of claim 17 wherein:

forming a second metallization layer includes:

depositing a first dielectric on the first metallization layer;

patterning the first dielectric based on a desired profile of the second metallization layer;

forming a via and a depression in the first dielectric, the depression generally corresponding to the desired profile of the second metallization layer; and

filling the via and the depression with a first conductive material; and

forming an interconnect aperture includes:

depositing a second dielectric on the second metallization layer and the first dielectric;

patterning the second dielectric and forming an opening generally corresponding to the interconnect aperture and at least a portion of the second metallization layer;

etching the first and second dielectrics and the semiconductor substrate via the opening;

depositing an insulation material in the interconnect aperture and on the second metallization layer;

removing at least a portion of the insulation material on the second metallization layer; and

filling the interconnect aperture with a second conductive material via the opening, at least a portion of the second conductive material being in direct contact with the second metallization layer.

21. The method of claim 17 wherein:

the conductive material is a first conductive material; and

forming a second metallization layer includes:

depositing a dielectric on the conductive material in the interconnect aperture;

forming a depression in the dielectric, the depression exposing at least a portion of the conductive material in the interconnect aperture; and

filling the depression with a second conductive material, the second conductive material having a first portion in direct contact with the first conductive

material in the interconnect aperture and a second portion extending laterally from the first portion.

22. The method of claim 17 wherein:

the conductive material is a first conductive material; and

forming a second metallization layer includes:

depositing a dielectric on the first metallization layer and the first conductive material in the interconnect aperture;

forming a first via and a second via in the dielectric, the first via exposing at least a portion of the first metallization layer, the second via exposing at least a portion of the first conductive material in the interconnect aperture; and

filling the first and second vias with a second conductive material.

23. The method of claim 17 wherein:

the conductive material is a first conductive material; and

forming an interconnect aperture includes:

depositing a dielectric on the second metallization layer;

forming the interconnect aperture through the dielectric and the semiconductor substrate;

exposing at least a portion of the second metallization layer; and

depositing a second conductive material in the interconnect aperture and onto the exposed portion of the second conductive material.

24. A method for fabricating a semiconductor device, comprising:

forming a first, second, ..., and N^{th} metallization layers on a semiconductor substrate, N being a positive integer not less than 3;

forming an interconnect aperture at least partially in the semiconductor substrate at least after the first metallization layer is formed; and

filling the interconnect aperture with a conductive material, the conductive material being in electrical contact with at least one of the metallization layers.

25. The method of claim 24 wherein forming an interconnect aperture includes forming the interconnect aperture at least partially in the semiconductor substrate after the N-2 metallization layer is formed.

26. The method of claim 24 wherein:

forming an interconnect aperture includes forming the interconnect aperture at least partially in the semiconductor substrate after the N-2 metallization layer is formed; and

forming a first, second, ..., and N^{th} metallization layers includes forming the N-1 metallization layer after filling the interconnect aperture with the conductive material.

27. The method of claim 24 wherein:

forming an interconnect aperture includes forming the interconnect aperture at least partially in the semiconductor substrate after the N-2 metallization layer is formed;

forming a first, second, ..., and N^{th} metallization layers includes forming the N-1 metallization layer after filling the interconnect aperture with the conductive material; and

the method further includes directly contacting the N-1 metallization layer with the conductive material in the interconnect aperture.

28. The method of claim 24 wherein:

forming an interconnect aperture includes forming the interconnect aperture at least partially in the semiconductor substrate after the N-2 metallization layer is formed;

forming a first, second, ..., and N^{th} metallization layers includes forming the N-1 metallization layer after filling the interconnect aperture with the conductive material; and

the method further includes forming a conductive via directly between the N-1 metallization layer and the conductive material in the interconnect aperture.

29. The method of claim 24 wherein:

forming an interconnect aperture includes forming the interconnect aperture at least partially in the semiconductor substrate after the N-1 metallization layer is formed; and

filling the interconnect aperture includes filling the interconnect aperture with the conductive material with a first portion in direct contact with the N-1 metallization layer and a second portion in the interconnect aperture.

30. The method of claim 24 wherein:

forming an interconnect aperture includes forming the interconnect aperture at least partially in the semiconductor substrate after the N-1 metallization layer is formed;

the method further includes exposing at least a portion of the N-1 metallization layer; and

filling the interconnect aperture includes introducing the interconnect aperture into the interconnect aperture and onto the exposed portion of the N-1 metallization layer.

CLAIMS

I/We claim:

1. A semiconductor device, comprising:

a semiconductor substrate;

first and second metallization layers, the second metallization layer being spaced apart from the semiconductor substrate with the first metallization layer therebetween; and

a conductive interconnect extending at least partially through the semiconductor substrate, wherein the conductive interconnect includes a first end and a second end opposite the first end, wherein the second metallization layer includes a first portion generally corresponding to the conductive interconnect and a second portion extending laterally from the first portion, and wherein the first end of the conductive interconnect is electrically coupled to the first portion of the second metallization layer, wherein the first end of the conductive interconnect includes a lateral portion that extends laterally to the first portion of the second metallization layer ; and

wherein the first metallization layer is in electrical contact with the conductive interconnect via the second metallization layer; and

wherein the semiconductor substrate includes a first side and a second side; and

the semiconductor device also includes:

an insulation between the first side of the semiconductor substrate and the first metallization layer;

an integrated circuit on or in the semiconductor substrate;

a conductive link at least partially in the insulation, the conductive link being between the integrated circuit and the first metallization layer;

a dielectric between the first and second metallization layers; and

the dielectric includes a conductive via directly between the first metallization layer and the second portion of the second metallization layer;

the first end of the conductive interconnect is in direct contact with the first portion of the second metallization layer; and

a solder ball attached to the second end of the conductive interconnect at the second side of the semiconductor substrate.

2. The semiconductor device of claim 1 wherein:

the dielectric having a first surface at least proximate the first metallization layer and a second surface at least proximate the second metallization layer; and

the first end of the conductive interconnect is generally planar with the second surface of the dielectric.

3. A semiconductor device, comprising:

a semiconductor substrate;

first and second metallization layers, the second metallization layer being spaced apart from the semiconductor substrate with the first metallization layer therebetween; and

a conductive interconnect extending at least partially through the semiconductor substrate, wherein the conductive interconnect includes a first end and a second end opposite the first end, wherein the second metallization layer includes a first portion generally corresponding to the conductive interconnect and a second portion extending laterally from the first portion, and wherein the first end of the conductive interconnect is electrically coupled to the first portion of the second metallization layer, wherein the first end of the conductive interconnect includes a lateral portion that extends laterally to the first portion of the second metallization layer; and

wherein the first metallization layer is in electrical contact with the conductive interconnect via the second metallization layer; and wherein:

the semiconductor device also includes a dielectric between the first and second metallization layers, the dielectric having a first surface in direct contact with the first metallization layer and a second surface in direct contact with the second portion of the second metallization layer; and

the first end of the conductive interconnect is in direct contact with the first portion of the second metallization layer.

4. A semiconductor device, comprising:

a semiconductor substrate;

a first metallization layer comprising a dielectric material and a conductive material;

a second metallization layer spaced apart from the semiconductor substrate by at least the first metallization layer; and

a conductive interconnect having a first end portion and a second end portion opposite the first end portion, the first end portion including a lateral portion extending laterally to a first portion of the second metallization layer, the second end portion extending at least partially through the semiconductor substrate, wherein the conductive interconnect is electrically connected to the first metallization layer via the second metallization layer, wherein the first portion of the second metallization layer is generally electrically connected to the first end portion of the conductive interconnect and a second portion of the second metallization layer is extending laterally from the first portion; and wherein:

the semiconductor substrate includes a first side, a second side, and an aperture extending at least partially between the first and second sides;

the second metallization layer includes a first metallization surface opposite a second metallization surface; and

the semiconductor device also includes:

an insulation between the first side of the semiconductor substrate and the first metallization layer;

an integrated circuit on or in the semiconductor substrate;

a conductive link at least partially in the insulation, the conductive link being between the integrated circuit and the first metallization layer;

a dielectric between the first and second metallization layers; and

the dielectric includes a conductive via directly between the first metallization layer and the second metallization layer;

the conductive interconnect includes:

a first section of a conductive material in the aperture;

a second section of the conductive material external to the aperture;

the second section of the conductive material extending laterally on the first section; and

a solder ball attached to the second end of the conductive interconnect at the second side of the semiconductor substrate.

5. A semiconductor device, comprising:

a semiconductor substrate;

a first metallization layer comprising a dielectric material and a conductive material;

a second metallization layer spaced apart from the semiconductor substrate by at least the first metallization layer; and

a conductive interconnect having a first end portion and a second end portion opposite the first end portion, the first end portion including a lateral portion extending laterally to a first portion of the second metallization layer, the second end portion extending at least partially through the semiconductor substrate, wherein the conductive interconnect is electrically connected to the first metallization layer via the second metallization layer, wherein the first portion of the second metallization layer is generally electrically connected to the first end portion of the conductive interconnect and a second portion of the second metallization layer is extending laterally from the first portion; and wherein:

the semiconductor device also includes a dielectric between the first and second metallization layers, the dielectric having a first surface and a second surface opposite the first surface, the second surface being in direct contact with the second metallization layer;

the dielectric includes a first conductive via and a second conductive via spaced apart from the first conductive via;

the first conductive via is directly between the first metallization layer and the second metallization layer; and

the second conductive via is directly between the second metallization layer and the conductive interconnect.

6. The semiconductor device of claim 1 wherein the lateral portion extends over the first portion of the second metallization layer.

7. The semiconductor device of claim 3 wherein the lateral portion extends over the first portion of the second metallization layer.

8. The semiconductor device of claim 4 wherein the lateral portion extends over the first portion of the second metallization layer.