SEMICONDUCTOR SUBSTRATES WITH UNITARY VIAS AND VIA TERMINALS, AND ASSOCIATED SYSTEMS AND METHODS

TECHNICAL FIELD

[0001] The present disclosure is directed generally to semiconductor substrates with unitary vias and via terminals, and associated systems and methods.

BACKGROUND

[0002] Packaged semiconductor dies, including memory chips, microprocessor chips, and imager chips, typically include a semiconductor die mounted to a substrate and encased in a plastic protective covering. The die includes functional features, such as memory cells, processor circuits, imager devices, and interconnecting circuitry. The die also typically includes bond pads electrically coupled to the functional features. The bond pads are electrically connected to pins or other types of terminals that extend outside the protective covering for connecting the die to busses, circuits, and/or other microelectronic assemblies.

[0003] Market pressures continually drive manufacturers to reduce the size of semiconductor die packages and to increase the functional capacity of such packages. One approach for achieving these results is to stack multiple semiconductor dies in a single package. The dies in such a package are typically interconnected by electrically coupling the bond pads of one die in the package with bond pads of other die(s) in the package.

[0004] A variety of approaches have been used to electrically interconnect the dies within a multi-die package. One existing approach is to use solder balls connected directly between the bond pads of neighboring dies. Another approach is to fuse "bumps" on the bond pads of neighboring dies. However, the foregoing processes can suffer from several drawbacks. For example, the foregoing structures typically require a multitude of steps to form the vias, the conductive material in the vias, and the bond pads or other connecting structures that form the connections between stacked dies. Each of the steps takes time and accordingly adds to the cost of manufacturing the packaged device. In addition, in at least some cases, each of the processes can elevate the temperature of the die, which can consume a significant portion of the total

thermal budget allotted to the package for processing. As a result, there remains a need for improved techniques for interconnecting dies within a semiconductor package.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Figure 1 is a partially schematic, side cross-sectional view of a package configured in accordance with an embodiment of the disclosure.

[0006] Figures 2A-2I are partially schematic, side cross-sectional views of semiconductor substrates undergoing processing in accordance with an embodiment of the disclosure.

[0007] Figure 2J is a partially schematic, side cross-sectional view of two semiconductor substrates stacked in accordance with a particular embodiment of the disclosure.

[0008] Figure 2K is a partially schematic, side cross-sectional view of two semiconductor substrates stacked in accordance with another embodiment of the disclosure.

[0009] Figures 3A-3F are partially schematic, side cross-sectional illustrations of representative methods for forming substrate terminals having shapes in accordance with further embodiments of the invention.

[0010] Figure 4 is a partially schematic, side cross-sectional illustration of a process for disposing a protective layer on a semiconductor substrate in accordance with a particular embodiment of the disclosure.

[0011] Figure 5 is a schematic illustration of a system that can include one or more packages configured in accordance with several embodiments of the disclosure.

DETAILED DESCRIPTION

[0012] Several embodiments of the present disclosure are described below with reference to packaged semiconductor devices and assemblies, and methods for forming packaged semiconductor devices and assemblies. Many details of certain embodiments are described below with reference to semiconductor dies. The term "semiconductor die" is used throughout to include a variety of articles of manufacture, including, for example, individual integrated circuit dies, imager dies, sensor dies, and/or dies having other semiconductor features. Several of the processes described below may be used to connect an individual die to another individual die, or to connect an individual die to a wafer or portion of a wafer, or to bond a wafer or portion

of a wafer to another wafer or portion of a wafer. The wafer or wafer portion (e.g., wafer form) can include an unsingulated wafer or wafer portion, or a repopulated carrier wafer. The repopulated carrier wafer can include an adhesive material (e.g., a flexible adhesive) surrounded by a generally rigid frame having a perimeter shape comparable to that of an unsingulated wafer, with singulated elements (e.g., dies) carried by the adhesive. The term "semiconductor substrate" is used throughout to include the foregoing articles of manufacture in any of the foregoing configurations.

[0013] Many specific details of certain embodiments are set forth in Figures 1-5 and the following text to provide a thorough understanding of these embodiments. Several other embodiments can have configurations, components, and/or processes different than those described in this disclosure. A person skilled in the relevant art, therefore, will appreciate that additional embodiments may be practiced without several of the details and/or features of the embodiments shown in Figures 1-5, and/or with additional details and/or features.

[0014] Figure 1 is a partially schematic, side cross-sectional view of a semiconductor assembly 100 that includes a semiconductor package 106 configured in accordance with an embodiment of the disclosure. The package 106 can include a support member 102 that carries multiple semiconductor substrates (e.g., semiconductor dies 101) that are interconnected electrically and mechanically with each other. Accordingly, each of the semiconductor dies 101 can include die terminals 110 that are connected to corresponding die terminals 110 of the neighboring die 101. The support member 102 can include support member terminals 107 that are connected to the die terminals 110 of one or more of the semiconductor dies 101. The support member terminals 107 are connected via lines internal to the support member 102 to package terminals 104. The entire package 106 (or portions of the package 106) can be surrounded by an encapsulant 103 to protect the semiconductor dies 101 and the associated connections between the dies 101, while the package terminals 104 remain exposed for connecting the package 106 to external devices, such as printed circuit boards and/or other circuit elements. The following discussion describes additional features of the terminals 110 used to connect neighboring dies 101 to each other, and associated methods for forming such terminals.

[0015] Figure 2A is a partially schematic, side cross-sectional illustration of a semiconductor substrate 120 (e.g., a wafer, wafer portion, die, or other substrate) that includes a substrate material 121 having a first major surface 123 and an oppositely-facing second major

surface 124. As shown in Figure 2A, multiple vias 140 have been formed so as to extend into the first surface 123 along corresponding via axes V. A bond pad can be added to the semiconductor substrate 120 after the vias 140 are formed (as described later with reference to Figure 2J), or the vias 140 can penetrate through pre-formed bond pads at the first surface 123. Individual vias 140 can be axisymmetric with respect to the corresponding via axis V (e.g., each via 140 can have a circular cross-sectional shape), or the vias 140 can have other cross-sectional shapes that closely surround the via axis V (e.g., a low aspect ratio elliptical shape). The vias 140 can be formed using techniques such as aniosotropic etching techniques. Each via 140 can include one or more sidewall surfaces 141 and an end surface 142. In some embodiments, the sidewall surfaces 141 can be scalloped, e.g., by using as stepwise Bosch etching process. In such cases, the vias 140 can be post-processed (e.g., using SF_6 or another isotropic etchant) to smooth the scallops. However, in particular embodiments, the etching process used to form the vias 140 can be a generally continuous process that produces generally smooth, unscalloped sidewall surfaces 141. The sidewall surfaces 141 can accordingly have a generally smooth, cylindrical shape. Suitable processes for forming the via 140 include a wet etch process, a steady state dry etch process, laser drilling, micro-electrodischarge machining, microbead blasting, and others.

[0016] The vias 140 are used to house conductive structures that are connected to semiconductor features (not shown in Figure 2A) within the substrate material 121, and terminals used to electrically connect the semiconductor substrate 120 to other semiconductor substrates and/or support members. The following Figures describe further details of the formation of these terminals.

[0017] As shown in Figure 2B, a protective layer 122 has been disposed on the semiconductor substrate 120 so as to cover the sidewall surfaces 141 and end surfaces 142 of the vias 140. The protective layer 122 can include a C_4F_8 passivation layer, CVD-deposited oxides or nitrides, or other suitable materials. In Figure 2C, the portions of the protective layer 122 covering the end surfaces 142 of the individual vias 140 have been removed, so as to re-expose the end surfaces 142. The portions of the protective layer 122 over the end surfaces 142 can be selectively removed, e.g., without removing the portions of the protective layer 122 adjacent to the sidewall surfaces 141. For example, an anisotropic removal process can be used to selectively remove this material. A representative removal process includes a spacer etch, or other etch process that selectively removes horizontally-oriented materials.

[0018] In Figure 2D, terminal openings 111 have been formed at the ends of individual vias 140. In general, the terminal openings 111 are formed without affecting the shapes of the vias 140 above, due to the protective function performed by the protective layer 122 that covers the sidewall surfaces 141. The terminal openings 111 can have shapes different than those of the via 140. For example, while the vias 140 may have a generally cylindrical shape, the terminal openings 111 can have a generally spherical shape. The terminal openings 111 can also extend laterally beyond the width of the via 140, for example, by using an isotropic removal process as opposed to an anisotropic removal process. Further representative techniques for forming such structures are included in an article titled "Micromachining of Buried Micro Channels in Silicon" (de Boer, et al., Journal of Micro Electromechanical Systems, Vol. 9, No. 1, March 2000), incorporated herein by reference. After the terminal openings 111 are formed, the portions of the protective layer 122 extending into and between the vias 140 are removed prior to subsequent steps for applying conductive material in both the via 140 and the terminal opening 111, as described below.

[0019] Figure 2E illustrates the semiconductor substrate 120 after additional materials have been disposed thereon. For example, as shown in Figure 2E, a dielectric layer 125 has been disposed on the first surface 123 of the substrate material 121, as well as in the vias 140 and the terminal openings 111. A barrier layer 126 has been disposed on the dielectric layer 125, and an optional seed layer 127 has been disposed on the barrier layer 126. Suitable dielectric materials include TEOS, parylene, nitrides, oxides and/or other suitable materials. Suitable barrier layer materials include tungsten, titanium nitride, tantalum, compounds of the foregoing materials and/or other suitable materials. In some embodiments, the seed layer 127 is used to facilitate the process of filling the vias 140 and the terminal openings 111. In other embodiments, a direct on barrier plating process can be used to achieve the same result.

[0020] Figure 2F illustrates the semiconductor substrate 120 after a conductive material 112 has been disposed in the vias 140 and the terminal openings 111. The conductive material 112 can be disposed in both the vias 140 and the terminal openings 111 using a bottom-up deposition process or other suitable process to form a unitary conductive structure 119 that fills both the vias 140 and the terminal openings 111. This single-step process can be performed without realigning the semiconductor substrate 120 between the operation of forming the conductive material 112 in the via 140 and the operation of forming the conductive material 112

in the terminal opening 111. This operation can also be performed without the need to form a vent hole at the end of the via 140, which further reduces processing time.

[0021] Suitable techniques for introducing the conductive material 112 into the via 140 and terminal opening 111 include but are not limited to pulsed chemical vapor deposition (pCVD), ionic physical vapor deposition (iPVD), atomic layer deposition (ALD), electro-grafting, bottom-up ECD plating, and electroless plating. Suitable conductive materials include copper, aluminum, tungsten, gold and/or alloys of the foregoing constituents. In particular embodiments, the conductive material 112 is selected to be electrolytic copper, which has enhanced purity when compared to electrolessly disposed materials, and when compared to solder. For example, the conductive material can be at least 90% copper and in some cases, 99% copper.

[0022] In still further particular embodiments, the conductive material 112 is solder free, e.g., it includes no solder or no more than a trace amount of solder. It is expected that such a material selection can produce conductive structures with enhanced conductivity and/or structural characteristics.

[0023] In still further embodiments, the conductive material 112 can be preformed (at least in part) before being disposed in the via 140 and the terminal opening 111. For example, the conductive material 112 can include a pre-formed wire that is inserted into the via 140 using a wire-bonding process. In this case, the process described below for removing material from the second surface 124 of the substrate 120 can be performed before rather than after the conductive material 112 is disposed in the via 140.

[0024] When the conductive material 112 has been introduced into the via 140 and the terminal opening 111 using a build-up technique (e.g., plating), the process can next include removing material from the second surface 124 to expose the conductive material 112 in the terminal opening 111. For example, in a particular embodiment, the substrate material 121 can be removed (e.g., in a backgrinding or other removal process) up to the dashed line L shown in Figure 2F.

[0025] Figure 2G illustrates a portion of the substrate 120 shown in Figure 2F, including a single via 140 after the substrate material 121 has been removed from the second surface 124. As shown in Figure 2G, removing the substrate material 121 can expose the conductive material 112 to form a first terminal 110a. The resulting first terminal 110a can have a width W2 that is

greater than a corresponding width W1 of the via 140. Accordingly, the first terminal 110a can include additional exposed surface area for connecting to adjacent structures. A passivation layer 128 can then be disposed on the second surface 124 to protect the second surface 124 after the foregoing backgrinding operation.

[0026] The dimensions of the via 140 and the first terminal 110a can be selected depending upon characteristics of the substrate 120 to form highly conductive, compact electrical paths. For example, for an initially 800μ-thick substrate 120, the via 140 can be selected to have a depth D1 of less than 100μ (e.g., 50μ or 25μ). The remaining substrate material 121 can be background, as described above. The width W1 can be 20μ or less (e.g., 10μ or 5μ).

[0027] In a particular aspect of an embodiment shown in Figure 2G, the first terminal 110a can have an exposed conductive surface 118 that is generally flush with the second surface 124 of the substrate material 121. Accordingly, the resulting conductive structure 119 in the via 140 and the terminal opening 111 extends through the substrate material 121 from the first surface 123 to the second surface 124. In other embodiments, additional substrate material 121 can be removed to as to further expose the surfaces of the first terminal 110a, e.g., to form a "bump." For example, Figure 2H illustrates a second terminal 110b that is formed by removing additional material from the second surface 124 of the substrate 120 in the regions surrounding the second terminal 110b. The substrate material 121 can be removed using a wet etch process, or a plasma dry etch process (e.g., with an SF_6O_2 chemistry). The dielectric material 125 in this region can also be removed. This process can produce electrically conductive, outwardly facing surfaces 113 that face laterally outwardly from the via axis V, and project axially away from the second surface 124 in a tapered fashion. Accordingly, the outwardly facing surfaces 113 can increase the exposed surface area of the second terminal 110b (relative to the cross-sectional area of the second terminal 110b) available for establishing connections with adjacent devices. In other embodiments, the outwardly facing surfaces 113 can project or otherwise extend axially into or against the structures of adjacent devices to establish electrical and physical connections.

[0028] The second terminal 110b can include conductive materials in addition to the conductive material 112 that fills the via 140. For example, the second terminal 110b can include a flash coating 114 that is applied to the exposed surface 118. The flash coating 114 can facilitate electrical connections with adjacent devices. In a particular embodiment, the flash coating can include tin, gold, indium or other suitable electrically conductive materials. In

general, the flash coating 114 can be applied using an electroless processing which does not require the use of a mask.

[0029] Figure 2I illustrates a representative third terminal 110c that also includes conductive materials in addition to the conductive fill material 112. In this particular embodiment, the additional material can include a solder ball 115. The solder ball 115 can contact the downwardly facing exposed surface 118 of the conductive material 112, as well as the outwardly facing surfaces 113. This arrangement can give the terminal 110c increased surface area for connecting to adjacent structures. Because the solder ball 115 extends around the outwardly facing surfaces 113, it can provide both increased physical and electrical continuity with the conductive material 112.

[0030] Figure 2J schematically illustrates a portion of a semiconductor assembly 100 that includes a first die 101a electrically connected to a second die 101b in a stacked arrangement. The dies 101a, 101b can include buried microelectronic elements 130 (e.g., capacitors or transistors) connected to bond pads 132 with lines 131. The bond pads 132 are in turn electrically connected to the conductive structures 119 in the vias 140. The first die 101a can include first terminals 110a generally similar in configuration to those described above with reference to Figure 2G. The second die 101b can include second terminals 110b generally similar in configuration to those described above with reference to Figure 2H. The two dies 101a, 101b can be brought together with the first terminals 110a contacting the second terminals 110b. In one embodiment, the exposed surfaces 118 of individual first terminals 110a can contact the exposed surfaces 118 of corresponding individual second terminals 110b. In another embodiment, one or both of the first and second terminals 110a, 110b can include a flash coating 114 (Figure 2H) that contacts the other terminal. The terminals 110a, 110b can be connected using heat, pressure, and/or other forms of energy (e.g., ultrasonic energy) to fuse corresponding first and second terminals 110a, 110b to each other. For example, the terminals 110a, 110b can be attached without reflowing the terminal constituents (e.g., by applying pressure, or pressure in combination with ultrasonic energy). Suitable representative processes include ultrasonic, thermal-sonic and/or thermal-compression processes. In one embodiment, the second terminals 110b can project axially beyond the corresponding second surface 124 of the second die 101b to engage with the corresponding first terminals 110a of the first die 101a. In some cases, a gap 105 may remain between the dies 101a, 101b in the interstices among the terminals 110a, 110b after the attachment process is complete. The gap 105 can be filled with an underfill material or

other suitable material, e.g., prior to encapsulating the stacked structure. In particular embodiments, the completed assembly can have a configuration generally similar to that shown in Figure 1.

[0031] In Figure 2J, the first and second dies 101a, 101b are stacked so that the exposed surfaces 118 of the first terminals 110a contact the exposed terminals 118 of the second terminals 110b. In other embodiments, the relative orientations of one or both dies 101a, 101b can be inverted. For example, in one embodiment, both dies 101a, 101b can be inverted (compared to the orientation shown in Figure 3J) so that the bond pads 132 of the first die 101a contact corresponding bond pads 132 of the second die 101b, and the exposed surfaces 118 of each die 101a, 101b face outwardly (e.g., upwardly and downwardly in Figure 2J).

[0032] In another example, shown in Figure 2K, the orientation of the second die 101b is inverted relative to the orientation shown in Figure 2J, while the first die 101a retains its orientation. Accordingly, the exposed surfaces 118 of the first die 101a contact the bond pads 132 of the second die 101b. This orientation can be used to stack more than two dies in particular embodiments. In other embodiments, the foregoing orientations described above with reference to Figures 2J-2K can be combined, e.g., when the assembly includes more than two stacked dies. For example, a third die can be stacked on top of the second die 101b shown in Figure 2J, with exposed surfaces of the third die terminals in contact with the bond pads 132 of the second die 101b.

[0033] One feature of at least some of the foregoing embodiments described above with reference to Figures 1-2K is that the conductive path through the via 140 can be formed concurrently with forming the terminal 110 at the end of the via 140. As a result, the overall conductive structure 119 within the via 140 and at the terminal 110 can be generally unitary and homogeneous. In particular, the same conductive material can fill the via 140 and the terminal opening 111, without forming a material boundary within the overall structure 119. This process can accordingly produce an overall conductive structure 119 having an increased continuity when compared with existing structures that have boundaries between vias and corresponding bond pads. As a result, these structures can have increased reliability when compared to existing structures.

[0034] In addition, the via 140 and the terminal 110 can be formed without the need for using a mask/lithography process at the second surface 124, which is typically used to form a

bond pad or bump at the end of a via. Instead, the structure can be formed using less time-consuming and less expensive deposition and selective etch processes. This in turn can reduce the amount of time needed to form the conductive structure 119 and therefore the cost of the die or other product in which the via is formed.

[0035] Another feature of at least some embodiments of the foregoing processes is that the semiconductor substrates 120 need not be realigned between the operation of filling the via 140 and the operation of forming the terminal 110. Instead, as discussed above, both structures can be formed as part of the same operation. Still further, as discussed above, the via 140 can be formed using processes that produce non-scalloped, generally uniform, flat, cylindrical walls. For example, a continuous, anisotropic etch process can be used to produce the via 140. As a result, the via 140 can be less time consuming to form than vias that use alternating etch processes, and can use the limited volume available in the substrate 120 more efficiently than processes that produce contoured and/or non-uniform walls.

[0036] Figures 3A-3F illustrate representative processes for forming conductive terminals having shapes in accordance with further embodiments of the disclosure. Referring first to Figure 3A, a via 140 is formed in a substrate 120 using processes generally similar to those described above. A terminal opening 311 can then be formed at the bottom of the via 140, using processes that may form shapes other than the generally spherical shape described above. For example, an anisotropic etch process can be used to remove substrate material 121 in a manner that is aligned with crystal planes of the substrate material 121, producing a terminal opening 311 having generally flat sidewalls. Representative processes for forming such openings are discussed in de Boer et al. (March 2000), previously incorporated by reference.

[0037] In Figure 3B, a dielectric layer 125, a barrier layer 126, and an optional seed layer 127 have been disposed in the via 140 and the terminal opening 311. The via 140 and the terminal opening 311 have then been filled with a conductive material 112 using any of the foregoing processes described above with reference to Figure 2F. Material from the second surface 124 of the substrate 120 is then removed to form a first terminal 310a having an exposed surface 318.

[0038] Figure 3C illustrates a second terminal 310b formed by removing additional substrate material 121 in a manner generally similar to that described above with reference to Figure 2H. Accordingly, the second terminal 310b can include outwardly facing surfaces 313

that project beyond the second surface 124. The second terminal 310b can include an additional conductive material, for example, a flash coating (as discussed above with reference to Figure 2H) or a solder ball (as discussed above with reference to Figure 2I).

[0039] Figure 3D illustrates a third terminal 310c configured in accordance with another embodiment of the disclosure. In this embodiment, the backgrinding process has been halted prior to removing any of the conductive material 112 within the terminal opening 311. The substrate material 121 has been selectively removed from around the conductive material 112 in the terminal opening 311 to form the illustrated structure. For example, the substrate 120 can be exposed to an etchant that preferentially removes the substrate material 121 (and possibly the dielectric material 125 and the barrier layer 126) while not removing the conductive material 112 and optionally the seed layer 127. This arrangement can produce a third terminal 310c that projects beyond the second surface 124 by and additional amount and provides an additional volume of conductive material 112 at the third terminal 310c for connecting the substrate 120 to adjacent structures.

[0040] Figures 3E and 3F illustrate another process for forming a terminal in accordance with another embodiment of the disclosure. As shown in Figure 3E, in some cases, the conductive material 112 applied to the surfaces of the terminal opening 311 and the via 140 may leave a void 316, e.g., in the terminal opening 311. While voids are generally undesirable in most semiconductor processing operations, the void 316 shown in Figure 3E may be readily accommodated and/or accounted for. For example, as shown in Figure 3F, when the substrate material 121 is removed from the second surface 124 to uncover the exposed surface 318, the void 316 is also exposed. Optionally, the void 316 can then be filled with a second conductive material 317. For example, the void 316 can be filled or partially filled with a flash coating, and the shape and additional surface area of the void 316 can facilitate a strong physical and electrical connection with the coating. In another embodiment, the void 316 can be left intact and can be used to receive conductive material from a corresponding terminal structure of a neighboring (e.g., stacked) substrate. For example, the void 316 can receive and connect with a solder ball or other terminal (e.g., the second terminal 110b or the third terminal 110c shown in Figures 2H, 2I respectively) from a neighboring substrate.

[0041] Figure 4 illustrates another embodiment for forming the vias 140 in the substrate 120. In this embodiment, a protective layer 422 is applied to the first surface 123 of the substrate 120, and to the sidewall surfaces 141 of the vias 140. In some cases, the via 140 may

have a high aspect ratio (e.g., a relatively long length and/or relatively small width), which can cause the protective layer 422 to more readily attach to the sidewall surfaces 141 than to the end surface 142. As a result, the end surface 142 may receive little or no protective material 422. This arrangement can eliminate the need to remove the protective layer 422 from the end surface 142 and instead, a terminal opening can be formed directly after applying the protective layer 422. As a result, embodiments of this process are expected to reduce the amount of time required to form the conductive terminals, and can thereby reduce the cost of forming the dies or other end products from the substrate 120.

[0042] Any of the semiconductor packages resulting from joining the substrates in accordance with the methods described above with reference to Figures 1-4 can be incorporated into a myriad of larger and/or more complex systems, a representative example of which is a system 500 shown schematically in Figure 5. The system 500 can include a processor 552, a memory 554 (e.g., SRAM, DRAM, flash memory and/or other memory device), input/output devices 556 (e.g., a sensor and/or transmitter), and/or other subsystems or components 558. Semiconductor packages having any one or a combination of the features described above with reference to Figures 1-4 may be included in any of the devices shown in Figure 5. The resulting system 500 can perform any of a wide variety of computing, processing, storage, sensing, imaging, and/or other functions. Accordingly, the representative system 500 can include without limitation, computers and/or other data processors, for example, desktop computers, laptop computers, Internet appliances, hand-held device (palm-top computers, wearable computers, cellular or mobile phones, personal digital systems, music players, cameras, etc.), multi-processor systems, processor-based or programmable consumer electronics, network computers and mini-computers. Other representative systems 500 may be housed in a single unit or distributed over multiple interconnected units (e.g., through a communication network). The components of the system 500 can accordingly include local and/or remote storage devices, and any of a wide variety of computer-readable media.

[0043] From the foregoing, it will be appreciated that specific embodiments of the disclosure have been described for purposes of illustration, but that the foregoing systems and methods may have other embodiments as well. For example, while certain of the embodiments described above were described in the context of semiconductor packages having two or three stacked dies, in other embodiments, the packages can include other numbers of stacked dies. In some cases, the via 140 may not extend completely through the substrate, e.g., if the substrate

forms the topmost die shown in Figure 1. In such cases, the via 140 may still be used for thermal purposes, e.g., to act as a heat conduit or heat sink. The same processes described above can be used to form the via and terminal, but the terminal is not exposed at the second surface of the substrate. Such substrates can also be used for planar (unstacked) dies. In other embodiments, the terminal can be exposed to connect the planar (unstacked) die to PCBs or other support members or substrates. Many of the processes for forming the foregoing connected structures and connecting the mating structures of different semiconductor substrates can be carried out at the die level (e.g., after singulating the dies), the wafer level (e.g., before singulating the dies) and/or other processing stages.

[0044] Certain features described in the context of particular embodiments may be combined or eliminated in other embodiments. For example, the process of coating the sidewall surfaces described above with reference to Figure 4 can be applied to vias formed in association with the conductive structures shown in any of the other Figures. The process of removing substrate material from around the entire terminal opening, as shown in Figures 3C and 3D, can be applied to the terminal openings shown in Figures 2E or 2H. Further, while features and results associated with certain embodiments have been described in the context of those embodiments, other embodiments may also exhibit such features and results, and not all embodiments need necessarily exhibit such features and results. Accordingly, the disclosure can include other embodiments not expressly shown or described above.

CLAIMS

We claim:

1. A semiconductor assembly, comprising,

a semiconductor substrate including a substrate material having a first major surface, a second major surface, and an opening extending from the first major surface to the second major surface, the opening including a generally cylindrical portion extending generally normal to the first major surface, the cylindrical portion having a generally smooth, uniform surface, the opening further including a terminal portion extending transverse to the cylindrical portion and intersecting the second major surface, the terminal portion having a width generally parallel to the plane of the first major surface that is greater than a corresponding width of the cylindrical portion;

a single, uniform, homogeneous volume of conductive material disposed in both the cylindrical portion and the terminal portion of the opening, the conductive material forming a conductive path in the cylindrical portion and at least a portion of a conductive terminal in the terminal portion, the conductive terminal having a cross-section that is convexly rounded, wherein the cross-section is taken in a plane normal to the second major surface, wherein the convexly rounded conductive terminal projects away from the second major surface in a direction away from the first major surface, the conductive terminal having a first cross-sectional area and a second cross-sectional area greater than the first cross-sectional area, wherein the first cross-sectional area is in a first plane that is generally parallel to the second major surface and includes an outermost surface of the semiconductor substrate and the second cross-sectional area is in a second plane generally parallel to the first plane and positioned beyond the outermost surface; and

a microelectronic element formed in the substrate material and electrically coupled to the conductive material.

2. The assembly of claim 1:

wherein the conductive terminal includes a solderless material;

wherein an outer boundary of the conductive terminal tapers laterally outwardly in a direction away from the second major surface; and

wherein the assembly further comprises a solder ball attached to the conductive terminal, the solder ball being in contact with the tapered outer boundary of the conductive terminal.

3. The assembly of claim 1 wherein the conductive terminal has an outermost boundary at the terminal portion with a cross-sectional area greater than a cross-sectional area of the opening at the terminal portion.

4. The assembly of claim 1 wherein the conductive material is a solderless material.

5. The assembly of claim 1 wherein the cylindrical portion does not have a scalloped internal surface.

6. The assembly of claim 1 wherein the conductive material is at least 90% copper.

7. The assembly of claim 1 wherein an outer boundary of the conductive terminal projects laterally outwardly in a direction away from the outermost surface of the semiconductor substrate.

8. The assembly of claim 1 wherein the conductive material has a concave, cup-shaped void.

9. The assembly of claim 1 wherein the substrate material forms a portion of a first semiconductor die, and wherein the conductive material is at least 90% copper and wherein the semiconductor assembly further comprises a second semiconductor die having a conductive terminal electrically connected to the conductive terminal of the first semiconductor die.

10. The assembly of claim 1 wherein the conductive terminal has a generally spherical shape intersecting the second major surface of the substrate material and beyond the outermost surface of the semiconductor substrate.

11. The assembly of claim 1 wherein the terminal portion has generally flat walls aligned with crystal planes of the semiconductor substrate material.

12. The assembly of claim 1, further comprising:

a seed layer on an outer boundary of the conductive material at the terminal portion; and

a barrier layer on an outer boundary of the seed layer at the terminal portion, wherein the seed layer and the barrier layer project outward beyond the outermost surface of the semiconductor substrate, and wherein the conductive terminal comprises the seed layer, the barrier layer, and the conductive material.

13. A semiconductor assembly, comprising,

a semiconductor substrate including a substrate material having a first major surface, a second major surface, and an opening extending from the first major surface to the second major surface, the opening including a generally cylindrical portion extending generally normal to the first major surface, the cylindrical portion having a generally smooth, uniform surface, the opening further including a terminal portion extending transverse to the cylindrical portion and intersecting the second major surface, the terminal portion having a width generally parallel to the plane of the first major surface that is greater than a corresponding width of the cylindrical portion;

a single, uniform, homogeneous volume of conductive material disposed in both the cylindrical portion and the terminal portion of the opening, the conductive material forming a conductive path in the cylindrical portion and at least a portion of a conductive terminal at the terminal portion, wherein the conductive terminal has an outermost boundary that projects laterally outward beyond an outermost surface of the semiconductor substrate substantially parallel to the second major surface;

a microelectronic element formed in the substrate material and electrically coupled to the conductive material;

a seed layer on an outer boundary of the conductive material at the terminal portion; and

a barrier layer on an outer boundary of the seed layer at the terminal portion, wherein the seed layer and the barrier layer project outward beyond the outermost surface of the semiconductor substrate, and wherein the conductive terminal comprises the seed layer, the barrier layer, and the conductive material.