(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
3 July 2003 (03.07.2003)

PCT

(10) International Publication Number
WO 03/054951 A1

(51) International Patent Classification[7]: H01L 21/336, 21/265

(21) International Application Number: PCT/US02/41103

(22) International Filing Date:
19 December 2002 (19.12.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/021,037 19 December 2001 (19.12.2001) US

(71) Applicant: ADVANCED MICRO DEVICES, INC. [US/US]; One AMD Place, Mail stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

(72) Inventors: LUNING, Scott; 1104 Mission Ridge, Austin, TX 78704 (US). KADOSH, Daniel; 2803 W. 50th Street, Austin, TX 78731 (US). CHEEK, Jon, D.; 3602 Newland Place, Round Rock, TX 78681 (US). BULLER, James, F.; 6908 Indica Cove, Austin, TX 78759 (US).

(74) Agent: COLLOPY, Daniel, R; Advanced micro devices, INC., One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

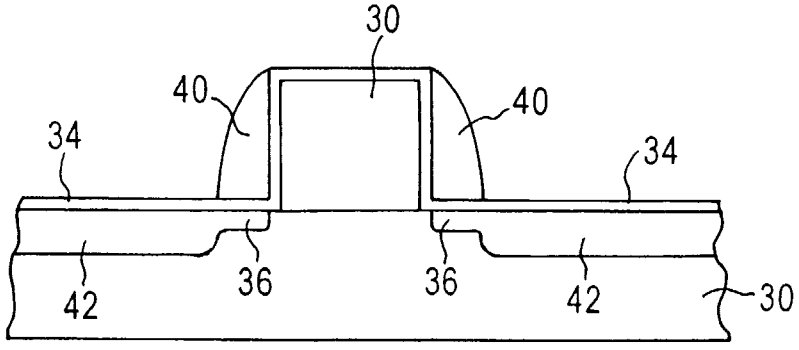
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SEMICONDUCTOR DEVICE COMPRISING A THIN OXIDE LINER AND METHOD OF MANUFACTURING THE SAME



(57) Abstract: A method of forming a semiconductor device provides a gate electrode (32) on a substrate (30); and an oxide liner (34) that is less than 100 A in thickness on the substrate (30) and the gate electrode (32). A nitride layer (38) is formed on the oxide liner (34). The nitride layer (38) is etched to form nitride spacers (40), the etching stopping on the oxide liner (34). The thinner oxide liner (34), e.g., less than 100 A, prevents the liner (34) from acting as a sink for dopants during thermal processing so that the dopants in the source/drain extension regions (36) and the source/drain regions (42) remain in the substrate (30) during the thermal processing, thereby preventing degradation of transistor performance.

WO 03/054951 A1