

CLAIMS

1. A computer-implemented method of facilitating processing within a computing environment, said computer-implemented method comprising:
 - obtaining an instruction to test for one or more pending external interrupts; and
 - executing the instruction, the executing including:
 - determining, based on information provided by the instruction, one or more external interruption subclasses to be tested;
 - checking whether one or more external interruptions are pending for the one or more external interruption subclasses being tested; and
 - indicating whether one or more external interruptions are pending for the one or more external interruption subclasses being tested.
2. The method of claim 1, wherein the determining comprises examining a mask provided in a location designated by the instruction to determine the one or more external interruption subclasses to be tested.
3. The method of claim 2, wherein the mask includes a plurality of indicators for a plurality of external interruption subclasses, and an indicator of the plurality of indicators set to a defined value indicates that an external interruption subclass corresponding to the indicator is to be tested.
4. The method of claim 3, wherein the plurality of external interruption subclasses comprises a warning track interruption, a malfunction alert, an emergency signal and an external call.
5. The method of any of claims 2 to 4, wherein the location comprises a register designated by a field of the instruction.
6. The method of any of the preceding claims, wherein the indicating comprises setting, for an external interruption subclass having a pending external interruption, an indicator in a location specified by the instruction.

7. The method of claim 6, wherein the location is a register specified by a field of the instruction.
8. The method of claim 7, wherein the indicator is a bit in a mask in the register specified by the instruction.
9. The method of any of the preceding claims, wherein the executing the instruction is performed regardless of whether a processor executing the instruction is enabled for interrupts.
10. The method of any of the preceding claims, wherein the executing further includes providing a summary indication indicating whether one or more external interruptions are pending for the one or more external interruption subclasses being tested.
11. The method of any of the preceding claims, wherein the instruction is a single architected instruction comprising an operation code specifying a test pending external interruption instruction, a first register field to be used in the indicating, and a second register field to be used in the determining.
12. A computer system for facilitating processing within a computing environment, said computer system comprising:
 - a memory; and
 - a processor in communication with the memory, wherein the computer system is configured to perform a method, said method comprising:
 - obtaining an instruction to test for one or more pending external interrupts; and
 - executing the instruction, the executing including:
 - determining, based on information provided by the instruction, one or more external interruption subclasses to be tested;
 - checking whether one or more external interruptions are pending for the one or more external interruption subclasses being tested; and
 - indicating whether one or more external interruptions are pending for the one or more external interruption subclasses being tested.

13. The computer system of claim 12, wherein the determining comprises examining a mask provided in a location designated by the instruction to determine the one or more external interruption subclasses to be tested, the mask including a plurality of indicators for a plurality of external interruption subclasses, and wherein an indicator of the plurality of indicators set to a defined value indicates that an external interruption subclass corresponding to the indicator is to be tested.

14. The computer system of either of claims 12 or 13, wherein the executing the instruction is performed regardless of whether a processor executing the instruction is enabled for interrupts.

15. The computer system of any of claims 12 to 14, wherein the executing further includes providing a summary indication indicating whether one or more external interruptions are pending for the one or more external interruption subclasses being tested.

16. A computer program product facilitating processing within a computing environment, the computer program product comprising:
a computer readable storage medium readable by a processing circuit and storing instructions for execution by the processing circuit for performing a method according to any of claims 1 to 11.

17. A computer program stored on a computer readable medium and loadable into the internal memory of a digital computer, comprising software code portions, when said program is run on a computer, for performing the method of any of claims 1 to 11.

18. A computer program stored on a computer readable medium and loaded into the internal memory of the system of any of claims 12 to 15, comprising software code portions, when said program is run on the system, for performing the method of any of claims 1 to 11.