CLAIMS

1. A method, comprising: clocking a processor at a default clocking frequency while the processor operates in a default mode of operation using a default number of execution units and while the processor draws a default current from a power rail; responsive to a first projected increase in a load for the processor in which the processor operates in a first increased load mode of operation using a first multiple of the default number of execution units, determining a first decreased clocking frequency that is inversely proportional to the first multiple of the default number of execution units, wherein the first multiple is a number greater than one and the first decreased clocking frequency is less than the default clocking frequency; and clocking the processor at the first decreased clocking frequency while the processor performs a transition from the default mode of operation to the first increased load mode of operation so that the processor draws substantially the default current from the power rail during the transition from the default mode of operation to the first increased load mode of operation.

2. The method of claim 1, further comprising: generating a first processor clock signal to cycle at the default clocking frequency so that edges of the first processor clock signal are synchronous with edges of a source clock signal, wherein clocking the processor at the default clocking frequency comprises clocking the processor with the first processor clock signal, and wherein a frequency of the source clock signal is an integer multiple of the default clocking frequency; and generating a second processor clock signal to cycle at the first decreased clocking frequency so that edges of the second processor clock signal are synchronous with edges of the source clock signal, wherein clocking the processor at the first decreased clocking frequency comprise clocking the processor with the second processor clock signal.

3. The method of claim 2, further comprising: generating the source clock signal in a phase-locked loop, wherein the phase-locked loop remains locked while the processor transitions from the default mode of operation to the first increased load mode of operation.

4. The method of claim 2, wherein clocking the processor with the second processor clock signal while the processor transitions from the default mode of operation to the first increased load of operation comprises clocking the processor at the first decreased clocking frequency for a first predetermined number of periods of the second processor clock signal.

5. The method of claim 4, further comprising: following the first predetermined number of periods for the second processor clock signal, clocking the processor with the first processor clock signal for a second predetermined number of periods for the first processor clock signal.

6. The method of claim 1, further comprising: determining a set of multiples of the default number of execution units, wherein the set of multiples ranges across an expected range of usage of the execution units for the processor; responsive to a second projected increase in processor load in which the processor operates in a second increased load mode of operation using a second multiple of the default number of execution units, quantizing the second multiple to a corresponding multiple from the set of multiples of the default number of execution units; mapping the corresponding multiple to a second reduced clocking frequency that is inversely proportional to the corresponding multiple; and clocking the processor at the second reduced clocking frequency as the processor transitions from the default mode of operation to the second increased mode of operation.

7. The method of claim 6, wherein the mapping the corresponding multiple comprises mapping the corresponding multiple through a lookup table.

8. A system, comprising: a clock source for providing a source clock signal having a source clock frequency; a clock divider configured to divide the source clock signal into a processor clock signal having a divided frequency; a processor including a plurality of execution units, wherein the processor is configured to operate in a default mode of operation in which the processor uses a default number of the execution units from the plurality of execution units to be clocked in each cycle of the processor clock signal and to operate in an increased load mode of operation in which the processor uses a multiple of the default number of the execution units to be clocked in each cycle of the processor clock signal, wherein the processor is further configured to assert an activity code to predict a transition from the default mode of operation to the increased load mode of operation; and a look-up table configured to map the activity code to a first command for the reduced frequency, and wherein the clock divider is configured to respond to the first command for the reduced frequency so that the divided frequency of the processor clock signal equals a reduced frequency that is inversely proportional to the multiple of the default number of execution units while the processor is configured to perform the transition from the default mode of operation to the increased load mode of operation.

9. The system of claim 8, wherein the clock source comprises a phase-locked loop configured to remain locked while the processor is configured to perform the transition from the default mode of operation to the increased load mode of operation.

10. The system of claim 8, wherein the system comprises a system-on-a-chip (SoC).

11. The system of claim 8, wherein the processor comprises a graphics processing unit (GPU) and wherein the plurality of execution units comprises a plurality of multiply-and-accumulate (MAC) units.

12. The system of claim 8, further comprising: a power source configured to regulate a power supply voltage on a power rail, wherein the processor is further configured to draw a default current from the power rail while the processor operates in the default mode of operation, and wherein the processor is further configured to substantially draw the default current from the power rail while the processor is configured to perform the transition from the default mode of operation to the increased load mode of operation.

13. The system of claim 8, wherein the system comprises a system-on-a-chip (SoC).

14. A system, comprising: a clock source for providing a source clock signal having a source clock frequency; a clock divider configured to divide the source clock signal into a processor clock signal having a divided frequency; and a processor including a plurality of execution units, wherein the processor is configured to operate in a default mode of operation in which the processor uses a default number of the execution units from the plurality of execution units to be clocked in each cycle of the processor clock signal and to operate in an increased load mode of operation in which the processor uses a multiple of the default number of the execution units to be clocked in each cycle of the processor clock signal, wherein the processor is further configured to assert an activity code to predict a transition from the default mode of operation to the increased load mode of operation and to map the activity code to a first command for the reduced frequency, and wherein the clock divider is configured to respond to the first command for the reduced frequency so that the divided frequency of the processor clock signal equals a reduced frequency that is inversely proportional to the multiple of the default number of execution units while the processor is configured to perform the transition from the default mode of operation to the increased load mode of operation.

15. The system of claim 14, wherein the clock source comprises a phase-locked loop configured to remain locked while the processor is configured to perform the transition from the default mode of operation to the increased load mode of operation.