

SPECIFICATION

A complementary amplifier circuit

- 5 The present invention relates to a complementary amplifier circuit and, more particularly, to a complementary metal-insulator-semiconductor (C-MIS) amplifier circuit comprising a p-channel metal-insulator-semiconductor field effect transistor (hereinafter referred to as a MISFET or simply as a FET) and an n-channel MISFET.

Complementary field effect transistor amplifier circuits are widely used in electronic circuits, such as for example an oscillator of an electronic wrist watch. Such a circuit has high threshold levels, inherent structural simplicity and low power consumption.

Various types of improved circuits which enjoy the low power characteristic of the complementary FET amplifier have been proposed.

For instance, as will be described later with specific reference to Fig. 1 of the accompanying drawing, we have proposed to connect, through a bias resistor, the gate and drain electrodes of each MISFET constituting the complementary amplifier to each other to equalize the gate potential and the drain potential and, at the same time, to connect the drain electrodes of two FETs through a load resistor to effect B-class operation to reduce the through current and, hence, the power consumption. This type of amplifier circuit is disclosed in the specification of United States Patent No. 4,100,502.

However the amplifier circuit shown in U.S. Patent No. 4,100,502 operation voltage which is higher than the sum of the threshold voltages of the two MISFETs constituting the complementary amplifier circuit.

In order that a MIS amplifier circuit can operate with an operating voltage which is only higher than the threshold voltage of each of the MISFETs constituting the amplifier circuit, the specification of United States Patent No. 3,887,881 discloses an amplifier circuit in which two potential divider circuits, to each of which a MISFET is connected in series are connected in parallel with a C-MIS amplifier circuit, the output from the potential divider circuit being applied to the gate electrodes of the FETs constituting a C-MOS amplifier.

However in the amplifier circuit disclosed in U.S. Patent No. 3,887,881, the operating voltage fluctuates undesirably and unstable operation of the amplifier results due to the fluctuation of characteristics of the circuit constituents, because the gate electrodes of the MOSFETs constituting the C-MOS amplifier circuit have fixed bias voltages applied to them.

It is an object of the present invention to provide a C-MIS amplifier circuit having low operational lower limit and capable of performing a stable amplification even if the

operation voltage fluctuates and having a reduced power consumption.

According to the present invention there is provided a complementary amplifier circuit including: a first FET of a first conductivity type having a gate electrode connected to an input terminal, a source electrode connected to a first potential source and a drain electrode; a second FET of a second conductivity type having a gate electrode, a source electrode connected to a second potential source and a drain electrode; a connecting means connected between the drain electrodes of said first and second FETs; a bias resistive means connected between the gate and the drain electrodes of said first FET; a capacitor connected between the gate electrodes of said first and second FETs; a third FET of the second conductivity type of which the gate and the second are connected to the gate and the source of said second FET respectively; a resistive means connected between the drain and the gate electrodes of said third FET; and load means connected between said first potential source and the drain electrode of the third FET.

In this circuit arrangement, the first FET is D.C. biased to its threshold voltage by the bias resistor, whilst the second FET is D.C. biased to its threshold voltage by the third MISFET. In addition, the gates of the first and second FETs are arranged to receive A.C. input signals which are separated from each other in D.C. sense.

Therefore, even if the operating voltage applied between the source electrodes of the first and the second FETs fluctuates, the amplifier circuit performs correct and stable amplification as long as the operating voltage is maintained higher than the higher one of the threshold voltages of the first and the second FETs. Also, since B-class operation is effected, the level at which the first and second complementary FETs become conductive simultaneously against an A.C. signal amplitude is minimized in order to reduce the power consumption.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawing, wherein:—

Figure 1 is a circuit diagram of a conventional complementary amplifier circuit.

Figures 2 and 3 are circuit diagrams of two preferred forms of complementary amplifier circuits in accordance with the present invention.

Referring to Fig. 1, a conventional complementary FET amplifier circuit similar to that shown in the Specification of U.S. Patent No. 4,100,502 includes a p-channel FET M_p connected to a potential source $+V_{DD}$ and an n-channel FET M_n connected to a different potential source V_{SS} (earth), the two FETs being connected in series in order to form a comple-

mentary amplifier. Between the complementary FETs M_p and M_n , two load resistors R_{L1} and R_{L2} of equivalent resistance are connected in series. Further, biasing resistors R_{F1} and R_{F2} are connected for the FETs M_p and M_n between the gate and drain electrodes thereof, respectively. The gate electrodes of the FETs M_p and M_n are supplied with an input signal V_{in} , the gate electrode of the FET M_p being supplied with the input signal V_{in} through a capacitor C_1 for A.C. coupling.

In the above described complementary FET amplifier circuit the bias resistors R_{F1} and R_{F2} are connected between the gate and drain electrodes of the FETs M_p and M_n respectively, the gate electrodes of these FETs being isolated in a D.C. sense from each other by the capacitor C_1 , so that the FETs are self-biased. Therefore, the above described amplifier undergoes B-class operation and, as the through current which is generated when both of the FETs M_p and M_n are simultaneously turned on is decreased, the power consumption of the amplifier circuit is conveniently reduced.

However, in order for the above-described amplifier to perform a correct amplification operation, the operating voltage applied between the terminals $+V_{DD}$ and V_{SS} has to be greater than the sum of the threshold voltages V_{THN} and V_{THP} of two FETs M_n and M_p . This sum of threshold voltages hereinafter will be referred to as the "operational lower limit voltage". Therefore, if the operating voltage supplied by the power source has decreased below the level of the operational lower limit voltage, the amplifier will fail to operate correctly.

Referring now to the first embodiment shown in Fig. 2, the complementary amplifier circuit includes a p-channel MISFET 1 (M_{P1}) and an n-channel MISFET 2 (M_{N1}) which are complementary to each other. These two MISFETs are connected in series between a power source line 4 which provides a first source potential V_{DD} and an earth line 5 which provides a second source potential. An output V_{out} is derived from the junction point 6 between the drain electrodes of these MISFETs 1 and 2. The gate and drain electrodes of the MISFET 1 are connected to each other through a self-bias resistor 7.

Broadly, metal insulator semiconductor field effect transistors (MISFETs) can be classified into the two types, namely a thin-film transistor (TFT) and a metal oxide semiconductor transistor (MOSFET). Since the MOS field effect transistors are more popular, the following description will be made with reference to the cases where MOSFETs are used rather than TFTs. In order to simplify the description, the MOSFETs will hereinafter be referred to simply as FETs.

The gate electrode of the FET 2 (M_{N1}) is connected to the gate electrode of the FET

(M_{P1}) through a capacitor 8. An input signal V_{in} is applied to the input terminal 9 and thus applied to the gate electrodes of both FETs.

A resistor 10 (R_2) and the drain-source path of an n-channel FET 3 (M_{N2}), which together constitute means for supplying electric current, are connected between the source line 4 and the earth line 5. The gate and source electrodes of the FET 3 (M_{N2}) are connected to each other through a resistor 12 (R_2), and the gate electrode of the FET 3 (M_{N2}) is also connected to the gate electrode of the FET 2 (M_{N1}).

In the above-described complementary amplifier circuit, the gate of the FET 1 (M_{P1}) is connected to the drain electrode thereof through a bias resistor 7 (R_1) the resistance of which is between 10 and 100 M ohms. Therefore, the gate potential is set in a D.C. sense substantially at the same level as the threshold voltage V_{THP} of the FET 1 (M_{P1}) to effect the amplification of the negative part of the cycle of the input signal.

Also, the gate electrode of the FET 2 (M_{N1}) is connected to the gate electrode of the FET 3 (M_{N2}) of the mirror circuit which is constituted by resistors 10, 12 and the FET 3. Therefore the D.C. bias is set at the level of the threshold voltage V_{THN} of the FET 2 to effect the amplification of the positive part of the cycle of the input signal. The capacitor 8 functions to isolate the gate potentials of the FETs 1 and 2 in a D.C. sense. In the described embodiment, the gate and drain electrodes of the p-channel FET 1 are connected to each other by means of the self-bias resistor 7, and the gate and drain of the n-channel FET 2 are isolated from each other. However, the gate and drain of the n-channel FET 3 are connected to each other by means of a resistor 12.

In the above described complementary amplifier circuit, the source voltage V_{DD} for simultaneously operating the FETs 1 and 2 has only to be higher than the higher one of the threshold voltage V_{THP} of the p-channel FET 1 and the threshold voltage V_{THN} of the n-channel MOSFET 2 (M_{N2}). Therefore, the amplifier can operate even after the source voltage V_{DD} has decreased below the value of one of these threshold voltages.

Assuming here that the threshold voltage V_{THP} and V_{THN} are equal, the operational lower limit voltage is lowered to one half of that of the conventional complementary amplifier circuit. When the operational voltage is lowered, the potential at the gate electrode of the FET 1 (M_{P1}) is decreased below the potential at the gate of the transistor 2, so that the capacitor 7 is charged such that the potential is higher at its one side connected to the gate electrode of the FET 2 than at the side thereof connected to the gate electrode of the FET 1.

In addition, the level at which the FETs 1 and 2 are simultaneously conductive against

an A.C. signal amplitude is minimized in order to reduce the power consumption.

Furthermore, stable operation of the amplifier is ensured even under a fluctuation of the characteristics of the constituent elements and the fluctuation of the source voltage, because the bias voltage of the FET is set by self-biasing.

Because of these features, the above described amplifier circuit is suitable particularly for such a use as requiring a high input impedance, e.g. an amplifier which is used in combination with the quartz oscillator of a wrist watch.

Referring now to the second embodiment shown in Fig. 3, a block 13 enclosed by broken lines includes the elements shown in the circuit of Fig. 2. However, in order to reduce the size of the circuit, a pair of parallel complementary FETs 15 and 16 constituting a high resistance and p-channel FET 17 (M_{p2}) as resistance means are substituted for the self-bias resistor 7 and the load resistance 10, respectively.

Similarly, in a modified form (not shown), a FET may be used in place of the bias resistance 12 (R_3) of the FET 3.

Resistors 18 and 19 which are connected in series between the drain electrodes of the MISFETs 1 and 2 cooperate with each other in order to limit the through current flowing between the FETs 1 and 2, and also in making the bias voltage between the gate and source electrodes approach the threshold voltage in order to further reduce the power consumption.

A quartz oscillator 21 and input/output capacitors 22, 23 are connected between the gate electrode of the FET 1 which is the input terminal of the amplifier and the junction between the resistors 18 and 19, through an output resistor 20, thereby constituting a quartz oscillator circuit. Since the quartz oscillator circuit operates in conventional manner, its operation will be described.

The drain electrodes of the FETs 1 and 2 are connected to respective gate electrodes of FETs 24 and 25 which constitute a wave shaping circuit which form part of another complementary amplifier.

If the output voltage is applied to the junction between the resistors 18 and 19, the through current in the above-mentioned wave shaping circuit becomes large thereby increasing the power consumption. A rectangular wave form is obtained at the output terminal of the wave shaping circuit, if the output voltage derived from the drain electrodes of the FETs 1 and 2 is applied to the wave shaping circuit, because the latter has no load resistor therein. Therefore, the D.C. component of the signal applied between the source and gate electrodes of each of the FETs 24 and 25 is substantially equal to the threshold voltage, so that the period in which the FETs

24 and 25 are concurrently conductive is shortened in order to reduce the power consumption.

70 CLAIMS

1. A complementary amplifier circuit including: a first FET of a first conductivity type having a gate electrode connected to an input terminal, a source electrode connected to a first potential source and a drain electrode; a second FET of a second conductivity type having a gate electrode, a source electrode connected to a second potential source and a drain electrode; a connecting means connected between the drain electrodes of said first and second FETs; a bias resistive means connected between the gate and the drain electrodes of said first FET; a capacitor connected between the gate electrodes of said first and second FETs; a third FET of the second conductivity type of which the gate and the source are connected to the gate and the source of said second FET respectively; a resistive means connected between the drain and the gate electrodes of said third FET; and load means connected between said first potential source and the drain electrode of the third FET.

2. A complementary amplifier circuit according to Claim 1, wherein said load means is a resistor.

3. A complementary amplifier circuit according to Claim 1, wherein said load means is constructed by a fourth FET of the first conductivity type of which the gate, the source and the drain electrodes are connected to said second potential source, said first potential source and the drain electrode of the third FET respectively.

4. A complementary amplifier circuit according to any one of the preceding claims, wherein said bias resistive means comprises a pair of complementary FETs arranged so that their source-drain paths are connected in parallel.

5. A complementary amplifier circuit according to Claim 1, wherein said connecting means comprises two resistors connected in series between the drain electrodes of said first and second FETs.

6. A complementary amplifier circuit according to Claim 5, further including a positive feed-back circuit connected between the junction point between said two resistors and the gate of said first FET, said feedback circuit comprising a crystal oscillator.

7. A complementary amplifier circuit according to Claim 6, further including a wave shaping circuit having a fourth FET of the first conductivity type and fifth FET of a second conductivity type, the drain-source paths being connected in series, and each gate electrode of said fourth and fifth FET is connected to drain electrodes of said first and second FETs respectively.



an A.C. signal amplitude is minimized in order to reduce the power consumption.

Furthermore, stable operation of the amplifier is ensured even under a fluctuation of the characteristics of the constituent elements and the fluctuation of the source voltage, because the bias voltage of the FET is set by self-biasing.

Because of these features, the above described amplifier circuit is suitable particularly for such a use as requiring a high input impedance, e.g. an amplifier which is used in combination with the quartz oscillator of a wrist watch.

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Similarly, in a modified form (not shown), a FET may be used in place of the bias resistance 12 (R_3) of the FET 3.

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A quartz oscillator 21 and input/output capacitors 22, 23 are connected between the gate electrode of the FET 1 which is the input terminal of the amplifier and the junction between the resistors 18 and 19, through an output resistor 20, thereby constituting a quartz oscillator circuit. Since the quartz oscillator circuit operates in conventional manner, its operation will be described.

The drain electrodes of the FETs 1 and 2 are connected to respective gate electrodes of FETs 24 and 25 which constitute a wave shaping circuit which form part of another complementary amplifier.

If the output voltage is applied to the junction between the resistors 18 and 19, the through current in the above-mentioned wave shaping circuit becomes large thereby increasing the power consumption. A rectangular wave form is obtained at the output terminal of the wave shaping circuit, if the output voltage derived from the drain electrodes of the FETs 1 and 2 is applied to the wave shaping circuit, because the latter has no load resistor therein. Therefore, the D.C. component of the signal applied between the source and gate electrodes of each of the FETs 24 and 25 is substantially equal to the threshold voltage, so that the period in which the FETs

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2. A complementary amplifier circuit according to Claim 1, wherein said load means is a resistor.

3. A complementary amplifier circuit according to Claim 1, wherein said load means is constructed by a fourth FET of the first conductivity type of which the gate, the source and the drain electrodes are connected to said second potential source, said first potential source and the drain electrode of the third FET respectively.

4. A complementary amplifier circuit according to any one of the preceding claims, wherein said bias resistive means comprises a pair of complementary FETs arranged so that their source-drain paths are connected in parallel.

5. A complementary amplifier circuit according to Claim 1, wherein said connecting means comprises two resistors connected in series between the drain electrodes of said first and second FETs.

6. A complementary amplifier circuit according to Claim 5, further including a positive feed-back circuit connected between the junction point between said two resistors and the gate of said first FET, said feedback circuit comprising a crystal oscillator.

7. A complementary amplifier circuit according to Claim 6, further including a wave shaping circuit having a fourth FET of the first conductivity type and fifth FET of a second conductivity type, the drain-source paths being connected in series, and each gate electrode of said fourth and fifth FET is connected to drain electrodes of said first and second FETs respectively.



8. A complementary amplifier circuit constructed and arranged to operate substantially as herein described with reference to and as illustrated in Fig. 2 or Fig. 3 of the accompanying drawing.

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The first thing I noticed when I stepped out of the car was the cold, crisp air. It was a relief after the warm, humid weather of the city. I walked towards the entrance of the building, my eyes scanning the architecture. The building was a grand, multi-story structure with a classical facade. The entrance was flanked by two large columns, and a set of stairs led up to a portico. I noticed a few people walking around, some in uniform, others in civilian clothes. I felt a sense of anticipation and nervousness. This was my first time in a place like this. I took a deep breath and walked up the stairs. The portico was open to the sky, and I could see the city in the background. I felt a sense of awe and wonder. This was a moment I would never forget.