FIG. 1A

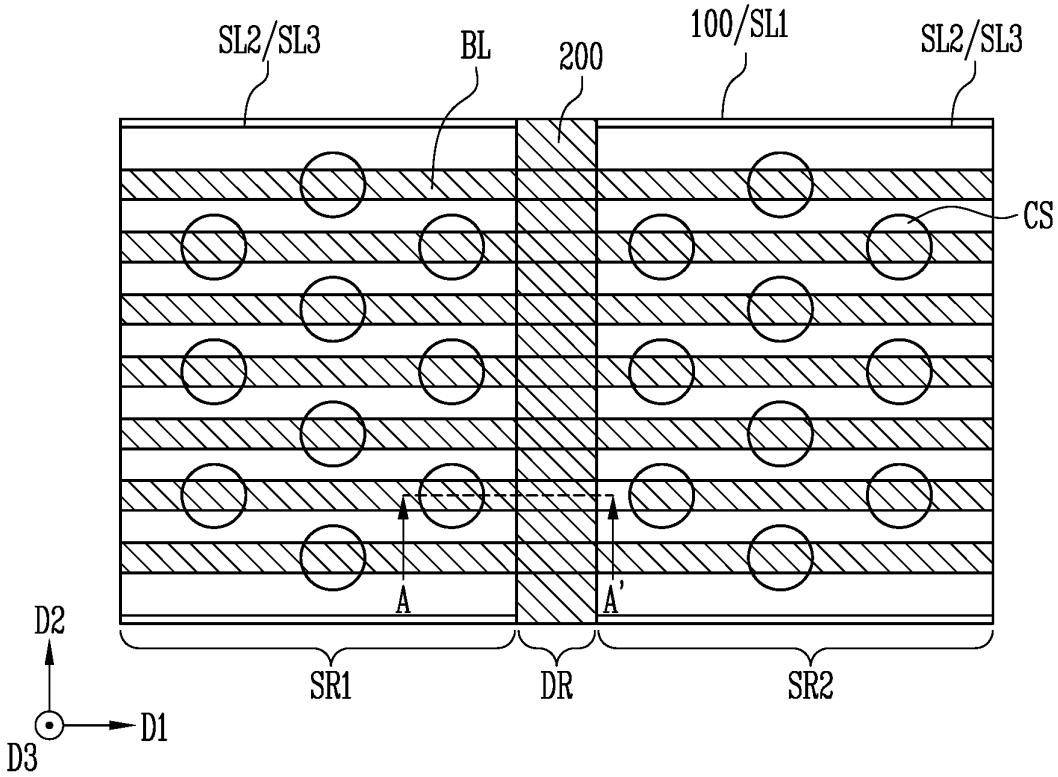


FIG. 1B

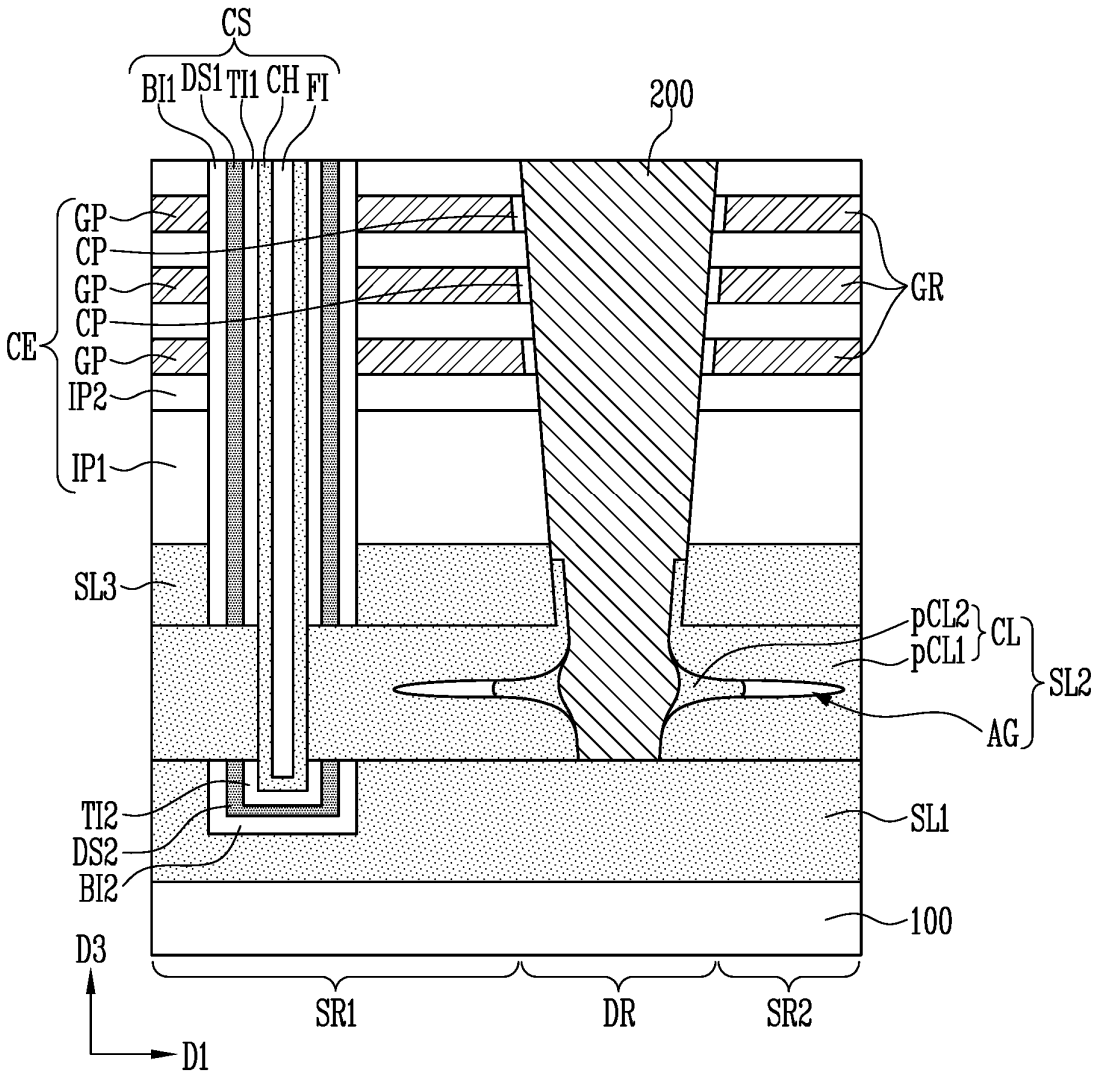

CS
BI1
DS1
TI1
CH
FI
200
GP
CP
GP
CP
GP
CE
IP2
IP1
GR
SL3
pCL2
pCL1
CL
SL2
AG
TI2
DS2
BI2
SL1
100
D3
D1
SR1
DR
SR2

FIG. 2A

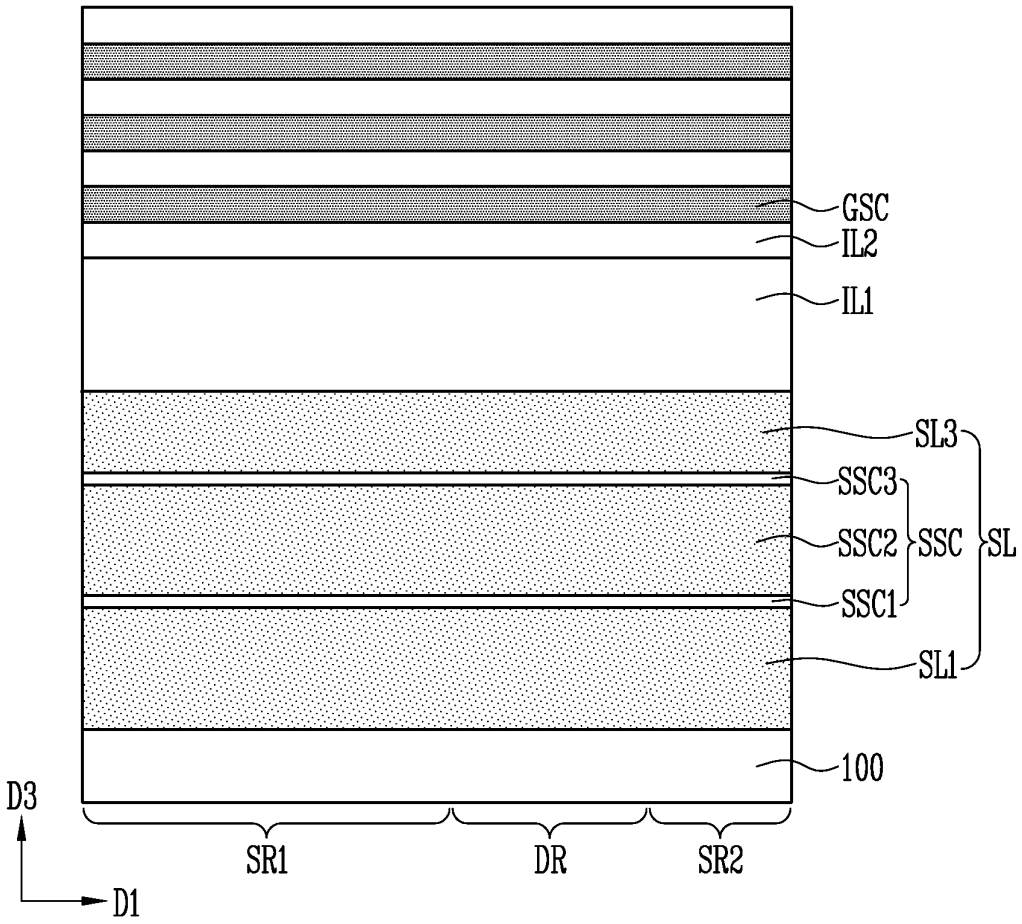


FIG. 2B

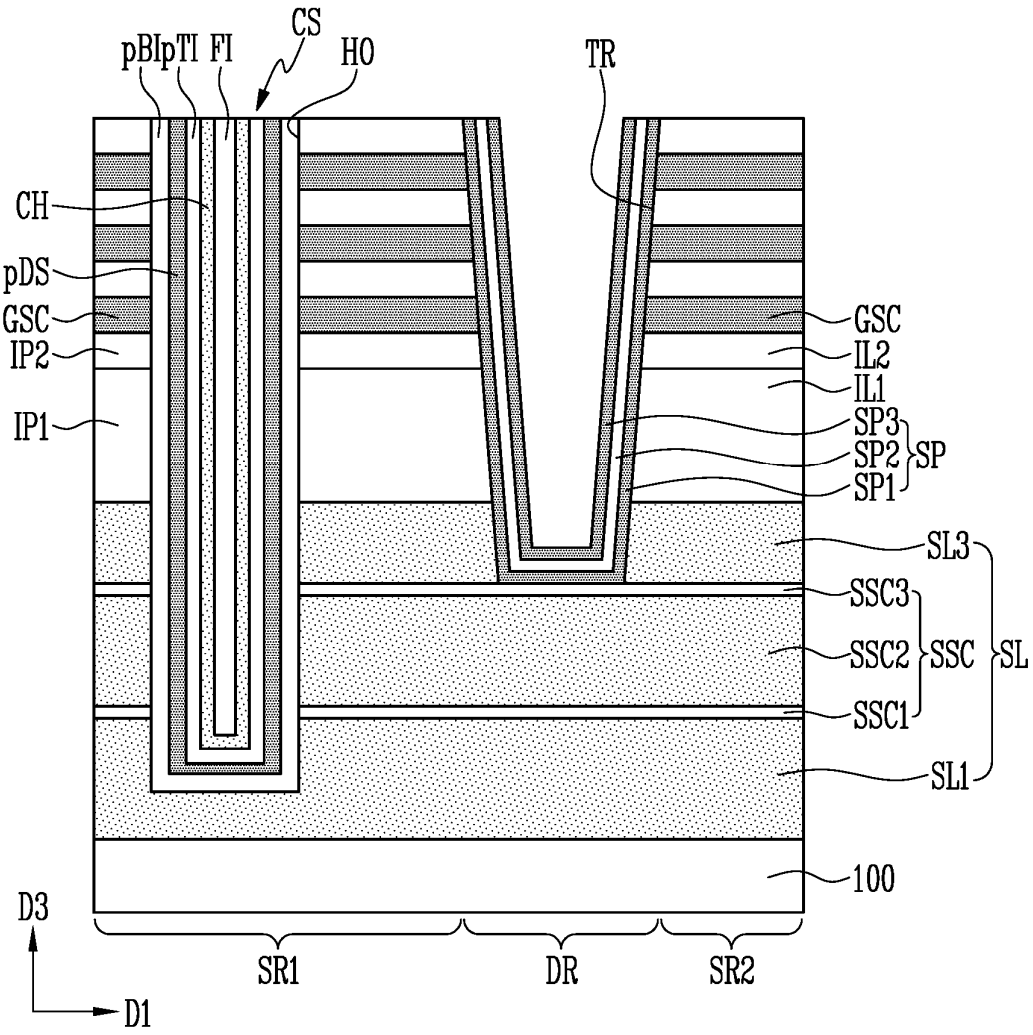

CS
pBI
pTI
FI
HO
TR
CH
pDS
GSC
IP2
IP1
GSC
IL2
IL1
SP3
SP2
SP1
SP
SL3
SSC3
SSC2
SSC1
SSC
SL
SL1
100
D3
D1
SR1
DR
SR2

FIG. 2C

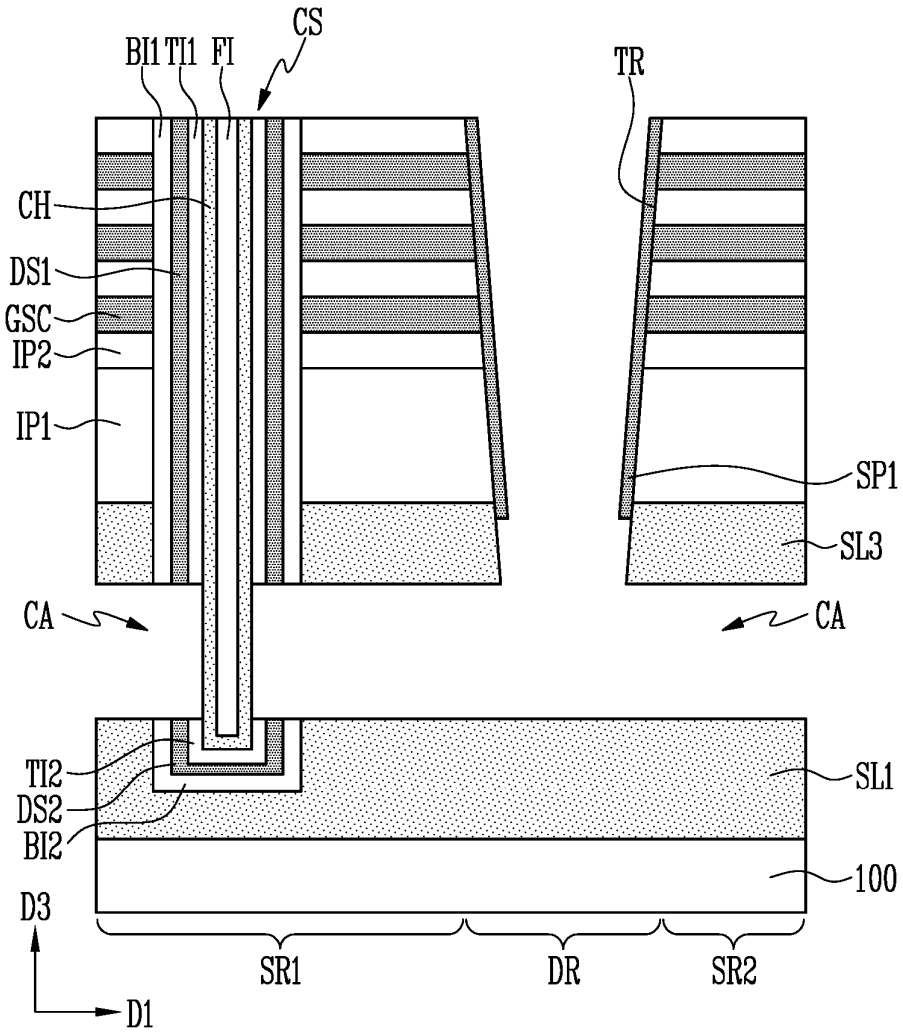

CS
BI1
TI1
FI
TR
CH
DS1
GSC
IP2
IP1
SP1
SL3
CA
CA
TI2
DS2
BI2
SL1
100
D3
D1
SR1
DR
SR2

FIG. 2D

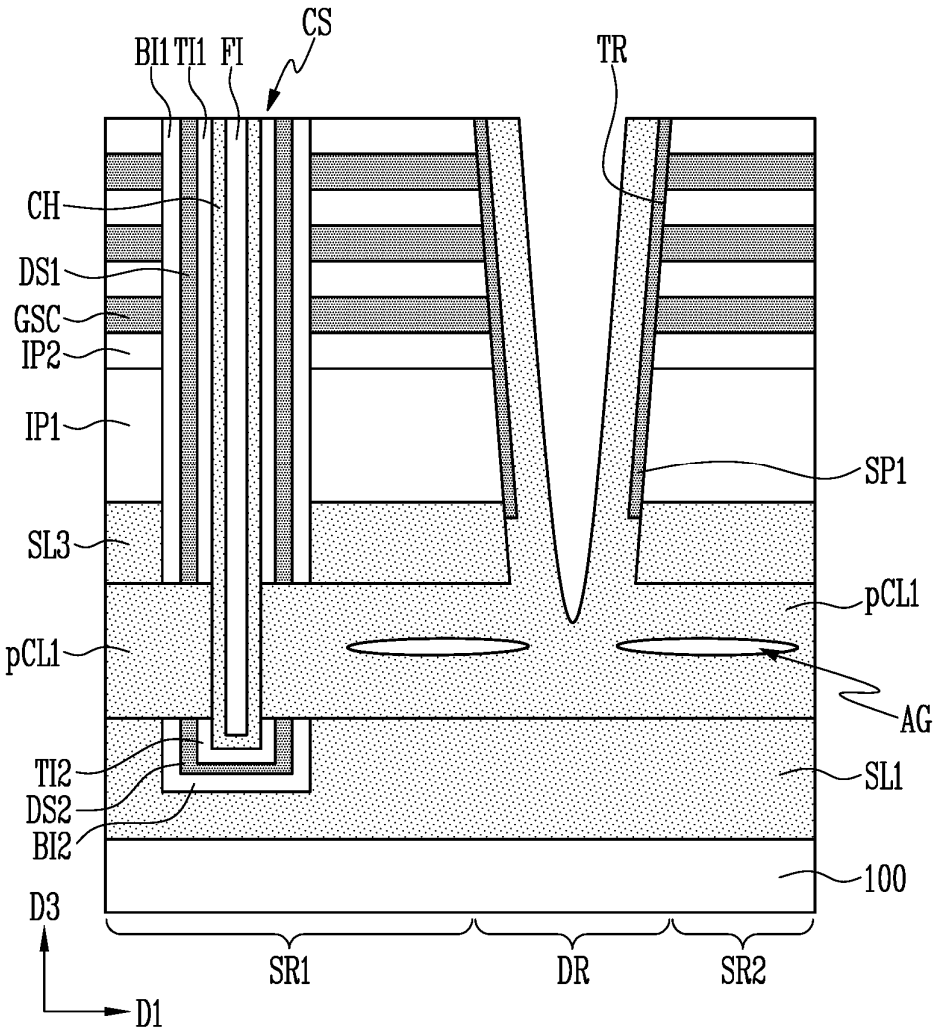

CS
BI1
TI1
FI
TR
CH
DS1
GSC
IP2
IP1
SP1
SL3
pCL1
pCL1
AG
TI2
DS2
BI2
SL1
100
D3
D1
SR1
DR
SR2

FIG. 2E

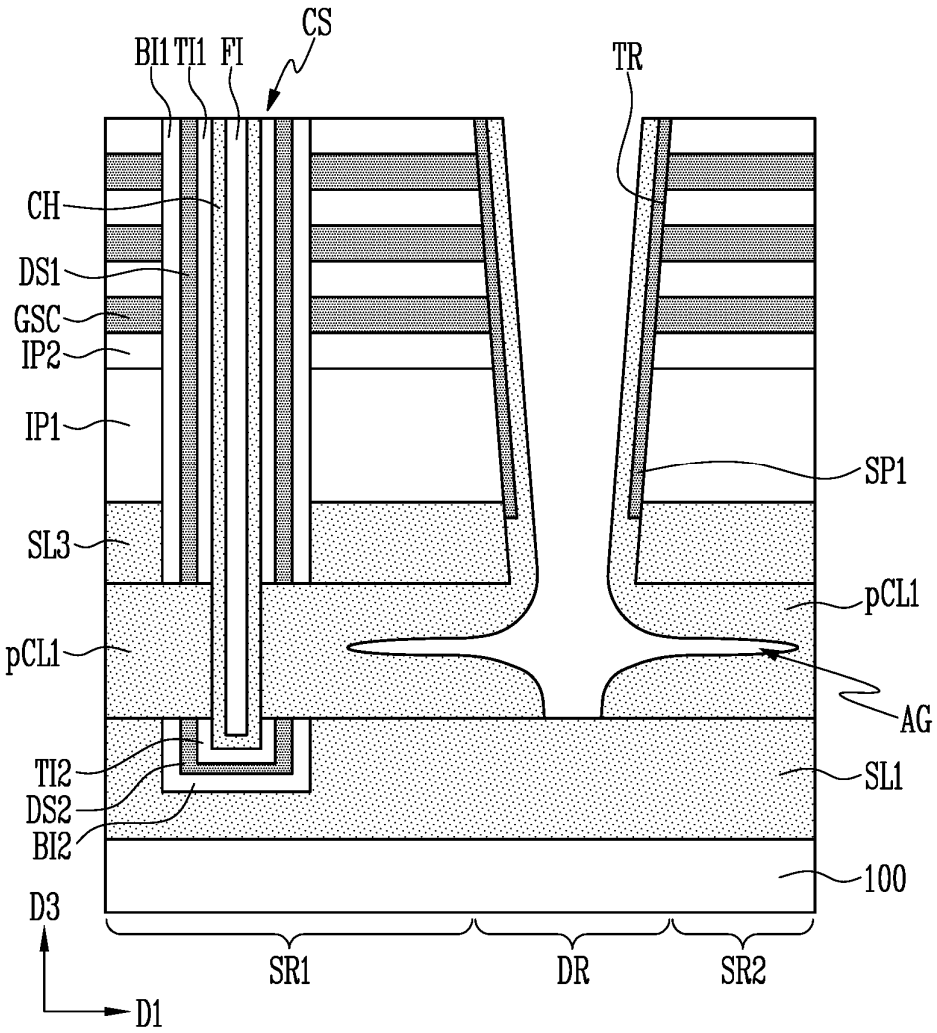

CS
BI1
TI1
FI
TR
CH
DS1
GSC
IP2
IP1
SP1
SL3
pCL1
pCL1
AG
TI2
DS2
BI2
SL1
100
D3
D1
SR1
DR
SR2

FIG. 2F

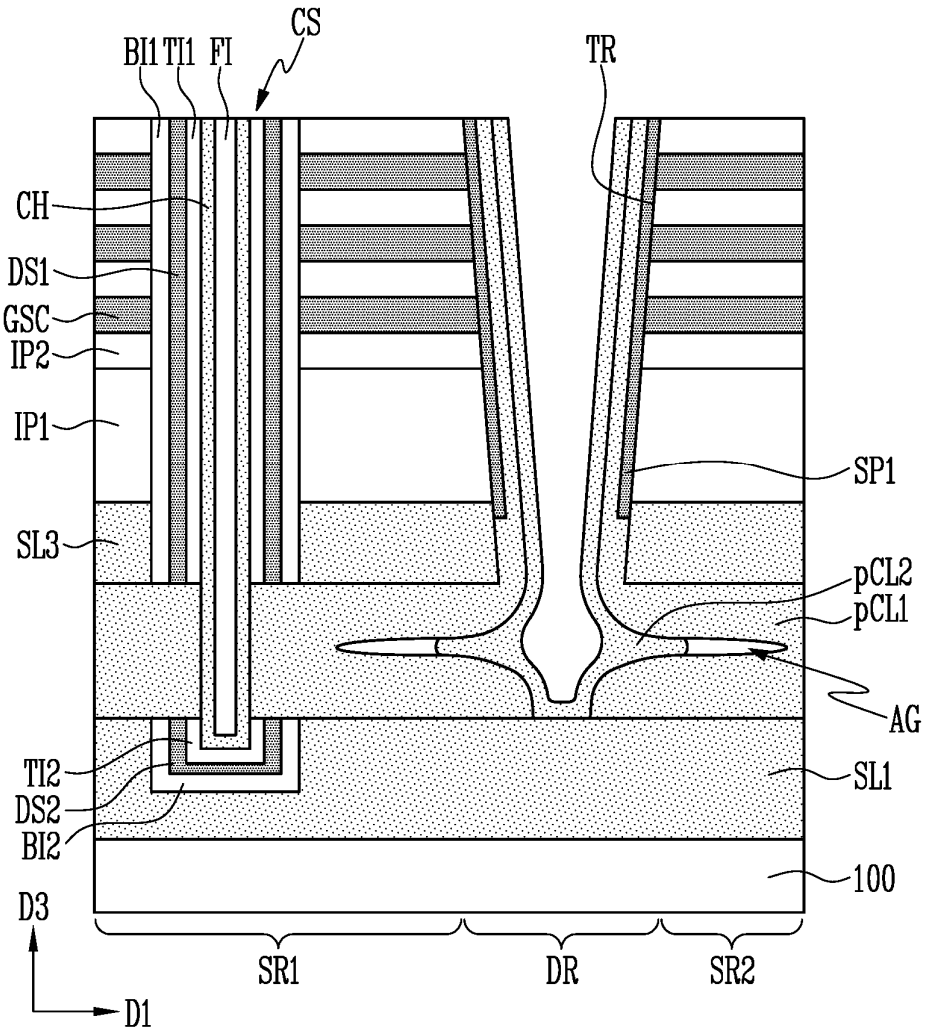

CS
BI1
TI1
FI
TR
CH
DS1
GSC
IP2
IP1
SP1
SL3
pCL2
pCL1
AG
TI2
DS2
BI2
SL1
100
D3
D1
SR1
DR
SR2

FIG. 2G

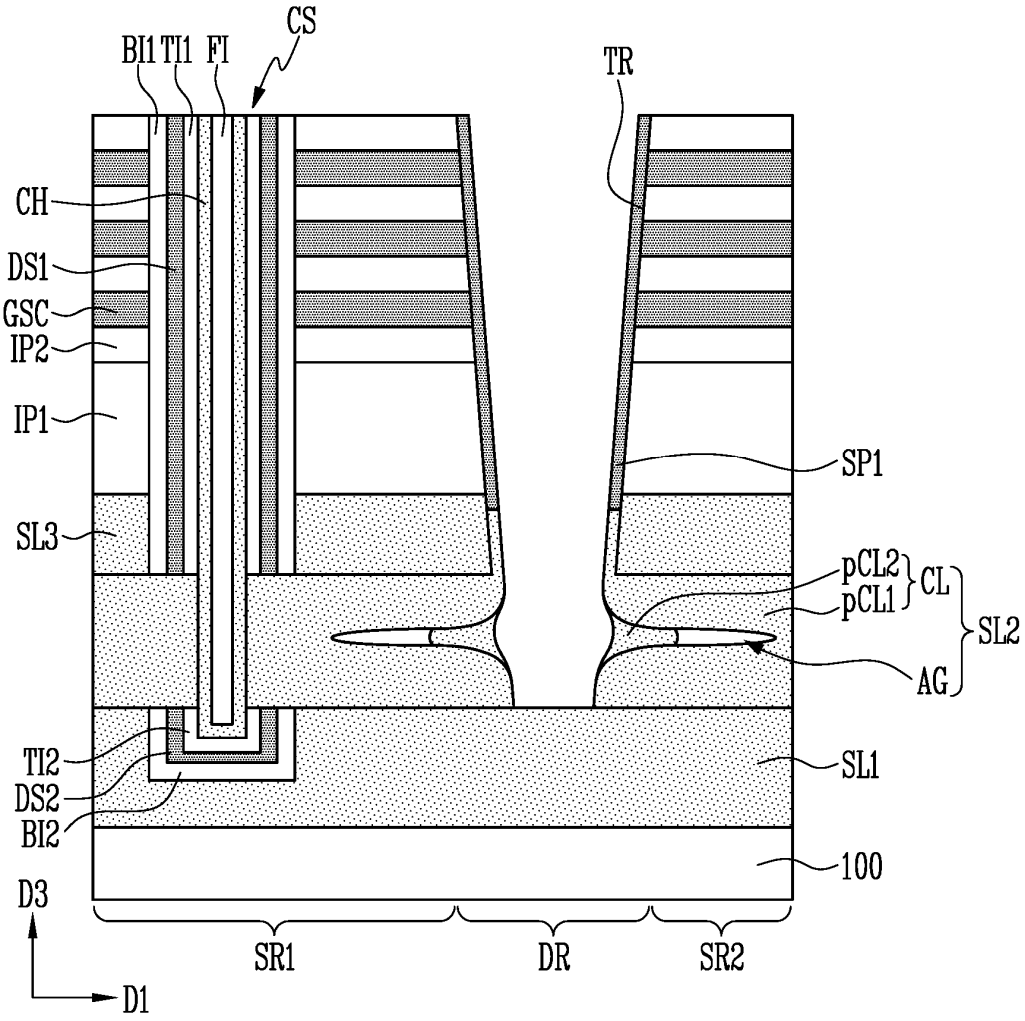

CS
BI1
TI1
FI
TR
CH
DS1
GSC
IP2
IP1
SP1
SL3
pCL2
pCL1
CL
SL2
AG
TI2
DS2
BI2
SL1
100
D3
D1
SR1
DR
SR2

FIG. 2H

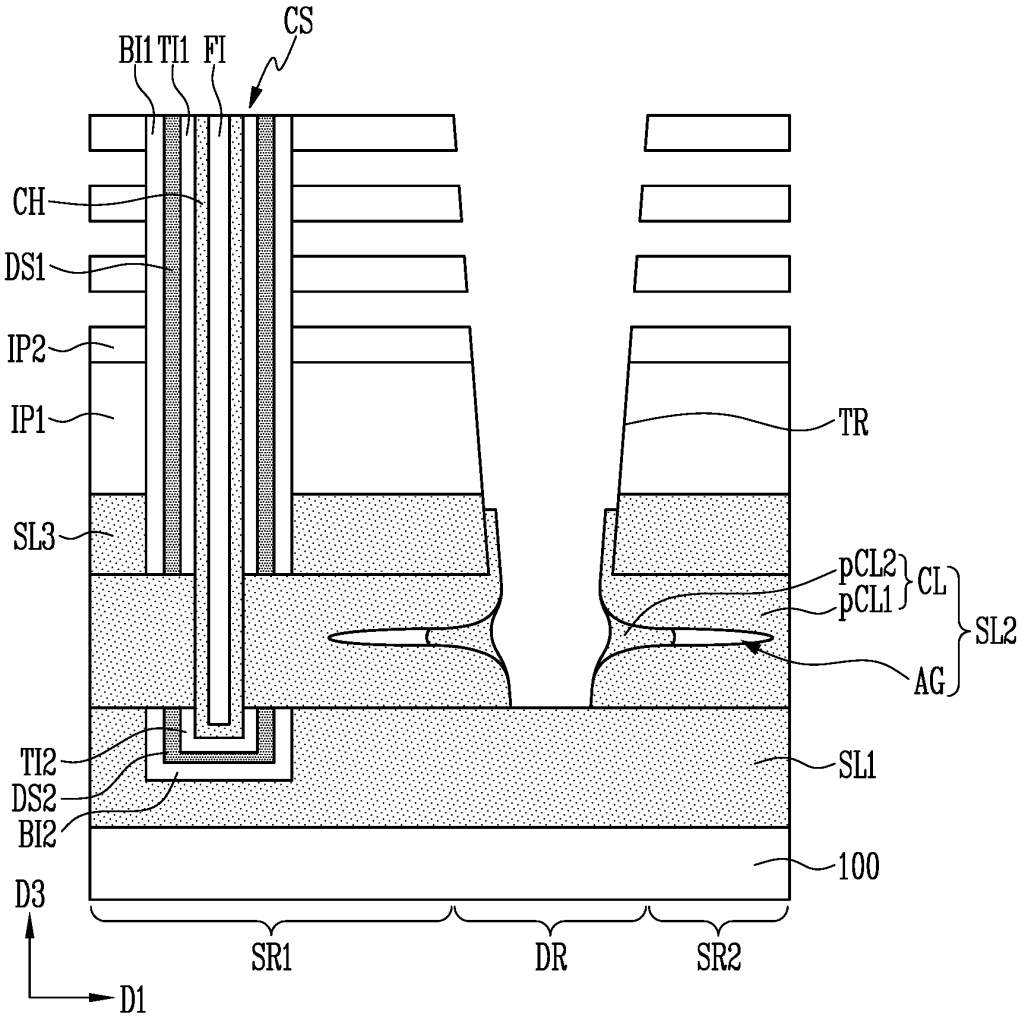

CS
BI1
TI1
FI
CH
DS1
IP2
IP1
SL3
TR
pCL2
pCL1
CL
SL2
AG
TI2
DS2
BI2
SL1
100
D3
D1
SR1
DR
SR2

FIG. 2I

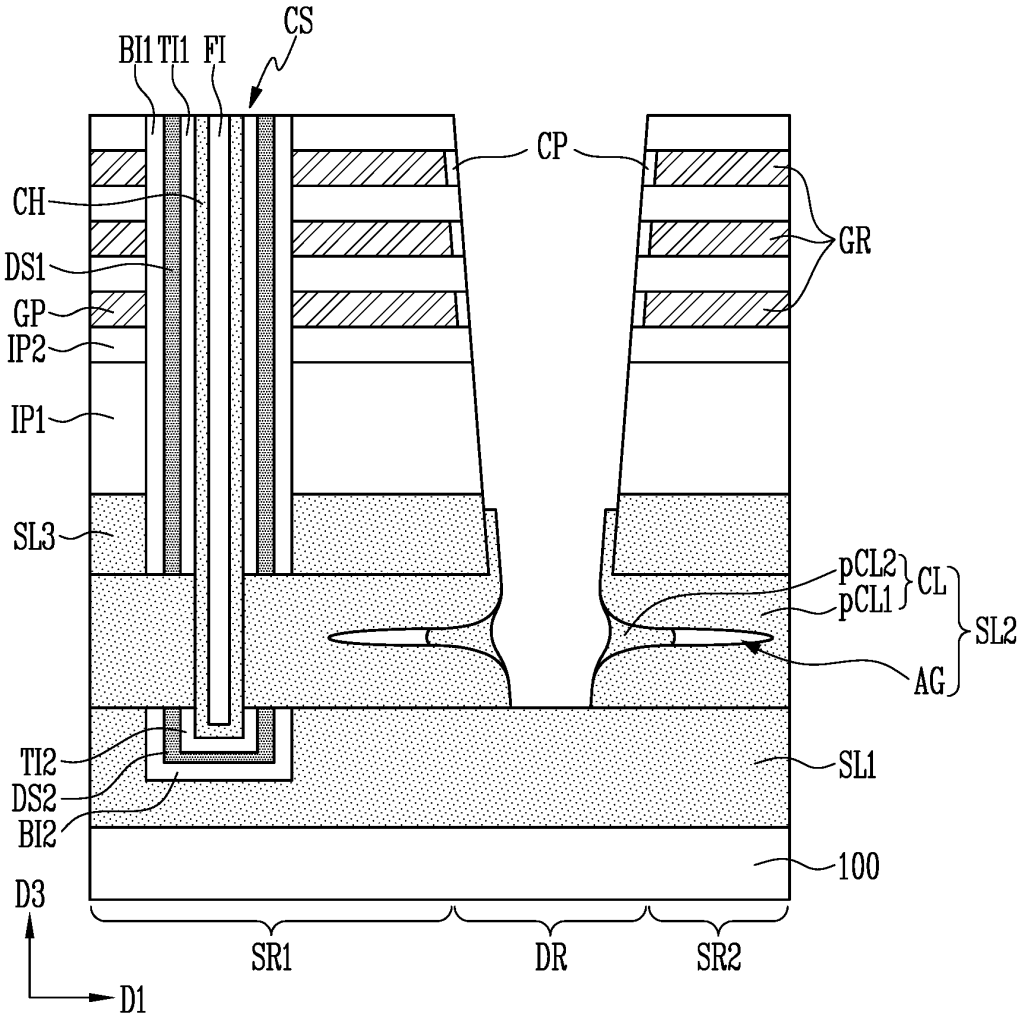

CS
BI1
TI1
FI
CP
CH
GR
DS1
GP
IP2
IP1
SL3
pCL2
pCL1
CL
SL2
AG
TI2
DS2
BI2
SL1
100
D3
D1
SR1
DR
SR2

FIG. 2J

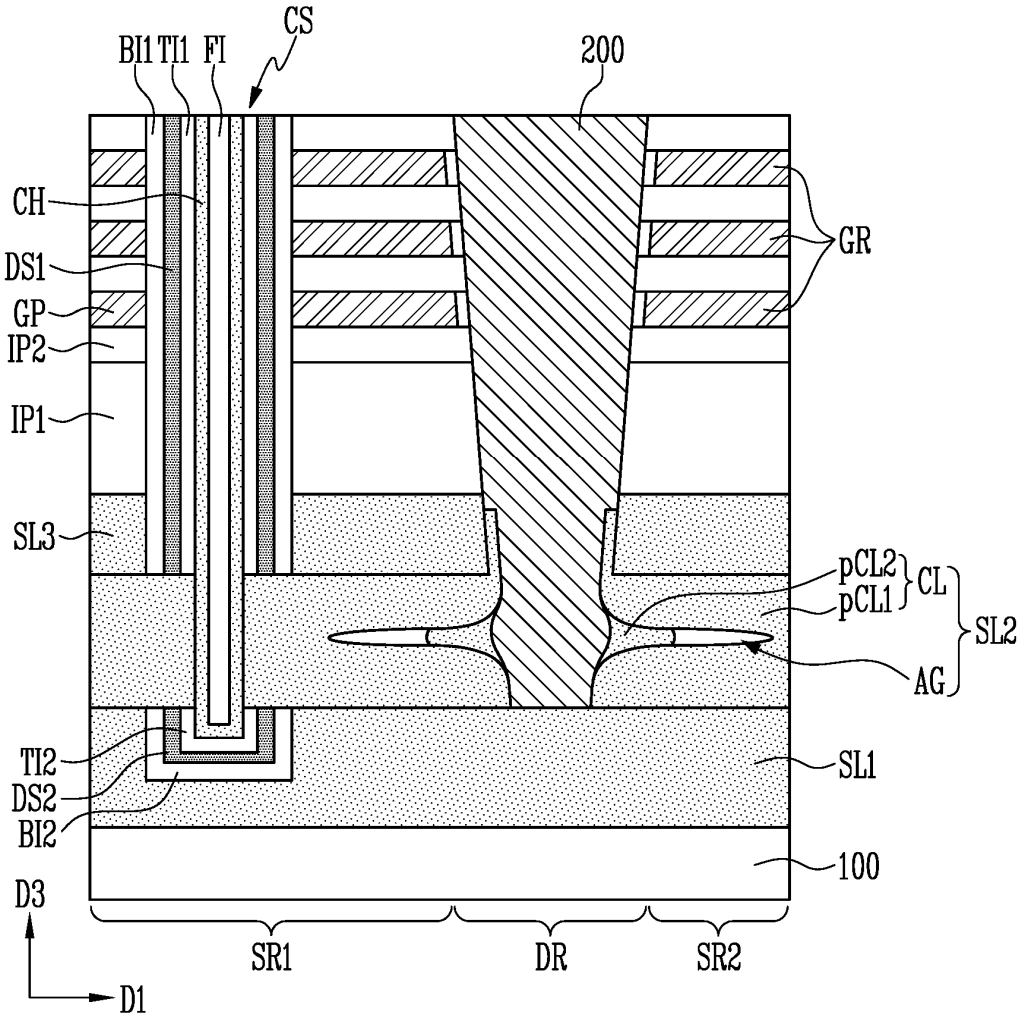

CS
BI1
TI1
FI
200
CH
DS1
GP
IP2
IP1
SL3
GR
pCL2
pCL1
CL
SL2
AG
TI2
DS2
BI2
SL1
100
D3
D1
SR1
DR
SR2

FIG. 3

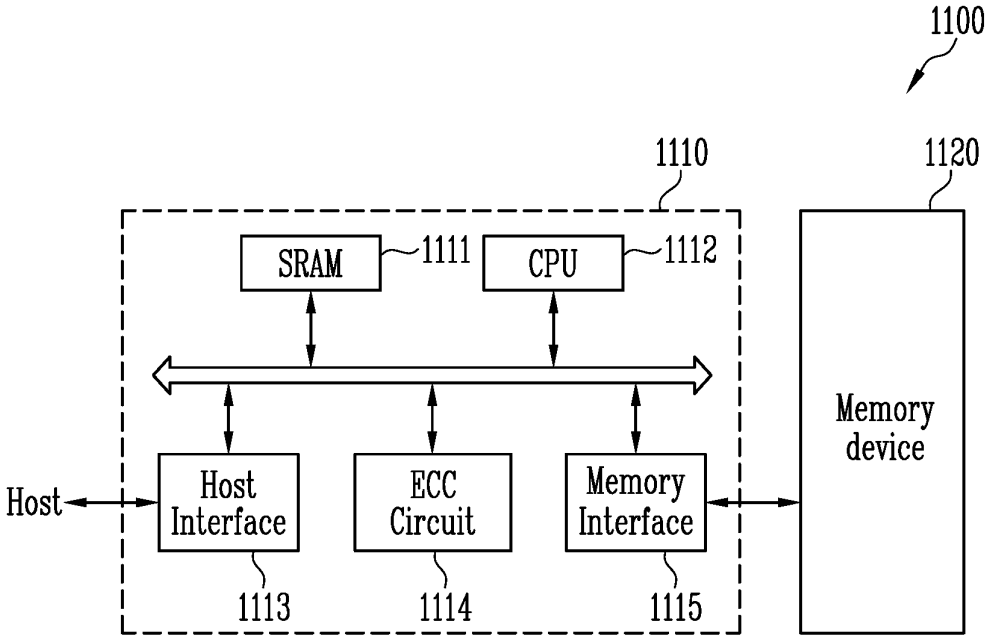
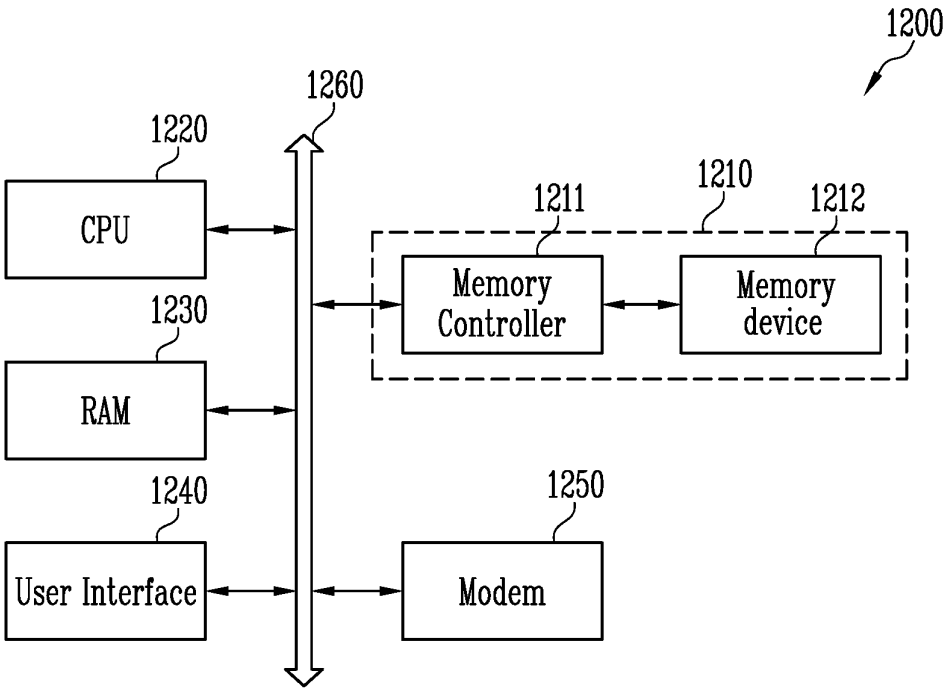

1100
1110
1120
SRAM
1111
CPU
1112
Host
Host Interface
ECC Circuit
Memory Interface
Memory device
1113
1114
1115

FIG. 4


1200
1260
1220
CPU
1211
1210
1212
Memory Controller
Memory device
1230
RAM
1240
1250
User Interface
Modem