LEADFRAME AND SEMICONDUCTOR PACKAGE WITH IMPROVED SOLDER JOINT STRENGTH

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to semiconductor packages and to the leadframes encapsulated therein, and, more particularly, but not by way of limitation, to a leadframe for semiconductor packages which exhibits improved solder joint strength upon being mounted to a motherboard.

HISTORY OF RELATED ART

It is conventional in the electronic industry to encapsulate one or more semiconductor devices, such as integrated circuit dies, or chips, in a semiconductor package. These plastic packages protect a chip from environmental hazards, and provide a method of and apparatus for electrically and mechanically attaching the chip to an intended device. Recently, such semiconductor packages have included metal leadframes for supporting an integrated circuit chip which is bonded to a chip paddle region formed centrally therein. Bond wires which electrically connect pads on the integrated circuit chip to individual leads of the leadframe are then incorporated. A hard plastic encapsulating material, or encapsulant, which covers the bond wire, the integrated circuit chip and other components, forms the exterior of the package. A primary focus in this design is to provide the chip with adequate protection from the external environment in a reliable and effective manner.

As set forth above, the semiconductor package therein described incorporates a leadframe as the central supporting structure of such a package. A portion of the leadframe completely surrounded by the plastic encapsulant is internal to the package. Portions of the leadframe extend internally from the package and are then used to connect the package externally. More information relative to leadframe technology may be found in Chapter 8 of the book Micro Electronics Packaging Handbook, (1989), edited by R. Tummala and E. Rymaszewski. This book is published by Van Nostrand Reinhold, 115 Fifth Avenue, New York, New York.

Once the integrated circuit chips have been produced and encapsulated in semiconductor packages described above, they may be used in a wide variety of electronic appliances. The variety of electronic devices utilizing semiconductor packages has grown dramatically in recent years. These devices include cellular phones, portable computers, etc. Each of these devices typically include a motherboard on which a significant number of such semiconductor packages are secured to provide multiple electronic functions. These electronic appliances are typically manufactured in reduced sizes and at reduced costs, as consumer demand increases. Accordingly, not only are semiconductor chips highly integrated, but also semiconductor packages are highly miniaturized with an increased level of package mounting density.

According to such miniaturization tendencies, semiconductor packages, which transmit electrical signals from semiconductor chips to motherboards and support the semiconductor chips on the motherboards, have been designed to have a small size. By way of example only, such semiconductor packages may have a size on the order of 1x1mm to 10x10 mm. Examples of such semiconductor packages are referred to as MLF (micro leadframe) type semiconductor packages and MLP (micro leadframe package) type semiconductor packages. Both MLF type semiconductor packages and MLP type semiconductor packages are generally manufactured in the same manner.

In further description of the above-described semiconductor package design aspects, reference is now made to Figures 1-3 where a prior art leadframe 100 and semiconductor package 200 are shown. Referring specifically now to Figure 1, a typical prior art leadframe 100 is shown and described. The leadframe 100 has a plate-type frame body 120 with an opening 125 at its center and a chip paddle 110 located within the opening 125 on which a semiconductor chip (not shown) is subsequently mounted. About the perimeter of the chip paddle 110 and extending inwardly from the frame body 120 toward the opening 125, a plurality of internal leads 130 are located radially and spaced at regular intervals. The chip paddle 110 is connected to the frame body 120 by tie bars 150 which may be extended inwardly from the ends of at least two internal leads 130, as shown here, or from the frame body 120 itself. The internal leads 130 extend outward into external leads 135 which are in turn made integral to the frame body 120. Dam bars 140 are provided to separate the internal leads 130 from the external leads 135 during the encapsulation process and to prevent encapsulation material (not shown) from

covering the external leads 135. It is particularly notable that in the prior art leadframe 100, each of the internal leads 130 are all substantially the same length L.

Referring still to Figure 1, the reference numerals 111, 131 and 151 denote half-etched portions of chip paddle 110, the internal leads 130 and the tie bars 150, respectively. These half-etched portions will generally be about half as thick as the remainder of the part. During the subsequent encapsulation process for forming a semiconductor package, encapsulation material flows under these portions of the part to ensure a better seal for the internal components.

Referring now to Figure 2, a semiconductor package 200 using the prior art leadframe 100 is presented. As shown, the semiconductor package 200 includes a semiconductor chip 105 having a plurality of bond pads or input/output pads 106 on its upper surface along its perimeter, and a chip paddle 110 which is bonded to the bottom surface of the semiconductor chip 105 via an adhesive. The chip paddle 110 also features a half-etched portion 111 along its perimeter. A plurality of internal leads 130, each of which has a half-etched portion (not shown) are radially located about the perimeter of the chip paddle 110. The input/output pads 106 of the semiconductor chip 105 are electrically connected to the internal leads 130 via conductive wires 115. As shown here, the semiconductor chip 105, the chip paddle 110, the internal leads 130, and the conductive wires 115, are all sealed within an encapsulation material 10 to create a semiconductor package 200. Referring back to Figure 1, the external portions of the leadframe 100, namely the dam bars 140 and the external leads 135, which are not encapsulated are then trimmed off. The tie bars 150 may also be cut or singulated following encapsulation to completely separate the chip paddle 110 from the frame body 120.

Referring now to Figure 3, note that following encapsulation, the chip paddle 110, the internal leads 130, and the tie bars 150 remain externally exposed on the underside of the semiconductor package 200. The semiconductor package 200 is subsequently placed in electrical communication with the host device by fusing or soldering the exposed bottom surfaces or lands of the internal leads 130 to a motherboard (not shown).

Referring still to Figure 3, the internal leads 130 on the underside of the semiconductor package 200 are regularly spaced at a distance G1 from each other. The internal leads 130 are all of substantially the same length L and are arranged at regular distances G1 to prevent the internal leads 130 which are closest to the corners from

forming a short circuit upon soldering. Typically, the internal leads will have a fixed length L of about 0.4 mm to 0.6mm. Unfortunately, as the other internal leads 130 which are not located near the corners are formed at the same length, the resulting semiconductor package 200 will typically exhibit very poor solder joint strength at the interface with the motherboard. Solder joint strength tends to vary proportionally with the amount of surface area placed in direct contact with the motherboard. Consequently, a lead having a larger surface area should exhibit greater solder joint strength than a lead with a smaller surface area.

BRIEF SUMMARY OF THE INVENTION

The present invention overcomes the shortcomings of the existing designs and satisfies a significant need for a leadframe and semiconductor package with improved solder joint strength at the interface between the semiconductor package and the motherboard to which it is mounted. More particularly, the leadframe and semiconductor package of the present invention address the need for improved solder joint strength by disposing internal leads of different lengths about the perimeter of the chip paddle.

In one embodiment of the present invention, the internal leads which are located centrally along the sides of the chip paddle are the longest in length whereas the shortest internal leads are located closer to the corners of the chip paddle. In another embodiment of the present invention, the internal leads located centrally along the sides of the chip paddle are formed at the shortest length whereas the longest internal leads are located closest to the corners of the chip paddle. In yet a further embodiment of the present invention, there is provided a semiconductor package comprising a semiconductor chip, a chip paddle, conductive wires and internal leads encapsulated within an encapsulation material with the chip paddle and internal leads externally exposed on an undersurface, produced from a leadframe with internal leads of different lengths located about the perimeter of the chip paddle.

In a semiconductor package using a leadframe constructed in accordance with the present invention, the solder joint strength between the semiconductor package and the motherboard can be improved by increasing the length or surface area of the internal leads which are brought into direct contact with the motherboard during soldering. Thus, in one embodiment, the leads are longer along the sides of the chip paddle to provide added solder joint strength to the entire chip package while reducing the likelihood of

shorting across the leads near the corners. However, in an alternative embodiment that is well suited to larger package designs, the leads are longer near the corners of the chip paddle to ensure greater solder joint strength in an area of known stress concentration.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the leadframe and semiconductor package of the present invention may be obtained by reference to the following detailed description when taking in conjunction with the accompanying drawings wherein:

Figure 1 is a top plan view of a prior art leadframe structure having internal leads of substantially the same length and equal spacing;

Figure 2 is a side view of a prior art semiconductor package having a semiconductor chip attached to the leadframe of Figure 1;

Figure 3 is a bottom view of a prior art semiconductor package having exposed exterior surfaces or lands on the underside of the chip paddle and internal leads for solder mounting to a motherboard;

Figure 4 is a top plan view of a leadframe structure according to one embodiment of the present invention having internal leads of at least two different lengths;

Figure 5 is a side view of a semiconductor package having a semiconductor chip attached to the leadframe of Figure 4 in accordance with one embodiment of the present invention;

Figure 6 is a bottom view of the semiconductor package of Figure 5 having exposed external surfaces or lands suitable for solder mounting to a motherboard; and

Figure 7 is a bottom view of a semiconductor package using an alternative leadframe design in accordance with another embodiment of the present invention having exposed exterior surfaces or lands for solder mounting to a motherboard.

DETAILED DESCRIPTION OF THE INVENTION

The various embodiments of the present invention will now be described more fully hereinafter with reference to the accompanying drawings.

Referring now to Figure 4, a top plan view of a leadframe 500 in accordance with one embodiment of the present invention and having internal leads of at least two

different lengths is shown. The leadframe 500 has a plate-type frame body 520 with an opening 525 at its center and a chip paddle 510 located within the opening 525 on which a semiconductor chip (not shown) is subsequently mounted. About the perimeter of the chip paddle 510 and extending inwardly from the frame body 520 toward the opening 525, a plurality of internal leads 530 are located radially and spaced at regular intervals. The chip paddle 510 is connected to the frame body 520 by tie bars 550 which extend inwardly from the ends of two internal leads 530, as shown here, or from the frame body itself 520. The internal leads 530 extend outward into external leads 535 which are in turn made integral to the frame body 520. Dam bars 540 are provided to separate the internal leads 530 from the external leads 535 during the encapsulation process and to prevent encapsulation material (not shown) from covering the external leads 535. It is particularly notable that in the leadframe 500 according to one embodiment of the present invention, the internal leads 530 are of at least two different lengths L1 and L2.

Referring still to Figure 4, the reference numerals 511, 531 and 551 denote half-etched portions of chip paddle 510, the internal leads 530 and the tie bars 550, respectively. These half-etched portions will generally be about half as thick as the remainder of the part. During the subsequent encapsulation process for forming a semiconductor package, encapsulation material flows under these portions of the part to ensure a better seal for the internal components.

Also, it is to be understood that the entire leadframe 500 including the frame body 520, chip paddle 510, internal leads 530, external leads 535, dam bars 540, and other structures may be formed of a single piece of material. Typically, this material will be a good electrical conductor such as aluminum, copper, or other metals and alloys. The leadframe may also be formed of one material and plated (wholly or partially) with another. Materials used to plate the leadframe include, but are not limited to, tin lead, tin, gold, silver, nickel, palladium, tin bismuth, or other similar materials know in the art. The leadframe 500 may be produced by either stamping or etching processes as known in the art.

Referring still to Figure 4, it is shown that the internal leads 530a through 530e are not uniform in length. In contrast to conventional prior art leadframe designs, the leadframe 500 formed in accordance with the present invention features internal leads 530 having at least two different lengths. As shown here, the three internal leads 530a, 530b, and 530c, which are located near the center 510a of one side of the chip paddle 510, are

longer than the internal leads 530d and 530e which are closest to the corners 510b and 510c of the chip paddle 510. This is also true of the internal leads 530 which are located about the other three sides of the chip paddle 510.

Alternatively, although not shown in Figure 4, the internal leads 530a, 530b and 530c which are located nearest the center 510a of one side of the chip paddle 510 may be made shorter than those 530d and 530e which are closest to the corner areas 510b and 510c of the chip paddle 510. This alternative structure is preferably applied to large size leadframes used for MLF packages. In packages having large sized leadframes, the weakest solder joint strength usually occurs in the corner regions of the package body, and short circuiting between the internal leads is less likely than in small sized leadframes.

While the internal leads 530 shown and described in these two embodiments are of two distinct lengths L1 and L2, it is to be understood that the internal leads 530 may be of several different lengths or widths, and are limited by the space provided between the chip paddle 510 and the frame body 520, and the need for sufficient lateral spacing between internal leads 530 to avoid short circuiting. The leadframe 500 according to the present invention addresses solder joint strength problems by placing more surface area of the internal leads 530 in direct contact with the motherboard (not shown) on which the semiconductor package is soldered. Longer or wider internal leads 530 will have greater surface area and accordingly have higher solder joint strength. However, as it is difficult to adjust the lateral spacing between internal leads 530 without short circuiting, producing a leadframe with different lengths of internal leads 530 appears to be the most direct solution to the solder joint strength problems of prior art leadframes.

Referring now to Figure 5, a semiconductor package 600 is depicted using a leadframe 500 in accordance with one embodiment of the present invention. As shown, the semiconductor package 600 includes a semiconductor chip 505 having a plurality of bond pads 506 on its upper surface along its perimeter, and a chip paddle 510 which is bonded to the bottom surface of the semiconductor chip 505 via an adhesive. The chip paddle 510 also features a half-etched portion 511 along its perimeter. A plurality of internal leads 530, each of which has a half-etched portion (not shown) are radially located about the perimeter of the chip paddle 510. The top of each one of the plurality of internal leads 530 may be plated with silver plate or gold plate for better electrical conductivity. The bond pads 506 of the semiconductor chip 505 are electrically connected

to the internal leads 530 via conductive wires 515. As shown here, the semiconductor chip 505, the chip paddle 510, the internal leads 530, and the conductive wires 515, are all sealed within an encapsulation material 10 to create a semiconductor package 600. Encapsulation material 10 can be thermoplastics or thermoset resins, with thermoset resins including silicones, phenolics, and epoxies. Referring back to Figure 4, the external portions of the leadframe 500, namely the dam bars 540 and the external leads 535, which are not encapsulated are then trimmed off. The tie bars (not shown) may also be cut or singulated following encapsulation to completely separate the chip paddle 510 from the frame body 520.

Referring now to Figure 6, note that following encapsulation, the chip paddle 510, the internal leads 530, and the tie bars 550 remain externally exposed on the underside of the semiconductor package 600. To minimize corrosion, the externally exposed portions of the chip paddle 510, internal leads 530, and the tie bars 550 may be plated with tin lead, tin, gold, nickel palladium, tin bismuth, or other corrosion-minimizing materials known in the art. The semiconductor package 600 is subsequently placed in electrical communication with the host device by fusing or soldering the exposed bottom surfaces or lands of the internal leads 530 to a motherboard (not shown).

Referring still to Figure 6, a bottom view illustrates the underside of the semiconductor package 600 featuring internal leads 530a - 530e which are of two different lengths L1 and L2. As shown here, the internal leads proximate to any one side of the chip paddle, for example 530a - 530e, may be divided into at least two subgroups referred to as outer leads 530d and 530e which are closest to the corners and inner leads 530a, 530b and 530c which are between the outer leads 530d and 530e and centrally located along the side 510a of the chip paddle 510. In this embodiment, the outer leads have a first length L1 and are shorter than the inner leads which have a length L2. By way of example only, L1 may be as short as 0.25 mm and L2 may be as long as 0.90 mm. This is true of the internal leads 530 proximate the other three sides of the chip paddle 510 as well.

Referring now to Figure 7, an alternative leadframe 700 included in the semiconductor package 800 featuring internal leads 730 which are of at least two different lengths L1 and L2 is shown. The leadframe 700 has a plate-type frame body 720. The chip paddle 710 is connected to the frame body 720 by tie bars 750 which extend inwardly from the ends of two of the internal leads 730. The internal leads 730

proximate to any one side of the chip paddle 710, for example the internal leads 730, may again be divided into at least two subgroups referred to as outer leads 730d and 730e which are closest to the corners 710b and 710c and inner leads 730a, 730b and 730c which are between the outer leads 730d and 730e and centrally located along the side 710a of the chip paddle 710. In this alternative embodiment, the outer leads have a first length L1 and are longer than the inner leads which have a length L2 or less (e.g. 730b). By way of example only, L1 may be as long as 0.90 mm and L2 may be as short as 0.25 mm. This is true of the internal leads 730 proximate the other three sides of the chip paddle 710 as well. As noted earlier in discussing leadframe design, this structure is preferably applied in large size MLF packages to address solder joint strength problems which may appear in the corner regions of the package body. As noted earlier, the embodiment set forth in Figure 7 is best suited to large size applications as there is a reduced tendency for short circuiting in the corners in comparison with small size applications. Note also that MLF packages of 10x10 mm size could be considered relatively large, but that leadframes and packages could also be produced in accordance with the present invention in other industry standard sizes (e.g. 20x20, 24x24, 28x28, 32x32 and 40x40 mm).

The following applications are all being filed on the same date as the present application and all are incorporated by reference as if wholly rewritten entirely herein, including any additional matter incorporated by reference therein:

Attorney Docket No.	Title of Application	First Named Inventor
09/687,787	Improved Thin and Heat Radiant Semiconductor Package and Method for Manufacturing	Jae Hun Ku
09/687,331	Leadframe for Semiconductor Package and Mold for Molding the Same	Young Suk Chung
09/687,532	Method for Making a Semiconductor Package Having Improved Defect Testing and Increased Production Yield	Tae Heon Lee
09/687,876	Near Chip Size Semiconductor Package	Sean Timothy Crowley
09/687,536	End Grid Array Semiconductor Package	Jae Hun Ku
09/687,585	Semiconductor Package Having Reduced Thickness	Tae Heon Lee

09/687,541	Semiconductor Package Leadframe Assembly and Method of Manufacture	Young Suk Chung
09/687,049	Improved Method for Making Semiconductor Packages	Young Suk Chung

It is thus believed that the operation and construction of the present invention will be apparent from the foregoing description of the preferred embodiments. While the leadframe and semiconductor package shown are described as being preferred, it will be obvious to a person of ordinary skill in the art that various changes and modifications may be made therein without departing from the spirit and the scope of the invention, as defined in the following claims. Therefore, the spirit and scope of the appended claims should not be limited to the description of the preferred embodiments contained herein.

This invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein. Rather, the embodiments are provided so that this disclosure is thorough and complete, and fully conveys the scope of the invention to those skilled in the art.

Claims

1. A semiconductor package, comprising:
a leadframe having:
a chip paddle defining opposed top and bottom surfaces and a plurality of sides and corners; and
a plurality of leads extending along at least one of the sides of the chip paddle in spaced relation thereto, each of the leads defining opposed top and bottom surfaces, the bottom surfaces of the leads being of at least two difference lengths;
a semiconductor chip mounted to the top surface of the chip paddle and electrically connected to at least one of the leads; and
an encapsulation material covering the leadframe and the semiconductor chip such that the bottom surfaces of the leads, which are of at least two different lengths, are exposed in the encapsulation material.

2. The semiconductor package of Claim 1 wherein the leads are segregated into multiple sets which extend long respective ones of the sides of the chip paddle in spaced relation thereto.

3. The semiconductor package of Claim 2 wherein the leads of each set include at least two outer leads and at least one inner lead disposed between the outer leads, the bottom surfaces of the outer leads each being of a first length and the bottom surface of the inner lead being of a second length which is unequal to the first length.

4. The semiconductor package of Claim 3 wherein the first length of the bottom surface of each of the outer leads exceeds the second length of the bottom surface of the inner lead.

5. The semiconductor package of Claim 3 wherein the first length of the bottom surface of each of the outer leads is less than the second length of the bottom surface of the inner lead.

6. The semiconductor package of Claim 1 wherein the bottom surface of the chip paddle is exposed in the encapsulation material.

7. The semiconductor package of Claim 6 wherein:

the encapsulation material defines a generally planar bottom surface;

the bottom surface of the chip paddle is generally planar and substantially flush with the bottom surface of the encapsulation material; and

the bottom surfaces of the leads are each generally planar and substantially flush with the bottom surface of the encapsulation material.

8. The semiconductor package of Claim 1 wherein the leadframe further comprises at least one tie bar attached to and extending from at least one of the corners of the chip paddle, the tie bar defining opposed top and bottom surfaces.

9. The semiconductor package of Claim 8 wherein the bottom surface of the at least one tie bar is exposed in the encapsulation material.

10. A semiconductor package comprising:

a plurality of leads, each of the leads defining opposed top and bottom surfaces, the bottom surfaces of the leads being of at least two different lengths;

a semiconductor chip defining multiple sides and electrically connected to at least one of the leads; and

an encapsulation material covering the leads and the semiconductor chip such that the bottom surfaces of the leads, which are of at least two different lengths, are exposed in the encapsulation material.

11. The semiconductor package of Claim 10 wherein the leads are segregated into multiple sets which extend along respective ones of the sides of the semiconductor chip.

12. The semiconductor package of Claim 11 wherein the leads of each set include at least two outer leads and at least one inner lead disposed between the outer leads, the bottom surface of the outer leads each being of a first length and the bottom surface of the inner lead being of a second length which is unequal to the first length.

13. The semiconductor package of Claim 12 wherein the first length of the bottom surface of each of the outer leads exceeds the second length of the bottom surface of the inner lead.

14. The semiconductor package of Claim 12 wherein the first length of the bottom surface of each of the outer leads is less than the second length of the bottom surface of the inner lead.

15. The semiconductor package of Claim 10 wherein:

the encapsulation material defines a generally planar bottom surface; and

the bottom surfaces of the leads are each generally planar and substantially flush with the bottom surface of the encapsulation material.

16. In a semiconductor package comprising a plurality of leads having bottom surfaces which are exposed in an encapsulation material and a semiconductor chip which is covered by the encapsulation material and electrically connected to at least one of the leads, the improvement comprising:

configuring the leads such that the bottom surfaces thereof which are exposed in the encapsulation material are of at least two different lengths.

17. The semiconductor package of Claim 16 wherein the semiconductor chip defines multiple sides, and the leads are segregated into multiple sets which extend along respective ones of the sides of the semiconductor chip.

18. The semiconductor package of Claim 17 wherein the leads of each set include at least two outer leads and at least one inner lead disposed between the outer leads, the bottom surfaces of the outer leads each being of a first length and the bottom surface of the inner lead being of a second length which is unequal to the first length.

19. The semiconductor package of Claim 18 wherein the first length of the bottom surface of each of the outer leads exceeds the second length of the bottom surface of the inner lead.

20. The semiconductor package of Claim 18 wherein the first length of the bottom surface of each of the outer leads is less than the second length of the bottom surface of the inner lead.