CLAIMS

1. A test circuit, comprising:

an input terminal, a processing circuit and an output terminal;

the input terminal being configured to receive an input signal, the input signal comprising a test command to instruct to test a target circuit module and an address of the target circuit module;

the processing circuit being configured to determine a test mode signal according to the test command and the address of the target circuit module, the test mode signal carrying a test type, the test mode signal being used to trigger the target circuit module to perform a test corresponding to the test type; and

the output terminal being configured to send the test mode signal to the target circuit module according to the address of the target circuit module;

wherein the processing circuit comprises:

a first address latch, a command logic circuit and a second address latch;

the first address latch being configured to receive a first internal address, and output a first internal delay address;

the command logic circuit being configured to receive the test command and a second internal address, and output a test mode command; and

the second address latch being configured to receive a third internal address and the test mode command, and output a third internal delay address;

wherein the processing circuit further comprises:

a control logic circuit, a test decoding circuit and a slave latch;

the control logic circuit being configured to receive the first internal delay address and the test mode command, and output a test mode enable active signal and a test mode enable slave signal;

the test decoding circuit being configured to receive the first internal delay address and the third internal delay address, and output a decoding signal; and

the slave latch being configured to receive the third internal address and the test mode enable slave signal, and output a slave address.

2. The test circuit according to claim 1, wherein the processing circuit further comprises:

a self-test circuit, being configured to receive the test mode enable active signal, the slave address and the decoding signal, and output the test mode signal to the target circuit module.

3. The test circuit according to claim 2, wherein the command logic circuit is configured to:

generate the test mode command according to the test command when a value of the second internal address is a preset value.

4. The test circuit according to claim 2 or 3, wherein the control logic circuit is configured to:

when a value of the first internal delay address is a first value, perform a logical operation on the first value with the test mode command to generate the test mode enable active signal; and

when the value of the first internal delay address is a second value, perform a logic operation on the second value with the test mode command to generate the test mode enable slave signal.

5. The test circuit according to any one of claims 2 to 4, wherein the test decoding circuit comprises a plurality of decoders.

6. The test circuit according to claim 5, wherein the decoder comprises a 3-8 decoder.

7. The test circuit according to any one of claims 2 to 6, wherein the control logic circuit comprises a first NAND gate, a first inverter, a second NAND gate, a second inverter, a third NAND gate, and a third inverter;

an output terminal of the first NAND gate is connected to an input terminal of the first inverter, an output terminal of the second NAND gate is connected to an input terminal of the second inverter, and an output terminal of the third NAND gate is connected to an input terminal of the third inverter;

the first NAND gate is configured to receive the first internal delay address, and output a first signal;

the first inverter is configured to receive the first signal, and output a second signal;

the second NAND gate is configured to receive the first signal and the test mode command, and output a third signal;

the second inverter is configured to receive the third signal, and output the test mode enable active signal;

the third NAND gate is configured to receive the second signal and the test mode command, and output a fourth signal; and

the third inverter is configured to receive the fourth signal, and output the test mode enable slave signal.

8. The test circuit according to any one of claims 2 to 7, wherein the self-test circuit comprises a first test sub-circuit, the first test sub-circuit comprises a first logic control sub-circuit and a first latch group, the first logic control sub-circuit is connected to the first latch group.

9. The test circuit according to claim 8, wherein an input terminal of the first logic control sub-circuit is connected to an output terminal of the control logic circuit, an output terminal of the test decoding circuit and an output terminal of the slave latch; and

the first logic control sub-circuit is configured to perform a logic operation according to the test mode enable active signal and the decoding signal, to generate a clock signal and output the clock signal to the first latch group.

10. The test circuit according to claim 9, wherein the first latch group is configured to receive the slave address and the clock signal, determine the test mode signal according to the slave address and the clock signal, and output the test mode signal to the target circuit module.

11. The test circuit according to any one of claims 8 to 10, wherein the first logic control sub-circuit comprises a first P-type transistor, a first N-type transistor, a second N-type transistor, a third N-type transistor, and a fourth N-type transistor;

a control terminal of the first P-type transistor is connected to an output terminal of the control logic circuit, a first terminal of the first P-type transistor is connected to a power supply terminal, and a second terminal of the first P-type transistor is connected to an input terminal of the first latch group and a first terminal of the first N-type transistor;

a control terminal of the first N-type transistor, a control terminal of the second N-type transistor, and a control terminal of the third N-type transistor are all connected to an output terminal of the test decoding circuit;

a second terminal of the first N-type transistor is connected to a first terminal of the second N-type transistor, a second terminal of the second N-type transistor is connected to a first terminal of the third N-type transistor, and a second terminal of the third N-type transistor is connected to a first terminal of the fourth N-type transistor;

a control terminal of the fourth N-type transistor is connected to the output terminal of the control logic circuit, the first terminal of the fourth N-type transistor is connected to the second terminal of the third N-type transistor, and a second terminal of the fourth N-type transistor is connected to a ground terminal.

12. The test circuit according to any one of claims 2 to 11, wherein the first internal address is 2 bits, the second internal address is 1 bit, and the third internal address is 7 bits.

13. A memory, comprising a control circuit, at least one circuit module, and the test circuit according to any one of claims 1 to 12;

the control circuit being configured to send the input signal to the test circuit; and

the test circuit being configured to receive the input signal, and send the test mode signal to one of the at least one circuit module according to the input signal.