

Device and method for producing a semiconductor wafer with reduced autodoping

Technical Area

The invention relates to a layer deposition arrangement for an epi-reactor for producing a semiconductor wafer having at least one epitaxial layer. The invention furthermore relates to a method for producing a semiconductor wafer comprising depositing at least one epitaxial layer using the layer deposition arrangement. The invention finally relates to a semiconductor wafer comprising a doped substrate wafer and at least one epitaxial layer deposited thereon.

Prior Art and Technical Object

The problem is known in conjunction with epi-coating processes of (highly) doped substrate wafers in epi-reactors that during the deposition of an epitaxial layer on a (highly) doped substrate wafer (for example, boron-doped substrate wafer) to produce a semiconductor wafer, dopants from the substrate wafer, which are deposited in a hole susceptor unit in the layer deposition arrangement, initially enter the deposition gas (in an uncontrolled manner) from the rear side of the substrate wafer (i.e. the side of the substrate wafer facing toward a hole susceptor unit within the epi-reactor) during the epi-deposition mode via the gas phase and then are finally predominantly incorporated into the epitaxial layer in the edge area of the front side of the substrate wafer (i.e. the side of the substrate wafer on which an epitaxial layer is deposited during the epi-deposition mode). This undesired phenomenon is known under the term "autodoping", which results in a radial variation of the specific resistance along the deposited epitaxial layer of the semiconductor wafer, which is typically specified by the characteristic variable "radial resistance variation" (RRV). In this case, the RRV value [%] is determined from measured individual R values resulting from a specifiable number of measurement points located on a measurement grid (cross-shaped measurement grid) on the epitaxial layer of the semiconductor wafer according to the equation $RRV [\%] = (R_{\max} - R_{\min}) / (R_{\max} + R_{\min})$ (in particular according to Semi Standards M62-0317 (Specification for Silicon Epitaxial Wafers), 2017).

To improve the RRV value, initially providing the (highly) doped substrate wafer with a LTO (Low Thermal Oxide) layer on the rear side of the semiconductor wafer (i.e. the side of the substrate wafer facing toward a hole susceptor unit within the epi-reactor) in a sealed manner is known from the prior art. The substrate wafer including applied LTO layer is then arranged in an epi-reactor within a hole susceptor unit and subjected to the epi-deposition mode. This LTO

layer acts as a dopant diffusion barrier layer and has the purpose of preventing as much as possible diffusion of the dopants from the substrate wafer into the (at least one) epitaxial layer during the epi-coating process. By providing such an oxide layer, comparatively lower radial specific resistances (RRV) are achieved after the epitaxial deposition, however, such an oxide layer remaining on a produced semiconductor wafer as the end product can be disadvantageous. Even after manual and/or chemical postprocessing (for example, by cleaning using HF component) to remove this layer – in particular due to the circumstance that an inhomogeneous, epitaxial growth takes place at the edge of the oxide layer during the epi-process – defects exist as a residue on the semiconductor wafer in an undesired manner, which are detectable using an inspection device, in particular an EBI unit, by means of scattered light measurement as light point defects (for example by means of an EBI unit of the company Nanophotonics AG having a mode of operation as described in paragraph 52 of document DE102009011622 A1). These defects characteristically occur in the form of a substantially annularly formed defect ring having high defect density or defect number in the surroundings of the edge area of the semiconductor wafer.

The present invention is therefore based on the objective technical object of producing a semiconductor wafer having an epitaxial layer in an epi-deposition mode by means of a compact hole susceptor unit of a layer deposition arrangement in a simple manner from a (highly) doped substrate wafer, which does not have the above-mentioned disadvantages or at least has them to a lesser extent and which in particular has a lower RRV value in combination with a comparatively defect-reduced surface of the free substrate wafer surface of the final semiconductor wafer.

The object is achieved according to the first aspect of the present invention by providing a layer deposition arrangement having a susceptor unit according to the features in claim 1, is furthermore achieved according to a second aspect by the method for producing a semiconductor wafer using the layer deposition arrangement comprising depositing at least one epitaxial layer according to the features as claimed in claim 7, and is finally achieved according to a third aspect by providing a semiconductor wafer according to the features as claimed in claim 10. Preferred embodiments are the subject matter of the dependent claims.

The invention is based in this case on the technical teaching that a semiconductor wafer having comparatively lower RRV (i.e. low RRV value) of the deposited epitaxial layer of the semiconductor wafer having a comparatively defect-reduced second wafer side of the doped substrate wafer is obtained in a simple manner if (i) the layer deposition arrangement for

producing the semiconductor wafer having a correspondingly designed hole susceptor unit is designed to be rotatable in relation to the preheat ring (and these are spaced apart from one another via a correspondingly designed gap unit), so that a reliable rotation of the hole susceptor unit in relation to the preheat ring and therefore a continuous and uniform deposition of the epitaxial layer is ensured during the epi-deposition mode and (ii) to combat the occurrence of the “autodoping” phenomenon in the semiconductor wafer to be produced during the epi-deposition mode, the layer deposition arrangement having its hole susceptor unit is designed in such a way that a reliable physical barrier unit against undesired flows is ensured during the epi-deposition mode in the entirety between the upper side and the lower side of the layer deposition arrangement.

General Description of the Invention

According to a first aspect, the invention therefore relates to a layer deposition arrangement for an epi-reactor for producing a semiconductor wafer having at least one epitaxial layer, wherein the layer deposition arrangement comprises a hole susceptor unit and a preheat ring, wherein the hole susceptor unit has a hole susceptor unit upper side and a hole susceptor unit lower side, and wherein, at least during an epi-deposition mode,

- the preheat ring surrounds the hole susceptor unit at a distance at least in some sections via a gap unit, in particular in the form of an air gap ring, wherein the hole susceptor unit is designed to rotate at a specifiable rotational velocity around a vertical axis, in particular a vertical center axis, of the hole susceptor unit in relation to the preheat ring, and wherein
- the layer deposition arrangement furthermore comprises at least one sealing ring unit, which is arranged on the layer deposition arrangement in such a way and is designed for the purpose of providing a physical barrier unit between the hole susceptor unit upper side and the hole susceptor unit lower side on the gap unit.

The term “between” in the meaning of the invention does not represent a directional restriction for the effect of the physical barrier (unit). Due to the design according to the invention of a layer deposition arrangement (in particular due to the selected relative arrangement of the components of the layer deposition arrangement or arrangement of the gap unit in relation to one another) and in particular due to the special design of the components of the sealing ring unit with respect to the gap unit during an epi-deposition mode of the layer deposition arrangement, an exchange of at least one of the deposition process gases and dopants via the

gap unit between the hole susceptor unit lower side and the hole susceptor unit upper side is reduced, in particular substantially avoided.

However, it is particularly advantageous that a flow of deposition process gases via the gap unit from the direction of the hole susceptor unit upper side in the direction of the hole susceptor unit lower side and a flow of dopant via the gap unit from the direction of the hole susceptor unit lower side in the direction of the hole susceptor unit upper side can be reduced, preferably substantially avoided.

The sealing ring unit can be arranged in principle for this purpose at any arbitrary point on the layer deposition arrangement, as long as the described function for creating a barrier effect or a physical barrier (unit) between the upper side and the lower side of the layer deposition arrangement is ensured in order to provide the contribution of reducing or, in the ideal case, avoiding the “autodoping” effect. In particularly advantageous variants of the layer deposition arrangement, the sealing ring unit is arranged here on the hole susceptor unit, in particular on the hole susceptor unit lower side or the hole susceptor unit upper side, and is arranged in relation to the preheat ring so that a flow of deposition process gases via the gap unit from the direction of the hole susceptor unit upper side into the hole susceptor unit lower side is reduced, preferably substantially avoided, and that a flow of dopant via the gap unit from the direction of the hole susceptor unit lower side into the hole susceptor unit upper side is reduced, preferably substantially avoided. Alternatively thereto, it can be provided that the sealing ring unit is arranged on the preheat ring, in particular on the side of the layer deposition arrangement facing toward the hole susceptor unit lower side or the hole susceptor unit upper side and is arranged in relation to the hole susceptor unit in such a way that a flow of deposition process gases via the gap unit from the direction of the hole susceptor unit upper side into the hole susceptor unit lower side is substantially reduced, preferably is substantially avoided, and that a flow of dopant via the gap unit from the direction of the hole susceptor unit lower side into the hole susceptor unit upper side is reduced, preferably is substantially avoided.

Additionally or alternatively, the sealing ring unit can be arranged at a point on the side of the layer deposition arrangement facing toward the hole susceptor unit lower side, in particular can be arranged directly on the hole susceptor unit lower side. In an alternative variant thereto, the sealing ring unit can be arranged at a point on the side of the layer deposition arrangement facing toward the hole susceptor unit upper side, in particular on an upper side of the preheat ring.

Additionally or alternatively, the sealing ring unit can be arranged on the layer deposition arrangement in such a way that it at least partially overlaps the hole susceptor unit and the preheat ring, viewed in a radial direction of the hole susceptor unit, and protrudes substantially completely over the gap unit, in particular in the form of an air gap ring, viewed in the radial direction.

In other words, it is also conceivable that the sealing ring unit can be arranged on the layer deposition arrangement within the gap unit as long as the above-described function of the sealing ring unit as a physical barrier unit is ensured and at the same time in spite of the internal arrangement within the gap unit, the reliable rotation of the hole susceptor unit in relation to the preheat ring during the epi-deposition mode is ensured.

Although a single sealing ring unit arranged accordingly on the layer deposition arrangement already reliably takes over the function of creating a physical barrier unit, in further preferred variants, it can be provided that at least one further sealing ring unit is arranged. In such a layer deposition arrangement, for example, a first sealing ring unit can be arranged on the susceptor unit lower side according to one of the variants described herein and a second sealing ring unit can be arranged on the upper side of the preheat ring according to one of the variants described herein. In this way, reductions down to avoidance of the occurrence of the “autodoping” effect during the epi-deposition mode are particularly advantageously achieved.

In principle, the geometric design of the hole susceptor unit and the preheat ring and the location of the gap ring and the sealing ring unit can take place in any way as long as the above-described requirements for the layer deposition arrangement with respect to producing the semiconductor wafer without occurring “autodoping” effect and with respect to reliable rotation of the hole susceptor unit in relation to preheat ring and uniform deposition of the epitaxial layer during the epi-deposition mode is ensured. In particularly advantageous variants of the invention, however, it is preferably provided that the preheat ring unit, preferably starting from a circumferential edge of the hole susceptor unit, is arranged spaced apart in relation to a radial direction of the hole susceptor unit, via a gap unit formed substantially annularly around the hole susceptor unit, in particular in the form of an air gap ring and the preheat ring surrounds the hole susceptor unit at least in some sections, preferably completely, at least along a circumferential direction of the hole susceptor unit. Particularly compact, reliable embodiments of the layer deposition unit are achieved in this way.

The sealing ring unit can in principle be designed geometrically arbitrarily, as long as it thus achieves the functions described above in detail on the layer deposition arrangement. In particularly advantageous variants, the sealing ring unit is preferably substantially in the form of

an annular disk; in this case the sealing ring unit can be formed in radial section having substantially plane-parallel surfaces or in radial section can have a shape deviating therefrom, such as a L shape or Z shape.

- 5 In further advantageous variants, the sealing ring unit can be formed as substantially annular and, viewed along its radial direction, can have a sealing ring width in a range of 5 mm to 50 mm, preferably in a range of 15 mm to 25 mm. In addition, the gap unit can be designed in the form of an air gap ring and, viewed in the radial direction of the hole susceptor unit, can have a gap width in the range of 1.2 mm to 2.6 mm, preferably in the range of 1.5 mm to 2.2 mm, more
10 preferably substantially 1.9 mm, wherein in particular the gap width along the circumferential direction is substantially constant.

In all of these variants of the sealing ring embodiment, the above-described functions of the sealing ring unit on the layer deposition arrangement are achieved in their entirety.

- 15 The radial direction can be understood in principle as any direction starting from a center point (or center axis) of the hole susceptor unit, which is in particular substantially symmetrical, in the direction of the gap unit and along a hole susceptor unit radius.

- In principle, the sealing ring unit can be fastened in any manner on the layer deposition
20 arrangement or can be a physical part thereof. In one advantageous variant, the sealing ring unit is preferably arranged detachably fastened on the layer deposition arrangement, for example, on the hole susceptor unit or on the preheat. Such designs permit a very flexible exchange of the components and access to components lying further inward (in particular the gap unit) during repair, maintenance, or other intervention situations in the layer deposition
25 arrangement. In this case, the sealing ring unit is preferably detachably fastened via a clamp connection, plug connection, or via a screw connection on the hole susceptor unit or on the preheat ring.

The sealing ring unit is preferably produced from a material which comprises SiC or graphite or quartz.

- 30 Alternatively to these variants, the sealing ring unit can be designed substantially as a monolithic unit having the hole susceptor unit or having the preheat ring. Such an embodiment advantageously reduces the number of joints in the layer deposition arrangement in comparison to detachable connecting points of the sealing ring unit.

- 35 The invention has furthermore recognized that to further reduce (or in particular to substantially avoid) the “autodoping” phenomenon in the semiconductor wafer to be produced during the epi-

deposition mode, the layer deposition arrangement having its hole susceptor unit is preferably to be designed in such a way that a reliable physical barrier unit is ensured between the upper side and the lower side of the layer deposition arrangement and also between the support surface for the semiconductor wafer on the hole susceptor unit and the upper side of the hole susceptor unit.

The receptacle point on the hole susceptor unit for the substrate wafer can in principle be designed arbitrarily. Particularly advantageous embodiments for reducing or avoiding the “autodoping” effect in the semiconductor wafer to be produced are achieved if a reliable physical barrier unit is also ensured between the support surface for the semiconductor wafer on the hole susceptor unit and the upper side of the hole susceptor unit. This can advantageously be achieved in that the support surface is preferably designed and inclined (i.e. by design of the geometric shape) in such a way that the substrate wafer placed thereon itself becomes the physical barrier unit or acts as such. In order to achieve this advantageous effect, it is provided for this purpose in particularly advantageous variants that the hole susceptor unit has a recess in the form of a substrate wafer receptacle unit on the hole susceptor unit upper side, which in turn comprises a substrate wafer receptacle surface formed substantially like a lateral inner surface of a truncated cone or in a funnel shape, wherein the surface, starting from a ledge reference point on a reference circle on the substrate wafer receptacle surface, has an inclination in relation to a radial direction of the hole susceptor unit and a horizontal plane of the hole susceptor unit in the form of a ledge angle, wherein the ledge angle has an angle dimension in the range of 0.0° to 2.0° , preferably in the range of 0.1° to 1.0° , more preferably in the range of 0.2° to 0.5° and, viewed along a circumferential direction of the hole susceptor unit, is substantially constant with a maximum variation of 1%, preferably at most 0.5%, more preferably at most 0.25%, along the circumferential direction.

In other words, by the deliberate selection of the geometric design of the support surface, namely in the form of this substrate wafer receptacle surface like a truncated cone or funnel shape within the hole susceptor unit, a support surface for a substrate wafer is created which, with a substrate wafer deposited during the epi-deposition mode, then causes a substantially joint-free, thus “tight” (in particular substantially annular) contact area to arise (between substrate wafer and support surface on hole susceptor unit), which forms a further physical barrier against undesired flows between upper side and lower side of the layer deposition arrangement and therefore provides a positive contribution to reducing or substantially avoiding the “autodoping” effect in the epitaxial layer.

In particularly advantageous variants, to achieve the reduction, in particular avoidance, of the “autodoping” effect, it is provided that the substrate wafer receptacle surface itself does not

have any hole units. In contrast, hole units are preferably provided distributed within the inner bottom surface of the substrate wafer receptacle unit of the hole susceptor unit, as is also provided in the generic hole susceptor unit (which is not discussed in more detail here).

- 5 It is also particularly advantageous if the substrate wafer receptacle surface preferably has a planarity dimensional tolerance in the range of 0.002 mm to 0.012 mm, preferably in the range of 0.005 mm to 0.008 mm. Such a unit of the substrate wafer receptacle surface also provides a contribution, with a deposited substrate wafer, for a substantially joint-free, thus “tight” contact and therefore ensures the required physical barrier.

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The location of the reference circle in particular defines the starting area of the inclination (ledge angle α_L) of the substrate wafer receptacle surface within the substrate wafer receptacle unit. The reference circle preferably coincides with the inner circumferential edge of the phase of the substrate wafer receptacle unit. In alternative advantageous variants, the reference circle can
 15 extend spaced apart from this inner circumferential edge in the direction of the vertical center axis of the hole susceptor unit; thus can have a smaller reference radius than the (imaginary) radius to the inner circumferential edge of the substrate wafer receptacle unit.

- A further advantageous contribution to reducing or substantially avoiding the “autodoping”
 20 phenomenon in the epitaxial layer during the epi-deposition mode can be achieved if it is preferably provided that a flushing unit having a flushing gas, in particular having hydrogen, is provided on the side of the layer deposition arrangement facing toward the hole susceptor unit lower side. In this case, the geometric alignment of a flushing nozzle of the flushing unit and the flushing pressure of the flushing gas can be pre-definably settable on the flushing unit.

- 25 Due to the provision of the above-described physical barrier units, it is advantageously possible to reduce, in particular to substantially avoid, process gases from passing from the upper side into the lower side of the layer deposition arrangement and causing coaching or deposits, due to which a flushing gas flushing, which is in particular a hydrogen flushing, by means of the flushing unit under the hole susceptor unit can advantageously be reduced down to 3 slm (in
 30 comparison to typically higher values in the range of 8 slm to 30 slm).

- According to a further, second aspect, the invention relates to a method for producing a semiconductor wafer using the layer deposition arrangement just described according to one of the above-described variants (or combinations thereof), comprising depositing at least one
 35 epitaxial layer on a (highly) doped substrate wafer, which does not have a doping diffusion

barrier layer, in particular does not have an LTO layer, to produce the semiconductor wafer in an epi-reactor, wherein the method comprises the following steps:

- positioning a second wafer side of the doped substrate wafer at a hole susceptor unit, in particular at a substrate wafer receptacle surface, of a layer deposition arrangement according to one of the above-described designs or variants for the layer deposition arrangement (or any combination of the above-described preferred variants),
- starting an epi-deposition mode of the layer deposition arrangement,
- depositing at least one epitaxial layer on a first wafer side of the doped substrate wafer during the epi-deposition mode.

In this case it is provided that at least during the epi-deposition mode, a rotation of the hole susceptor unit around a vertical center axis of the hole susceptor unit in relation to the preheat ring takes place at a specifiable rotational velocity, in particular in the range of 25 rpm to 60 rpm.

An epi-deposition mode is preferably to be understood as the process mode which, within a (typically designed) epi-reactor, comprises the complete deposition process of the at least one epitaxial layer on the substrate wafer.

Preferably, in addition to the actual deposition process, the epi-deposition mode also comprises process times prior and subsequent thereto, during which, for example, only the hole susceptor unit having the deposited substrate wafer rotates in relation to the preheat ring, without a deposition occurring at the same time.

The layer deposition arrangement is preferably designed so that different epi-deposition modes can be executed thereon offset in time, wherein the modes can differ, for example, in the flow rate of the deposition gases in the epi-reactor, the type of the deposition medium, in the specified epi-process temperature window, in the rotational velocity of the hole susceptor unit, etc.

The substrate wafer is preferably designed as a monocrystalline silicon wafer and the at least one deposited epitaxial layer as a monocrystalline silicon layer.

By means of the method according to the invention using the above-described layer deposition arrangement (i.e. while substantially avoiding an “autodoping” effect during the epi-deposition mode) a semiconductor wafer having the advantageous properties described at the outset with respect to RRV value of the epitaxial layer and having comparatively defect-reduced surface

quality of the final semiconductor wafer (in particular with respect to the surface side of the substrate wafer, which is at least temporarily provided with an LTO layer in the prior art) can be achieved in its entirety.

- 5 A further advantageous contribution to reducing or substantially avoiding the “autodoping” phenomenon in the epitaxial layer during the epi-deposition mode can be achieved if the method furthermore preferably provides that during the epi-deposition mode, on the side of the layer deposition arrangement facing toward a hole susceptor unit lower side, a flushing unit having a flushing gas, in particular in the form of hydrogen, is provided, wherein the flushing by means
10 of the flushing gas, in particular in the form of a hydrogen flushing, under the hole susceptor unit can be kept pre-definably controlled and variable, in particular pre-definably controlled and variable to at least 3 slm and at most 30 slm, over the epi-deposition mode.

- 15 In further preferred variants of the method, it is preferably provided that after completing the deposition of at least one epitaxial layer and after ending the epi-deposition mode, the produced semiconductor wafer experiences a final cleaning step which comprises chemical cleaning of the semiconductor wafer.

- According to a further, third aspect, the invention finally relates to a semiconductor wafer
20 comprising a substrate wafer and at least one epitaxial layer, wherein
- the substrate wafer has a doping by means of at least one dopant, in particular boron,
 - the at least one epitaxial layer is arranged on a first wafer side of the substrate wafer, and
 - the semiconductor wafer:
25 has a radial resistance variation (RRV) in the range of 1.30% to 2.20%, and has at least 1 defect and fewer than 200 effects on a second wafer side of the substrate wafer, which are detectable using an inspection device by means of scattered light measurement as light point defects, and which are arranged on a defect ring formed, at least in some sections, substantially annularly, which extends within a substantially
30 annular area on the second wafer side, wherein the area has a radial width of 3 mm and its outer circumference substantially coincides with the semiconductor wafer edge.

- The semiconductor wafer according to the invention having its advantageous RRV value and simultaneously its comparatively defect-reduced second wafer side is a direct result of an
35 epitaxial deposition on a boron-doped substrate wafer carried out according to the method according to the invention on the layer deposition arrangement according to the invention (i.e.

among other things with complete abstinence from an LTO layer). These few defects (at least 1 defect and fewer than 200) on the semiconductor wafer according to the invention result in this case in particular solely from scratches or from friction-related deposit conditions of the semiconductor wafer edge on the substrate wafer support surface during the epi-mode (and also not additionally due to a high number of additional defects as a result of LTO layer residues in this area as is the case in the prior art). Preferably, the number of these defects is in a range of 1 defect to 100 defects, more preferably in a range of 6 to 100 defects.

These defects (in their advantageously comparatively small number) are in particular detectable using an inspection device by means of scattered light measurement as light point defects, in particular using an EBI unit (for example from the company Nanophotonics AG having a mode of operation as described in paragraph [0053] in DE102009011622 A1).

In other words, it is preferably provided that no layer in the form of a doping diffusion barrier layer, in particular in the form of a low thermal oxide (LTO) layer is arranged on the second wafer side of the substrate wafer, wherein in particular at no time of the production of the semiconductor wafer is a low thermal oxide (LTO) layer arranged on the second wafer side of the substrate wafer. In other words, it is provided in particular that no residues in the form of defects of a low thermal oxide (LTO) layer are arranged on the second wafer side of the substrate wafer.

In preferred variants, it can be provided that the doped substrate wafer having the dopant boron forms a substrate resistance of the substrate wafer between 0.005 and 0.020 Ohmcm, and/or the semiconductor wafer has an RRV in a range of 1.40% to 2.10%, preferably in a range of 1.45% to 2.00%.

The substrate wafer is preferably formed as a monocrystalline silicon wafer and the at least one deposited epitaxial layer is a monocrystalline silicon layer.

The deposited epitaxial layer preferably has an average layer thickness in a range of 1.5 μm to 20 μm . However, the invention is not restricted to this range and a greater or lesser layer thickness of the deposited epitaxial layer is possible.

The substrate wafer preferably has an average layer thickness of essentially 775 μm . However, the invention is not restricted to this range and a greater or lesser layer thickness of the substrate wafer is possible.

The invention is particularly suitable for produced semiconductor wafers having a target diameter in a range of 290 to 310 mm, in particular for a semiconductor wafer having a target diameter of essentially 300 mm ("300 mm wafer"), but is not restricted thereto. For example, among other things, the production of a "200 mm" wafer is also conceivable (with a corresponding adaptation of the diameter of the recess unit of the susceptor unit).

In further preferred variants of the semiconductor wafer, the semiconductor wafer can be formed in such a way that for a doped substrate wafer of the semiconductor wafer having a substrate resistance in a range of 0.005 to 0.008 Ohmcm, it forms an RRV of the semiconductor wafer in a range of 1.40% to 2.10%, preferably in a range of 1.45% to 2.00%. Alternatively thereto, the semiconductor wafer can be formed in such a way that for a doped substrate wafer of the semiconductor wafer having a substrate resistance in a range greater than 0.008 to 0.016 Ohmcm, it forms an RRV of the semiconductor wafer in a range of 1.40% to 1.80%, preferably in a range of 1.45% to 1.60%, more preferably essentially 1.50%. In particular, the described RRV values can be achieved in an epi-deposition mode of an epi-process which is carried out at a temperature in the range of 1080°C to 1125°C, preferably in the range of 1100°C to 1120°C, and in particular the substrate wafer is boron doped.

In relation to semiconductor wafers which are manufactured by means of conventional hole susceptor units (i.e. in particular without a sealing ring and/or without corresponding geometrically designed substrate wafer receptacle surface within the hole susceptor unit), the described preferred variants of the semiconductor wafers furthermore display the advantage that their RRV values are significantly lower in comparison to RRV values of those semiconductor wafers which were produced by means of these conventional hole susceptor units and using substrate wafers (also) without doping a diffusion barrier layer. In addition, the RRV value of the semiconductor wafer is subject to a lower sensitivity in relation to a dependence on the dopant quantity in the substrate wafer (in other words a lower dependence on the substrate resistance). The latter effect enables a flexible use of the layer deposition arrangement in the epi-reactor for different epi-process controls since adjustments or re-fittings on the epi-reactor for substrate wafers of different dopant quantity are implementable faster in comparison to known embodiments of the layer deposition arrangement (having a conventional hole susceptor).

For example, in this case in advantageous variants of the semiconductor wafer, the substrate resistance of the substrate wafer of the semiconductor wafer can be in a range of 0.005 to 0.008 Ohmcm and the RRV of the semiconductor wafer can correspond to a percentage value in the

range of 40% to 50% of a reference RRV, which is formed with equal substrate resistance and identically formed substrate wafer as a reference substrate wafer of a reference semiconductor wafer, on which at least one epitaxial layer is deposited by means of a (conventional) hole susceptor unit, i.e. in particular without sealing ring unit and/or without corresponding

5 geometrically designed substrate wafer receptacle surface within the hole susceptor unit, on the reference substrate wafer with identical epi-deposition mode settings. Alternatively, the substrate resistance of the substrate wafer of the semiconductor wafer can be in a range greater than 0.008 to 0.012 Ohmcm and the RRV of the semiconductor wafer can correspond to a percentage value in the range of 40% to 65% of a reference RRV, which is formed with equal

10 substrate resistance and identically formed substrate wafer as the reference substrate wafer of a reference semiconductor wafer, on which at least one epitaxial layer is deposited by means of a (conventional) hole susceptor unit, i.e. in particular without sealing ring unit and/or without corresponding geometrically designed substrate wafer receptacle surface within the hole susceptor unit, on the reference substrate wafer with identical epi-deposition mode settings.

15 Alternatively, the substrate resistance of the substrate wafer of the semiconductor wafer can be in a range greater than 0.012 to 0.016 Ohmcm and the RRV of the semiconductor wafer can correspond to a percentage value in the range of 60% to 85% of a reference RRV, which is formed with equal substrate resistance and identically formed substrate wafer as the reference substrate wafer of a reference semiconductor wafer, on which at least one epitaxial layer is

20 deposited by means of a (conventional) hole susceptor unit, i.e. in particular without sealing ring unit and/or without corresponding geometrically designed substrate wafer receptacle surface within the hole susceptor unit, on the reference substrate wafer with identical epi-deposition mode settings. In particular, the described RRV values can be achieved in an epi-deposition mode of an epi-process which is carried out at a temperature in the range of 1080°C to 1125°C,

25 preferably in the range of 1100°C to 1120°C.

In particular, the substrate wafer is boron doped.

Brief Description of the Figure

Figure 1 shows a schematic detail of a three-dimensional view of a layer deposition arrangement 1 having a hole susceptor unit 1.1, preheat ring 1.2, gap unit 1.3, and sealing ring unit 1.4 (flushing unit not shown).

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Preferred Exemplary Embodiment

A preferred exemplary embodiment of the layer deposition arrangement 1 according to the invention is described hereinafter. Furthermore, a preferred exemplary embodiment of the semiconductor wafer according to the invention (comprising a boron-doped silicon substrate wafer and a deposited epitaxial monocrystalline silicon layer) is described, which is produced
 5 by means of this layer deposition arrangement 1 according to the method according to the invention.

Figure 1 shows a schematic detail of a three-dimensional view of the layer deposition arrangement 1 having a hole susceptor unit 1.1 and a preheat ring 1.2. In this case, the preheat
 10 ring 1.2 is arranged, starting from a circumferential edge 1.11 of the hole susceptor unit 1.1 in relation to a radial direction of the hole susceptor unit 1.1, spaced apart via a substantially annular gap ring unit 1.3 formed around the hole susceptor unit 1.1 in the form of an air gap ring 1.3 and the preheat ring surrounds the hole susceptor unit 1.1 here along the circumferential direction of the hole susceptor unit 1.1. The air gap ring 1.3 has a gap width of
 15 1.9 mm viewed in the radial direction of the hole susceptor unit 1.1, wherein the gap width remains essentially constant along the circumferential direction. This embodiment ensures reliable rotation (at a specifiable rotational velocity, for example, in the range of 25 rpm to 60 rpm, here essentially at the level of 50 rpm) of the hole susceptor unit 1.1 in relation to the preheat ring 1.2 around the vertical center axis and thus a uniform deposition of the epitaxial
 20 layer on the substrate wafer deposited on the hole susceptor unit 1.1 (specifically on a first wafer side of the substrate wafer) during an epi-deposition mode.

The sealing ring unit 1.4 of the layer deposition arrangement 1, as shown in Figure 1, is designed to provide a physical barrier unit at the air gap ring 1.3 between a hole susceptor unit
 25 upper side 1.12 and the hole susceptor unit lower side 1.13.

The sealing ring unit 1.4 is formed essentially as an annular disk in the present exemplary embodiment, consists of SiC, and is arranged directly at the hole susceptor unit lower side 1.13. The design of the seal ring unit in the form of an annular disk has a substantially Z-shaped form in the radial section in Figure 1, wherein here the sealing ring unit 1.4 is fastened on the hole
 30 susceptor unit (not shown in more detail) via multiple detachable clamp connections on the hole susceptor unit lower side 1.13 extending along the circumferential direction 1.11. Furthermore, the sealing ring unit 1.4 is attached to the layer deposition arrangement 1 such that it partially overlaps the hole susceptor unit 1.1 and the preheat ring 1.2, viewed in a radial direction of the hole susceptor unit 1.1 and protrudes completely over the air gap ring viewed in the radial
 35 direction. In the present exemplary embodiment, a clearance 1.5 remains between the lower side of the preheat 1.2 and the facing side of the sealing ring leg 1.41, wherein the measure

applies for the size of the clearance 1.5 that the clearance 1.5 is to be as large as necessary in order to ensure a secure reliable procedure of the epi-deposition mode, but is to be as small as possible so as to still ensure the required physical barriers. In the present case, the clearance 1.5 is 1.0 mm in the vertical direction. For this purpose, the sealing ring unit in the present exemplary embodiment also has a corresponding length along the radial direction, in the present case of 20 mm (so that an undesired flow path between the hole susceptor unit upper side 1.12 and the hole susceptor unit lower side 1.13 is extended or obstructed).

It is apparent that in other embodiments, other dimensions, geometrical designs, and arrangement points (for example, on the preheat ring upper side) for the sealing ring unit and a clearance 1.5 of another size can also be selected, as long as the sealing ring unit 1.4 ensures the function of a physical barrier between the hole susceptor unit upper side 1.12 and the hole susceptor unit lower side 1.13 (in other words to substantially prevent the exchange of deposition process gases and boron dopants via the gap unit 1.3).

The layer deposition arrangement 1 comprises a recess in the form of a substrate wafer receptacle unit 1.15 for accommodating the deposited substrate wafer, which in turn comprises a substrate wafer receptacle surface 1.14 and also an inner bottom surface 1.16 (which is provided with hole units as in conventional hole susceptors).

Specifically, a second wafer side of the deposited substrate wafer faces toward the substrate wafer receptacle surface 1.14.

The substrate wafer receptacle surface 1.14 is essentially formed like a lateral inner surface of a truncated cone or essentially funnel-shaped, wherein the substrate wafer receptacle surface 1.14, starting from an (imaginary) ledge reference point L-BP on an (imaginary) reference circle BK on the substrate wafer receptacle surface 1.14, has an inclination in relation to a radial direction of the hole susceptor unit and a horizontal plane of the hole susceptor unit in the form of a ledge angle α_L and the ledge angle α_L in the present exemplary embodiment has an angle size of 0.2° and, viewed along the circumferential direction of the hole susceptor unit 1.1, extends substantially consistently with a maximum variation of 0.25% along the circumferential direction. This geometrical design of the substrate wafer receptacle surface 1.14 ensures a substantially joint-free, thus "tight" contact for the substrate wafer and therefore produces a physical barrier between the support surface for the semiconductor wafer on the hole susceptor unit 1.1 and the hole susceptor unit upper side 1.12, which further reduces, in particular avoids, the "autodoping" effect.

The location of the reference circle BK defines the starting area of the inclination (ledge angle α_L) of the substrate wafer receptacle surface 1.14 within the substrate wafer receptacle unit 1.15. In the present exemplary embodiment, the reference circle coincides with the inner

circumferential edge of the phase of the substrate wafer receptacle unit 1.15. It is apparent that in other advantageous variants, the reference circle BK can extend spaced apart from this inner circumferential edge in the direction of the vertical center axis, thus has a smaller reference radius.

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A radial direction can be understood in this case as any direction starting from the vertical center axis of the substantially symmetrical hole susceptor unit 1.1 and perpendicular to the vertical center axis in the direction of the air gap ring 1.3 and along a hole susceptor unit radius.

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Furthermore, the substrate wafer receptacle surface has a planarity dimensional tolerance of 0.010 mm. This geometrical design of the substrate wafer receptacle surface 1.14 also ensures a substantially joint-free, thus “tight” contact for the substrate wafer and therefore produces a physical barrier between the support surface for the semiconductor wafer on the hole susceptor unit 1.1 and the hole susceptor unit upper side 1.12, which further reduces, in particular substantially avoids, the “autodoping” effect.

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To achieve the reduction of the “autodoping” effect, it is furthermore provided that the substrate wafer receptacle surface 1.14 itself does not comprise hole units in this case. In contrast, as is also provided in the generic hole susceptor unit, hole units are provided distributed within the inner bottom surface 1.16 of the substrate wafer receptacle unit 1.15 of the hole susceptor unit 1.1 (which is not discussed in more detail here; a small number of hole units are indicated as examples in the hole susceptor center in Figure 1).

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To further advantageously reduce or substantially avoid the “autodoping” phenomenon in the epitaxial layer to be deposited during the epi-deposition mode, it is furthermore provided in the present exemplary embodiment that a flushing unit 1.6 having a flushing gas in the form of hydrogen is provided on the side of the layer deposition arrangement 1 facing toward the hole susceptor unit lower side 1.13, the flushing gas flushing, thanks to the provision of the sealing ring unit 1.4 on the layer deposition arrangement hole susceptor unit and thanks to the design and additional function of the support surface (barrier unit) under the hole susceptor unit 1.1, is reducible down to 3 slm.

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In particular due to the interaction of all these structural (arrangement of the sealing ring unit 1.4; geometrical design of the substrate wafer receptacle surface 1.14; geometrical design of the gap unit 1.3) and process-technology precautions (reduced flushing by flushing unit 1.6 of the hole susceptor unit lower side 1.3) on the layer deposition arrangement 1, reductions are

particularly advantageously achieved with respect to the “autodoping” effect down to complete avoidance of the “autodoping” effect on the semiconductor wafer to be produced.

The deposition of the epitaxial layer on the first wafer side of the boron-doped substrate wafer during the epi-deposition mode takes place in a temperature range of 1100°C to 1120°C. After the complete deposition of the epitaxial layer on the first wafer side of the boron-doped substrate wafer during the epi-deposition mode and after complete ending of the epi-deposition mode, the produced semiconductor wafer is removed from the epi-reactor.

The semiconductor wafer produced by means of the layer deposition arrangement 1, the boron-doped substrate wafer of which has a substrate resistance (ascertained by means of layer resistance measurement according to SEMI Standards MF673 “*TEST METHODS FOR MEASURING RESISTIVITY OF SEMICONDUCTOR WAFERS OR SHEET RESISTANCE OF SEMICONDUCTOR FILMS WITH A NONCONTACT EDDY-CURRENT GAUGE*”) of 0.005 Ohmcm, has an RRV of the epitaxial layer in the amount of essentially 2.10%. This RRV value was ascertained using the ascertainment method according to SEMI Standards M62-0317 (Specification for Silicon Epitaxial Wafers), 2017) ($RRV [\%] = (R_{\max} - R_{\min}) / (R_{\max} + R_{\min})$) in consideration of nine ascertained R values resulting from nine measurement points on the epitaxial layer (wherein the nine measurement points were arranged on a cross-shaped measurement grid on the epitaxial layer, wherein the measurement grid leads through the semiconductor wafer notch); the four measurement points assigned to the edge area of the semiconductor wafer are arranged in consideration of an edge exclusion, wherein the measurement point in the surroundings of the notch is selected in this case in consideration of an edge exclusion of 10 mm (i.e. arranged spaced apart in a radial direction 10 mm from the edge on the measurement grid) and the remaining three measurement points, which are located in the edge area of the semiconductor wafer, are selected in consideration of an edge exclusion of 5 mm (i.e. arranged spaced apart in a radial direction 5 mm from the edge on the measurement grid).

The RRV of the epitaxial layer of the semiconductor wafer in the amount of 2.10% fundamentally corresponds to the RRV value which the semiconductor wafer would obtain after the epitaxial deposition upon provision of an LTO layer as a dopant diffusion barrier layer on the second layer side of the substrate wafer in conventional production on a conventional hole susceptor unit, but now with the advantage that no LTO layer at all has to be removed manually and/or chemically (for example using HF component) after the epi-deposition mode and therefore the surface properties on the second wafer side of the substrate wafer are also advantageously improved in comparison to the prior art using LTO layer in such a way that the second wafer

side of the doped substrate wafer is comparatively defect-reduced. Specifically, the second wafer side of the substrate wafer in the present exemplary embodiment has 6 defects, which are arranged on a defect ring formed substantially annular at least in sections, which extends within a substantially annular area on the second wafer side, wherein the area has a radial width of 3 mm and its outer circumference substantially coincides with the semiconductor wafer edge.

These 6 defects (in their advantageously small number) on the semiconductor wafer are defects which were detected using an inspection device by means of scattered light measurement as light point defects (defects resulting from residues of a removed LTO layer (prior art) would in principle also be detected as light point defects in this semiconductor wafer area and moreover in a higher number (together with the other defects as light point defects in total more than 200); in the absence of LTO layer residues in the semiconductor wafer according to the invention, the detected 6 light point defects exclusively represent defects resulting from scratches or from friction points on the substrate wafer receptacle surface or similar scenarios and these are in these comparatively small number of defects).

In relation to semiconductor wafers which are manufactured by means of conventional hole susceptor units (i.e. in particular without sealing ring and/or without corresponding geometrically designed substrate wafer receptacle surface within the hole susceptor unit), the semiconductor wafer furthermore has the advantage that its RRV value (2.10%) is significantly lower in comparison to the RRV value of the semiconductor wafer which was produced by means of these conventional hole susceptor units with equal substrate resistance (0.005 Ohmcm) and which (also) was produced using substrate wafer without doping diffusion barrier layer. In the present exemplary embodiment, the RRV of the semiconductor wafer corresponds to approximately 40% of a reference RRV which is formed with equal substrate resistance and identically formed substrate wafer of a reference semiconductor wafer, the epitaxial layer of which is deposited by means of a (conventional) hole susceptor without sealing ring unit 1.4 and without the provision of a corresponding geometrically designed substrate wafer receptacle surface 1.14 on a substrate wafer equivalent to the substrate wafer.

Claims

1. A layer deposition arrangement (1) for an epi-reactor for producing a semiconductor wafer having at least one epitaxial layer, wherein

- the layer deposition arrangement (1) comprises a hole susceptor unit (1.1) and a preheat ring (1.2), wherein the hole susceptor unit (1.1) has a hole susceptor unit upper side (1.12) and a hole susceptor unit lower side (1.13),

wherein, at least during an epi-deposition mode,

- the preheat ring (1.2) surrounds the hole susceptor unit (1.1) at least in sections, spaced apart via a gap unit (1.3), in particular in the form of an air gap ring, wherein the hole susceptor unit (1.1) is designed to rotate at a predeterminable rotational velocity around a vertical axis of the hole susceptor unit (1.1) in relation to the preheat ring (1.2), and
- the layer deposition arrangement (1) furthermore comprises at least one sealing ring unit (1.4), which is arranged on the layer deposition arrangement (1) and is designed so as to provide a physical barrier unit on the gap unit (1.3) between the hole susceptor unit upper side (1.12) and the hole susceptor unit lower side (1.13).

2. The layer deposition arrangement as claimed in claim 1, wherein

- the sealing ring unit (1.3) is formed essentially as an annular disk,

and/or

- the sealing ring unit (1.4) is arranged at a point on the side of the layer deposition arrangement (1) facing toward the hole susceptor unit lower side (1.13), in particular directly on the hole susceptor unit lower side (1.13), or is arranged at a point on the side of the layer deposition arrangement (1) facing toward the hole susceptor unit upper side (1.12), in particular on an upper side of the preheat ring (1.2),

and/or

- the sealing ring unit (1.4) is arranged on the layer deposition arrangement (1) in such a way that it at least partially overlaps the hole susceptor unit (1.1) and the preheat ring (1.2), viewed in a radial direction of the hole susceptor unit (1.1), and protrudes essentially completely beyond the gap unit (1.4), in particular in the form of an air gap ring, viewed in the radial direction.

3. The layer deposition arrangement as claimed in claim 1 or 2, wherein

- the sealing ring unit (1.4) is formed essentially annular and, viewed along its radial direction, has a sealing ring width in the range of 5 mm to 50 mm, preferably in a

range of 15 mm to 25 mm, and the gap unit (1.3) in the form of an air gap ring, viewed in the radial direction of the hole susceptor unit (1.1), has a gap width in the range of 1.2 mm to 2.6 mm, preferably in the range of 1.5 mm to 2.2 mm, more preferably essentially 1.9 mm, wherein in particular the gap width is essentially constant along the circumferential direction.

4. The layer deposition arrangement as claimed in any one of the preceding claims, wherein

- the sealing ring unit (1.4) is arranged detachably fastened on the layer deposition arrangement (1), in particular on the hole susceptor unit (1.1) or on the preheat ring (1.2) and the sealing ring unit (1.4) is in particular produced from a material which comprises SiC or graphite or quartz,

or

- the sealing ring unit (1.4) is substantially formed as a monolithic unit with the hole susceptor unit (1.1) or the preheat ring (1.2).

5. The layer deposition arrangement as claimed in any one of the preceding claims, wherein

the hole susceptor unit (1.1) comprises a recess on the hole susceptor unit upper side (1.12) in the form of a substrate wafer receptacle unit (1.15), which comprises a substrate wafer receptacle surface (1.14),

wherein

- the substrate wafer receptacle surface (1.14) is formed substantially like a lateral inner surface of a truncated cone, wherein, starting from a ledge reference point on a reference circle on the substrate wafer receptacle surface (1.14), it has an inclination in relation to a radial direction of the hole susceptor unit (1.1) and a horizontal plane of the hole susceptor unit (1.1) in the form of a ledge angle, wherein the ledge angle has an angle size in the range of 0.0° to 2.0°, preferably in the range of 0.1° to 1.0°, more preferably in the range of 0.2° to 0.5°, and is substantially constant viewed along a circumferential direction of the hole susceptor unit (1.1), having a maximum variation of 1%, preferably at most 0.5%, more preferably at most 0.25%, along the circumferential direction,
- and/or
- the substrate wafer receptacle surface (1.1) has a planarity dimensional tolerance in a range of 0.002 mm to 0.012 mm, preferably 0.005 mm to 0.008 mm.

6. The layer deposition arrangement as claimed in any one of the preceding claims, wherein

a flushing unit having a flushing gas, in particular having hydrogen, is provided on the side of the layer deposition arrangement (1) facing toward the hole susceptor unit lower side (1.13), wherein a flushing gas flushing, in particular hydrogen flushing, under the hole susceptor unit (1.1) is reducible down to 3 slm.

7. A method for producing a semiconductor wafer, comprising the deposition of at least one epitaxial layer on a doped substrate wafer, which does not have a doping diffusion barrier layer, in particular an LTO layer, in an epi-reactor to produce the semiconductor wafer, wherein the method comprises the following steps:

- positioning a second wafer side of the doped substrate wafer on a hole susceptor unit (1.1), in particular on a substrate wafer receptacle surface (1.14), of a layer deposition arrangement (1) as claimed in any one of claims 1 to 6,
- starting an epi-deposition mode of the layer deposition arrangement (1),
- depositing at least one epitaxial layer on a first wafer side of the doped substrate wafer during the epi-deposition mode.

8. The method as claimed in claim 7, wherein

- at least during the epi-deposition mode, a rotation of the hole susceptor unit (1.1) takes place around a vertical center axis of the hole susceptor unit (1.1) in relation to the preheat ring (1.2) at a pre-definable rotational velocity,

and

- during the epi-deposition mode, a flushing unit having a flushing gas, in particular in the form of hydrogen, is provided on the side of the layer deposition arrangement (1) facing toward a hole susceptor unit lower side (1.13), wherein the flushing by means of the flushing gas, in particular in the form of a hydrogen flushing, under the hole susceptor unit (1.1) is kept pre-definably controlled and variable over the epi-deposition mode to at least 3 slm and at most 30 slm.

9. The method as claimed in claim 7 or 8, wherein after completing the deposition of at least one epitaxial layer and after ending the epi-deposition mode, the semiconductor wafer experiences a final cleaning step which comprises a chemical cleaning of the semiconductor wafer.

10. A semiconductor wafer comprising a substrate wafer and at least one epitaxial wafer, wherein

- the substrate wafer includes a doping using at least one dopant,
- the at least one epitaxial layer is arranged on a first wafer side of the substrate wafer,
- the semiconductor wafer
 - has a radial resistance variation (RRV) in a range of 1.30% to 2.20%, and
 - on a second wafer side of the substrate wafer, has at least 1 defect and fewer than 200 defects, which are detectable using an inspection device by means of scattered light measurement as light point defects, and which are arranged on a defect ring formed substantially annularly, at least in some sections, which extends within a substantially annular area on the second wafer side, wherein the area has a radial width of 3 mm and its outer circumference substantially coincides with the semiconductor wafer edge.

11. The semiconductor wafer as claimed in claim 10, wherein no layer in the form of a doping diffusion barrier layer, in particular in the form of a low thermal oxide (LTO) layer is arranged on the second wafer side of the substrate wafer, in particular not at any time of the production of the semiconductor wafer.

12. The semiconductor wafer as claimed in claim 10 or 11, wherein no residues in the form of defects of a low thermal oxide (LTO) layer are arranged on the second wafer side of the substrate wafer.

13. The semiconductor wafer as claimed in any one of claims 10 to 12, wherein the doped substrate wafer having the dopant boron forms a substrate resistance of the substrate wafer between 0.005 and 0.020 Ohmcm, and/or the semiconductor wafer has an RRV in a range of 1.40% to 2.10%, preferably of 1.45% to 2.00%.

14. The semiconductor wafer as claimed in any one of claims 10 to 13, wherein

- the semiconductor wafer is formed such that, for a doped substrate wafer of the semiconductor wafer having a substrate resistance in the range of 0.005 to 0.008 Ohmcm, it forms an RRV of the semiconductor wafer in a range of 1.40% to 2.10%, preferably in a range of 1.45% to 2.00%,

or

- the semiconductor wafer is formed such that, for a doped substrate wafer of the semiconductor wafer having a substrate resistance in a range greater than 0.008

20.016 Ohmcm, it forms an RRV of the semiconductor wafer in a range of 1.40% to 1.80%, preferably in a range of 1.45% to 1.60%, more preferably substantially 1.50%.