ABSTRACT

MULTICHIP WAFER LEVEL PACKAGES AND COMPUTING SYSTEMS INCORPORATING SAME

The present invention defines a packaging implementation providing a multichip multilayer system on a chip solution. Greater integration of a plurality and variety of known good die contained within cavities formed in a separate substrate is achieved. Additional redistribution and interconnect layers above the multichip configuration may be formed with the redistribution layers terminating in electrical connections such as conductive bumps or balls. In one embodiment, the substrate cavities receive signal device connections, such as conductive bumps, of a plurality of semiconductor dice in a flip-chip configuration. A portion of the substrate's back surface is then removed to a depth sufficient to expose the conductive bumps. In another embodiment, the cavities receive the semiconductor dice with their active surface facing up wherein metal layer connections are formed and coupled to bond pads or other electrical connectors of the semiconductor dice. Computing systems incorporating the packaging are also disclosed.

[FIG. 3F]