

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO SEMICONDUCTORS

(71) We, FAIRCHILD CAMERA & INSTRUMENT CORPORATION, of 464 Ellis Street, Mountain View, California 94040, United States of America, a corporation organised and existing under the laws of the state of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices, and in particular, to a semiconductor device capable of sustaining high reverse voltages.

The term "planar" is commonly used in the semiconductor arts to describe a semiconductor device containing a p-n junction which intersects a single plane surface of semiconductor material. This type of device distinguishes from the mesa device which contains a p-n junction which intersects a cylindrical or nonplanar surface of the semiconductor material. In a typical "mesa" device the p-n junction lies completely in a plane. In a "planar" device portions of the p-n junction are curved.

The breakdown voltage of a p-n junction is defined as the reverse voltage at which reversed current above a given magnitude begins to flow. Commonly, in transistors two breakdown voltages are defined: BV_{OBO} denotes the initial breakdown voltage of a reverse-biased collector-base junction with the emitter open-circuited while LV_{OBO} denotes the lowest reverse voltage reached in a transistor with the base lead open-circuited once breakdown begins.

Numerous attempts have been made to increase the breakdown voltages of semiconductor p-n junctions, both planar and mesa. For example, Loro et al in U.S. patent 3,405,329 issued October 8, 1968, substantially increase the breakdown voltage of a p-n junction by placing a shield (i.e. a "field plate") on insulation over the entire line of

intersection of the p-n junction with the surface of the device. The shield, electrically connected to the more highly doped region adjacent the junction, extends on insulation over the more lightly doped region adjacent the junction for at least a short distance beyond this intersection. Loro et al postulated that the field plate caused the junction depletion layer to change in shape at the intersection of the junction with the device surface thereby increasing the breakdown voltage of the junction.

Grove et al in U.S. Patent 3,463,977 issued August 26, 1969 disclose an optimized structure for a planar semiconductor device. Grove et al select the thickness of the insulation between a field plate not connected to the base region and the underlying semiconductor material to equalize the breakdown voltage of the metallurgical p-n junction with the breakdown voltage of the p-n junction induced by the field plate. The result is to maximize the breakdown voltage of the device.

While these prior art attempts to increase the breakdown voltage of p-n junctions, and in particular of planar p-n junctions, where successful, the typical breakdown voltages achieved were less than a thousand volts and, in most cases, at best around 600 to 800 volts.

This invention, on the other hand, significantly increases the breakdown voltage of p-n junctions above the voltages obtained by the prior art.

According to this invention, a semiconductor device comprises; monocrystalline semiconductor material of one conductivity type containing therein a region of opposite conductivity type with the pn junction between said monocrystalline semiconductor material and said region extending to one surface of said semiconductor material; insulation extending across the intersection of said pn junction with said surface; a field plate in contact with said region of said

opposite conductivity type and extending on to the insulation to terminals adjacent to or to overlie the intersection of said p-n junction with said one surface; and resistive polycrystalline silicon film of approximately uniform thickness formed on top of and adherent to said insulation; said polycrystalline silicon film extending from said field plate to an electrode making contact with said monocrystalline material.

It is to be understood that the term "approximately" qualifying the uniform thickness of the resistive polycrystalline silicon film refers to manufacturing tolerances and is not to be taken to mean that the thickness of the film varies in such a manner as to cause the effective resistivity of the film to vary with the distance between said field plate and said electrode.

Upon application of a bias voltage, a small current flows through the resistive material from the field plate to the electrode. The magnitude of this current is determined by the resistivity of the material. However, the voltage drop produced by the current flow through the resistive material is, to a first approximation, reasonably linear with distance. Consequently, the depletion region associated with the metallurgical p-n junction is advantageously shaped to reduce the electric field strength within the depletion region. As a result, the breakdown voltage of the junction is substantially increased relative to that of prior art junctions.

In one embodiment, the depletion region associated with the p-n junction assumes, in the more lightly doped semiconductor material, a shape consisting of a straight-line portion and a complexly-curved portion joined by a curved portion. The complexly curved portion of the depletion region can be approximated by a straight-line

Typically, the resistive material has a sheet resistivity on the order of approximately 3×10^{10} ohms per square. Polycrystalline silicon, formed in a film approximately 7,000 angstroms thick, has the required sheet resistivity. Planar devices using the film resistor of this invention had a junction breakdown voltage in excess of 2,000 volts with total leakage currents less than two microamperes.

Fig. 1 shows a p-n junction of the prior art without a field plate;

Fig. 2 shows a prior-art p-n junction with a field plate overlying, but insulated from, the intersection of the metallurgical p-n junction with the device surface;

Fig. 3 shows the structure of a semiconductor device embodying this invention with a resistive material located on insulation between the field plate and an electrode attached through a degenerate region to the more lightly doped region adjacent the p-n junction; and

Figs. 4a and 4b show in cross-section respective transistors embodying this invention.

While this invention will be described in conjunction with but a single p-n junction, and, in Fig. 4, a single transistor, it should be understood that the invention can be applied to control the breakdown voltages associated with p-n junctions used in a wide variety of devices, ranging, for example, from diodes to thyristors. The structures shown in Figs. 1, 2 and 3 are identical except for the components used to shape the depletion region associated with the p-n junction. Accordingly, identical and well-known portions of these structures are numbered only in Fig. 1; in Figs. 2 and 3 only the distinct or novel features are numbered.

Fig. 1 shows a typical p-n junction of the prior art. A semiconductor wafer 10 comprises a substrate 11 of semiconductor material on which is placed a layer 14 of insulation. Typically, semiconductor material 11 contains a selectively doped n-type region 12 in which is formed a more highly doped p⁺ type region 13. p⁺ type region 13 can be formed in a wide variety of ways ranging from diffusion to ion implantation. A metallurgical p-n junction 18 (shown as a dashed line) separates p⁺ type region 13 from n-type region 12.

Insulation layer 14 is formed over the surface 15 of semiconductor material 11 during the processing of wafer 10. Typically, insulation 14 is thermally-grown silicon oxide, formed prior to and during the diffusion of p⁺ type region 13.

Associated with p-n junction 18 is depletion region 19 the boundaries of which are denoted by lines 18a and 18b. Consisting of a region depleted of mobile minority and majority carriers, depletion region 19 contains an electric field induced by the fixed charges that remain in this region. These charges are positive in that portion of n-type region 12 included in the depletion region and negative in that portion of p-type region 13 included in the depletion region. The intensity of this electric field increases as the reverse voltage across the junction increases. Depletion region 19 contains a curved portion 17 wherein the electric field, represented by the field lines 16, becomes particularly large as the reverse voltage increases. Junction breakdown usually occurs first in this curved region and thus the breakdown voltage BV_{bro} of the junction is the reverse voltage at which this curved portion of the depletion region breaks down.

Electrical contact is made to p⁺ type region 13 and to n-type region 12 in a well-known manner by applying conductive layers (not shown) to selected surface areas of these two regions. Region 13 is contacted through window 14a in layer 14 while region 12 is

contacted either from its bottom side or through another window in layer 14. Varying the electric potential applied to these conductive layers controls the voltage across the p-n junction.

Fig. 2 shows a structure of the prior art using a field plate or field relief electrode 29 to control and shape the depletion region 19. The structure shown in Fig. 2 increases junction breakdown voltage BV_{BO} .

In Fig. 2, field relief electrode 29 extends from conductive layer 29a contacting p⁺ type region 13 over insulation 14 to beyond the intersection of the metallurgical p-n junction 18 with the surface of semiconductor material 11. Portion 29b of field relief electrode 29 extends over n-type region 11 and shapes regions 27 and 28 of the depletion region to decrease the strength of the electric field across these regions. Consequently, even though junction 18 can be made to break down in region 27, the reverse voltage required to induce this breakdown is significantly increased over the reverse voltage required to break down the p-n junction shown in Fig. 1. At best, the breakdown voltage BV_{BO} of the high-voltage junction shown in Fig. 2 is about 600 to 800 volts.

Fig. 3 shows the structure of a semiconductor device embodying this invention wherein the breakdown voltage BV_{BO} of the p-n junction 18 is significantly increased relative to that of the structure shown in Fig. 2. In addition to field relief electrode 29, the structure in Fig. 3 has a charged particle collector 39, sometimes called an equipotential or "EQR" ring, attached to a highly doped n⁺ type region 36 formed in n-type region 12. Ohmic contact can be made to n-type material 12 through region 36. Formed between equipotential ring 39 and field plate 29 is a sheet of resistive polycrystalline silicon material 38. Although material 38 is shown as extending from the end of field plate 29 to the end of equipotential ring 39, in the embodiment shown in Fig. 4, material 38 extends as a film over all of, and is substantially coextensive with, underlying insulation layer 14. Material 38 is uniform in thickness.

A negative voltage applied to p⁺ type region 13 and a positive voltage applied through electrode 39 and n⁺ type region 36 to n-type region 12, reverse biases junction 18. p-n junction 18 might be, for example, the base-collector junction of a transistor, or the p-n junction of a diode. A small leakage current flows through resistive material 38 from p⁺ type region 13 to n-type region 12. This leakage current creates an approximately linear-with-distance voltage drop through material 38.

The leakage current through resistive material 38 is controlled by the resistivity of this material. This resistivity must be low

enough to allow the resistive material to charge (resistive material 38 together with underlying insulation 14 can be considered an RC ladder network for analysis of its time constant) but high enough so that it does not contribute significantly to leakage current. Leakage currents on the order of one microampere are achieved when material 38 has a resistance on the order of 10^8 ohms.

Resistive material 38 forces that portion 37 of depletion region 19 to assume a shape slightly concave upward as shown. Electric field lines 36 within depletion region 19 are approximately parallel, thereby preventing any one region of p-n junction 18 from sustaining an electric field intensity above that required for breakdown. With a normal field plate structure, junction breakdown occurs at the tip of the field plate or at the intersection of the p-n junction with the surface, but with the structure of this invention, the field strength beneath the field plate and resistive material is reduced below the field strength obtained in the same region with a conventional field plate structure. Junction breakdown thus occurs at a much higher reverse voltage than hitherto possible.

In one embodiment, material 38 was polycrystalline silicon with a sheet resistivity of approximately 3×10^{10} ohms per square. The film of material 38 was about 7,000 angstroms thick and the breakdown voltage of the junction between p⁺ type region 13 and n-type region 12 was in excess of 2,000 volts with junction leakage currents less than 2 microamperes. The thickness of insulation 14, a layer of silicon oxide, was about 1.3 microns. Base junction depth, that is the depth of p⁺ type region 13, was 10 microns. The distance which field plate 29 extended beyond the intersection of junction 18 with surface 15 was three mils. The film of material 38 extended for about 10.5 mils from the end of field plate 29 to equipotential ring 39. n-type region 12 was formed of phosphorous-doped monocrystalline silicon possessing a resistivity of about 55 ohm centimeters corresponding to a dopant concentration between 8 and 9×10^{18} atoms per cubic centimeter.

Among the advantages of this invention are a low leakage current across the planar junction. The resistive material eliminates surface arcing between the field plate and the collector electrode and the need for a junction coating. Arcing makes unpredictable the breakdown voltage of the junction and impairs device reliability, and a junction coating is one way of overcoming this arcing. The improved breakdown voltage is achieved with no increase in device area, and the device can be tested to break down non-destructively in the water. Tolerances on the resistivity and the approximately uniform thickness of the polycrystalline silicon are about an order of

magnitude. If desired, silicon nitride passivation can be used over insulation 14 covering the junction.

Fig. 4a shows in cross-section an isometric view of a transistor constructed using the thin-film surface resistor of this invention. For illustrative convenience, the dimensions of this drawing are not to scale. Die or wafer 41 comprises a substrate of monocrystalline semiconductor material containing therein an n-type collector region 53 in which has been diffused a p-type base region 42 and an n-type emitter region 43. Alternatively, the conductivity-type of each region can be reversed if desired. Formed between the base and emitter regions is p-n junction 49 and between the base and collector regions is p-n junction 50. Depletion region 54 associated with p-n junction 50 extends primarily into the n-type collector region 53, which is more lightly doped than the p-type base region. Overlying the surface of the device is insulation layer 44, typically a thermally-grown oxide of silicon. Formed over insulation layer 44 is a layer 45 of polycrystalline silicon possessing a sheet resistivity of the order of 3×10^{10} ohms per square. Windows are etched through polycrystalline silicon layer 45 and oxide layer 44 to form contact regions to the underlying emitter, base, and collector regions. Contact to collector region 53 is made through a degenerate n⁺ type region 52 formed on one surface of collector region 53. An equipotential ring 46 of conductive material contacts n⁺ type region 52 and extends over polycrystalline silicon layer 45 toward field plate 47 contacting base region 42. If desired, ring 46 could be an extension of resistive material 45. Field plate 47, an extension of the contact to base region 42, extends on polycrystalline silicon layer 45 over the intersection of p-n junction 50 with the surface of monocrystalline silicon wafer 41. Contact 48 to emitter region 43 extends slightly on to oxide layer 44. No resistive material of the layer 45 is formed over oxide layer 44 overlying the intersection of p-n junction 49 with the surface of wafer 41 as this junction is forward biased during normal operation of the transistor. However, if desired the polycrystalline silicon can be left on oxide layer 44 over the base-emitter junction since this simplifies the processing steps and does not contribute significantly to emitter-base leakage current. Region 51 of the depletion region 54 is approximately linear with a slight upward concavity, as shown, due to the voltage distribution created by current through resistive layer 45. Transistors constructed using the principles of this invention had breakdown voltages BV_{CBO} in excess of 2,000 volts with an h_{FE} equal to or greater than 12. LV_{CBO} was about 1300 volts.

Fig. 4b shows an alternative embodiment of this invention wherein field plate 47 no

longer extends across the intersection of junction 50 with the surface of the device but rather terminates at the end of resistive layer 45. Plate 47 contacts p-type base region 42 and also contacts material of the layer 45 either at the end of material as shown by the portion of contact 47 represented by the continuous line, or at the end and top of region 45a of layer 45, as shown by section 47a of contact 47. In this embodiment region 45a is selectively doped to increase its conductivity. Region 45a thus, in effect, functions as a field plate and serves to shape the underlying depletion region associated with p-n junction 50. Region 45a does not have to cross the intersection of junction 50 with the semiconductor surface but to cross the intersection of junction 50 with the semiconductor surface but does have to come close to this intersection.

It should be understood that in each of the figures of this application, the polarity of each of the regions of semiconductor material could be reversed, if desired.

It should be noted that the figures are not to scale and that their dimensions have been exaggerated for clarity. In particular, the size of the depletion layer has been exaggerated relative to the size of the collector region to make easier the description of the invention.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising monocrystalline semiconductor material of one conductivity type containing therein a region of opposite conductivity type with the pn junction between said monocrystalline semiconductor material and said region extending to one surface of said semiconductor material; insulation extending across the intersection of said pn junction with said surface; a field plate in contact with said region of said opposite conductivity type and extending on to the insulation to terminate adjacent to or to overlie the intersection of said pn junction with said one surface; and a resistive polycrystalline silicon film of approximately uniform thickness formed on top of and adherent to said insulation, said polycrystalline silicon film extending from said field plate to an electrode making contact with said monocrystalline semiconductor material.

2. A semiconductor device as claimed in claim 1 including means for applying selected potentials to said monocrystalline semiconductor material of one conductivity type and to said region of opposite conductivity type.

3. A semiconductor device as claimed in claim 2 wherein when said p-n junction is reverse biased the resistive polycrystalline silicon film produces approximately parallel electric field lines in that portion of the



magnitude. If desired, silicon nitride passivation can be used over insulation 14 covering the junction.

Fig. 4a shows in cross-section an isometric view of a transistor constructed using the thin-film surface resistor of this invention. For illustrative convenience, the dimensions of this drawing are not to scale. Die or wafer 41 comprises a substrate of monocrystalline semiconductor material containing therein an n-type collector region 53 in which has been diffused a p-type base region 42 and an n-type emitter region 43. Alternatively, the conductivity-type of each region can be reversed if desired. Formed between the base and emitter regions is p-n junction 49 and between the base and collector regions is p-n junction 50. Depletion region 54 associated with p-n junction 50 extends primarily into the n-type collector region 53, which is more lightly doped than the p-type base region. Overlying the surface of the device is insulation layer 44, typically a thermally-grown oxide of silicon. Formed over insulation layer 44 is a layer 45 of polycrystalline silicon possessing a sheet resistivity of the order of 3×10^{10} ohms per square. Windows are etched through polycrystalline silicon layer 45 and oxide layer 44 to form contact regions to the underlying emitter, base, and collector regions. Contact to collector region 53 is made through a degenerate n^+ type region 52 formed on one surface of collector region 53. An equipotential ring 46 of conductive material contacts n^+ type region 52 and extends over polycrystalline silicon layer 45 toward field plate 47 contacting base region 42. If desired, ring 46 could be an extension of resistive material 45. Field plate 47, an extension of the contact to base region 42, extends on polycrystalline silicon layer 45 over the intersection of p-n junction 50 with the surface of monocrystalline silicon wafer 41. Contact 48 to emitter region 43 extends slightly on to oxide layer 44. No resistive material of the layer 45 is formed over oxide layer 44 overlying the intersection of p-n junction 49 with the surface of wafer 41 as this junction is forward biased during normal operation of the transistor. However, if desired the polycrystalline silicon can be left on oxide layer 44 over the base-emitter junction since this simplifies the processing steps and does not contribute significantly to emitter-base leakage current. Region 51 of the depletion region 54 is approximately linear with a slight upward concavity, as shown, due to the voltage distribution created by current through resistive layer 45. Transistors constructed using the principles of this invention had breakdown voltages BV_{CEO} in excess of 2,000 volts with an h_{FE} equal to or greater than 12. LV_{CEO} was about 1300 volts.

Fig. 4b shows an alternative embodiment of this invention wherein field plate 47 no

longer extends across the intersection of junction 50 with the surface of the device but rather terminates at the end of resistive layer 45. Plate 47 contacts p-type base region 42 and also contacts material of the layer 45 either at the end of material as shown by the portion of contact 47 represented by the continuous line, or at the end and top of region 45a of layer 45, as shown by section 47a of contact 47. In this embodiment region 45a is selectively doped to increase its conductivity. Region 45a thus, in effect, functions as a field plate and serves to shape the underlying depletion region associated with p-n junction 50. Region 45a does not have to cross the intersection of junction 50 with the semiconductor surface but to cross the intersection of junction 50 with the semiconductor surface but does have to come close to this intersection.

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WHAT WE CLAIM IS:—

1. A semiconductor device comprising monocrystalline semiconductor material of one conductivity type containing therein a region of opposite conductivity type with the pn junction between said monocrystalline semiconductor material and said region extending to one surface of said semiconductor material; insulation extending across the intersection of said pn junction with said surface; a field plate in contact with said region of said opposite conductivity type and extending on to the insulation to terminate adjacent to or to overlie the intersection of said pn junction with said one surface; and a resistive polycrystalline silicon film of approximately uniform thickness formed on top of and adherent to said insulation, said polycrystalline silicon film extending from said field plate to an electrode making contact with said monocrystalline semiconductor material.

2. A semiconductor device as claimed in claim 1 including means for applying selected potentials to said monocrystalline semiconductor material of one conductivity type and to said region of opposite conductivity type.

3. A semiconductor device as claimed in claim 2 wherein when said p-n junction is reverse biased the resistive polycrystalline silicon film produces approximately parallel electric field lines in that portion of the

depletion region beneath said field plate and said resistive polycrystalline silicon film.

5 4. A semi-conductor device as claimed in claim 1 wherein said resistive polycrystalline silicon film is formed on top of and is co-extensive with said insulation which extends across the intersection of said p-n junction with said one surface.

10 5. A semiconductor device as claimed in claim 4 wherein said field plate overlies, and is in conductive contact with, said resistive polycrystalline silicon.

15 6. semiconductor device as claimed in claim 1, 2, 3 or 4 wherein that portion of said resistive polycrystalline silicon film overlying on insulation the intersection of said p-n junction is doped with a selected impurity to form said field plate.

20 7. A semiconductor device as claimed in any preceding claim wherein said resistive

polycrystalline silicon film is a film possessing a sheet resistivity of the order of 3×10^{10} ohms per square.

8. A semiconductor device as claimed in any preceding claim wherein said one surface of said monocrystalline semiconductor material is planar. 25

9. A semiconductor device as claimed in any preceding claim wherein said monocrystalline semiconductor material is silicon. 30

10. A semiconductor device substantially as hereinbefore described with reference to Figure 3 or Figure 4a or Figure 4b of the accompanying drawings.

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