FIG. 1

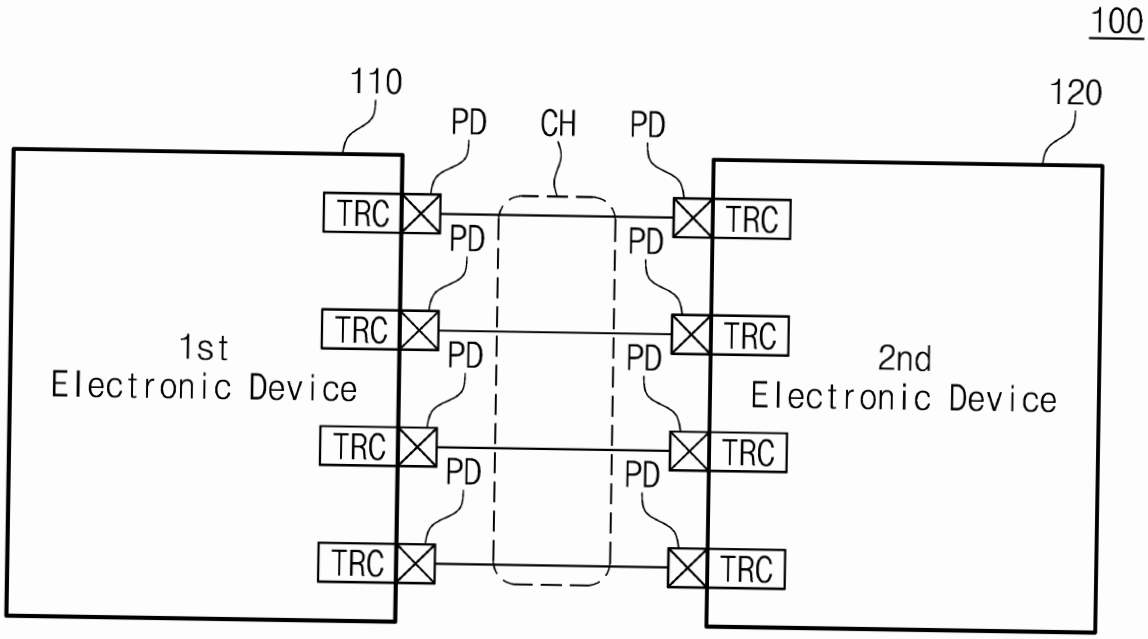

100
110
120
PD
CH
PD
TRC
TRC
PD
PD
TRC
TRC
1st
Electronic Device
PD
PD
2nd
Electronic Device
TRC
TRC
PD
PD
TRC
TRC

FIG. 2

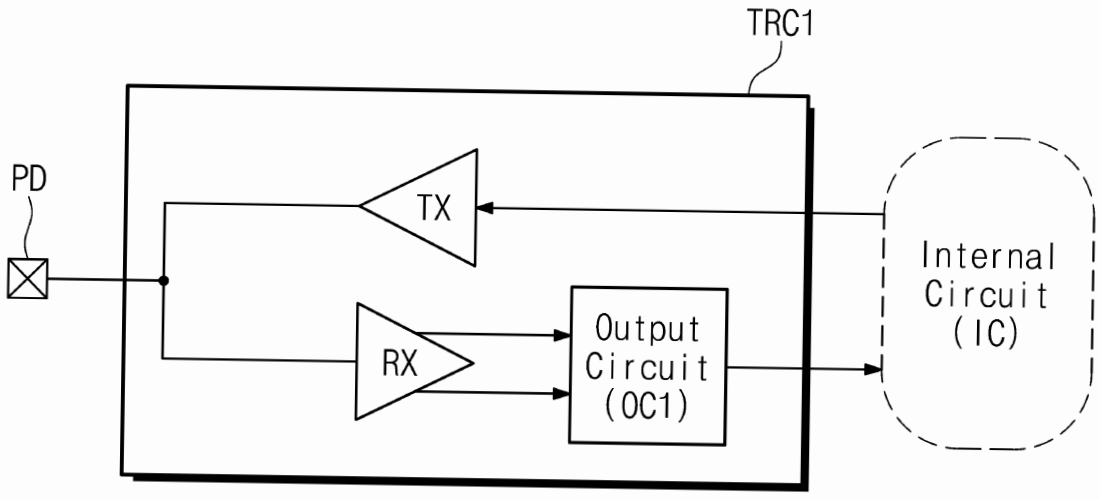

TRC1
PD
TX
RX
Output
Circuit
(OC1)
Internal
Circuit
(IC)

FIG. 3

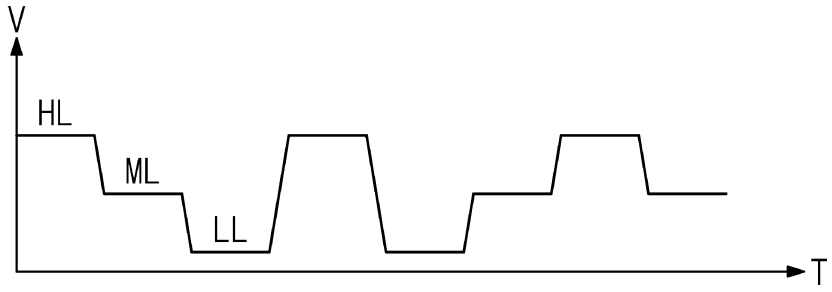


FIG. 4

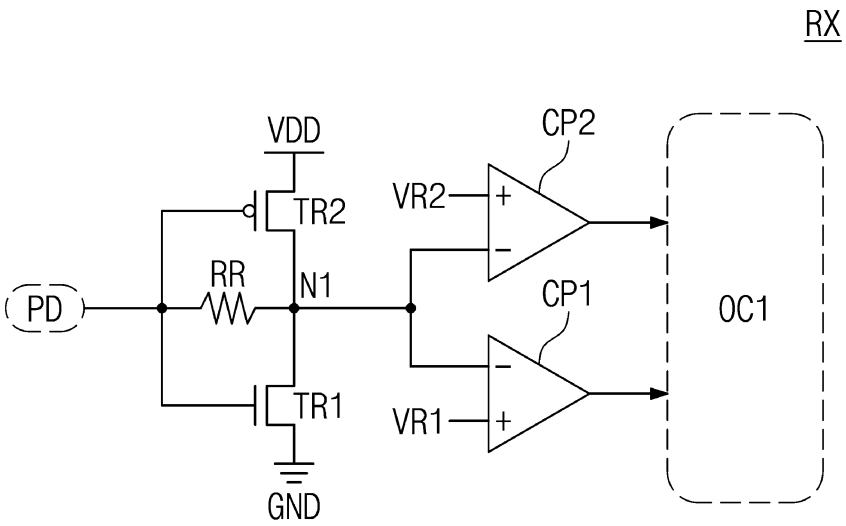


FIG. 5

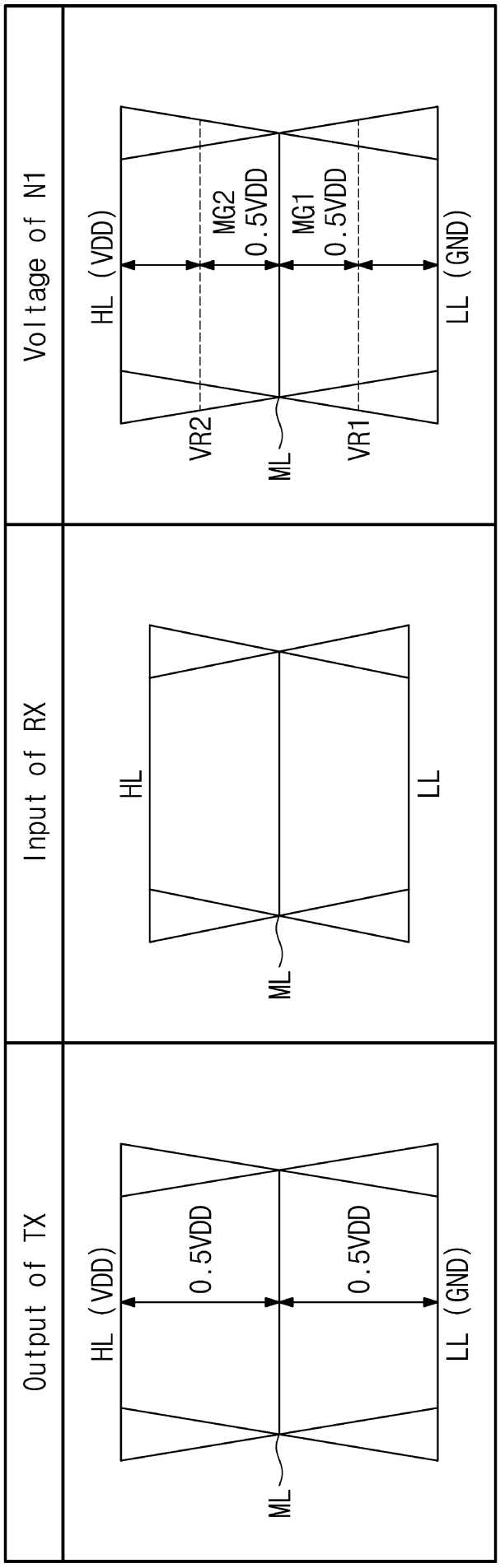

Output of TX
Input of RX
Voltage of N1
HL (VDD)
0.5VDD
0.5VDD
LL (GND)
ML
HL
LL
ML
HL (VDD)
MG2
0.5VDD
MG1
0.5VDD
LL (GND)
VR2
ML
VR1

FIG. 6

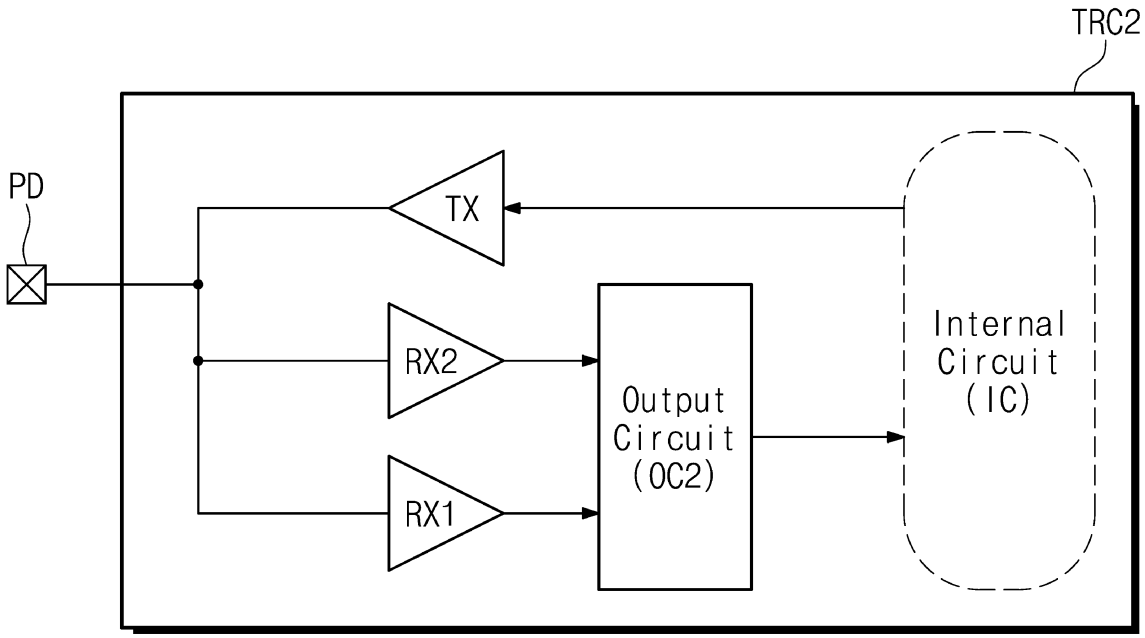

TRC2
PD
TX
RX2
RX1
Output
Circuit
(OC2)
Internal
Circuit
(IC)

FIG. 7

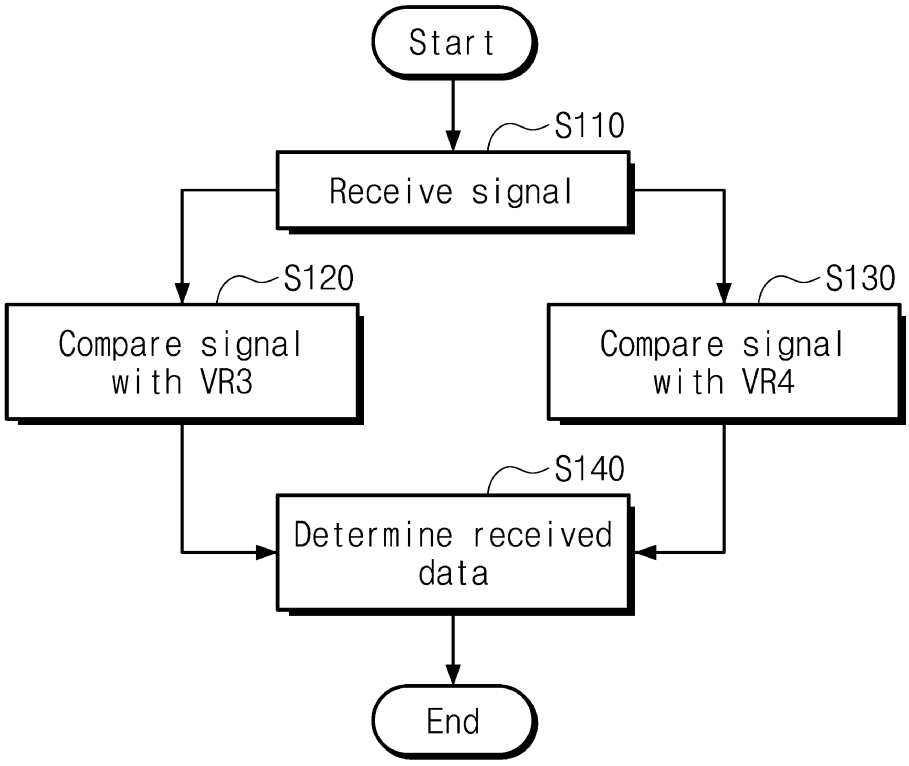

Start
S110
Receive signal
S120
Compare signal
with VR3
S130
Compare signal
with VR4
S140
Determine received
data
End

FIG. 8

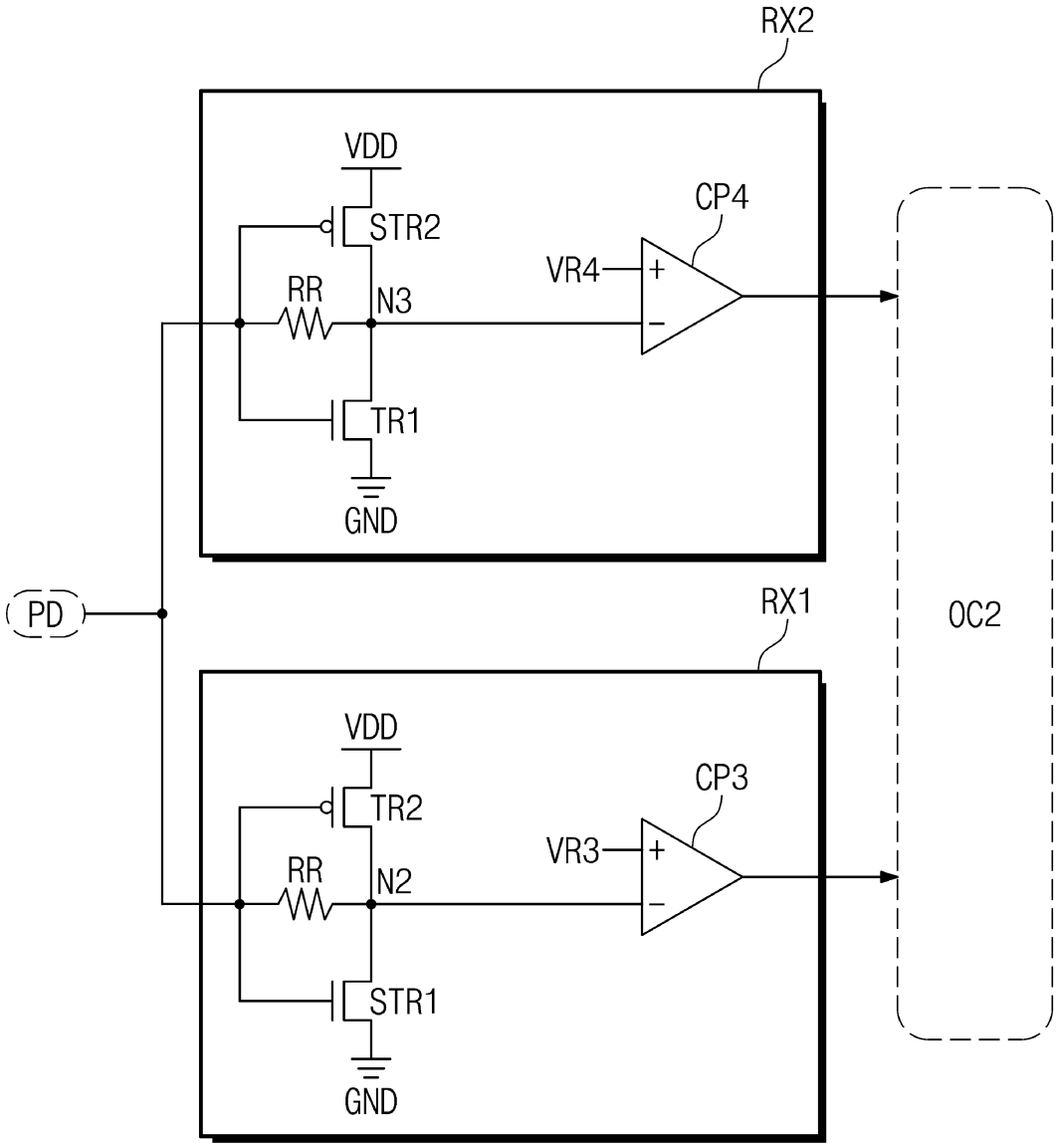

RX2
VDD
STR2
CP4
VR4
+
RR
N3
−
TR1
GND
PD
RX1
OC2
VDD
TR2
CP3
VR3
+
RR
N2
−
STR1
GND

FIG. 9

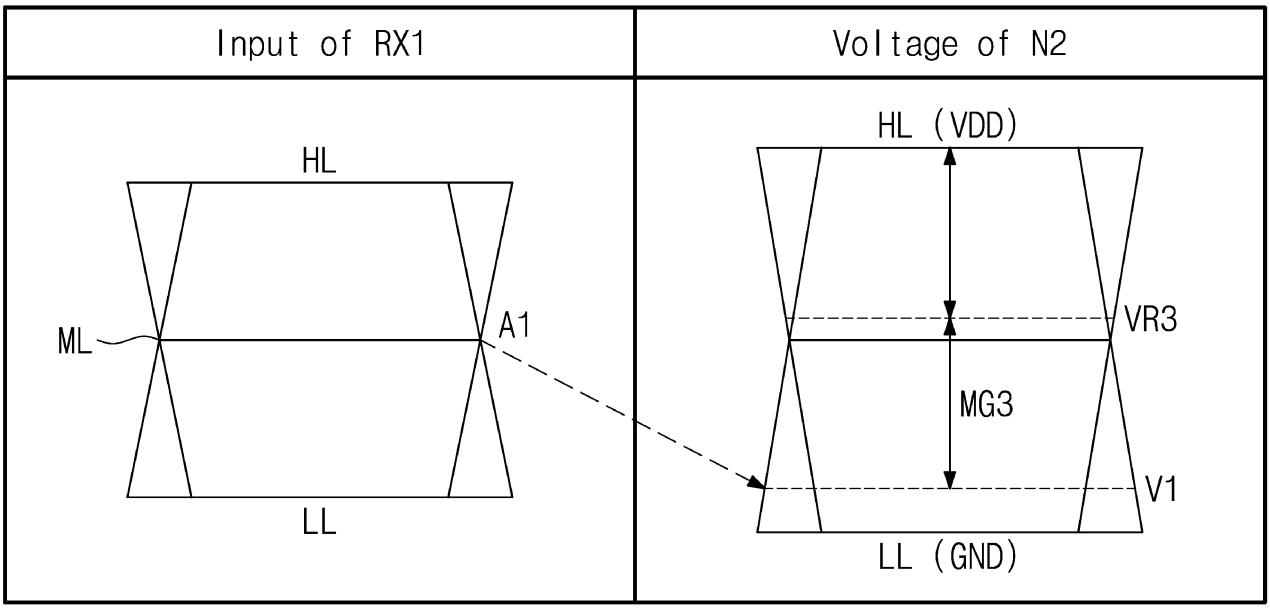

Input of RX1
Voltage of N2
HL
ML
A1
LL
HL (VDD)
VR3
MG3
V1
LL (GND)

FIG. 10

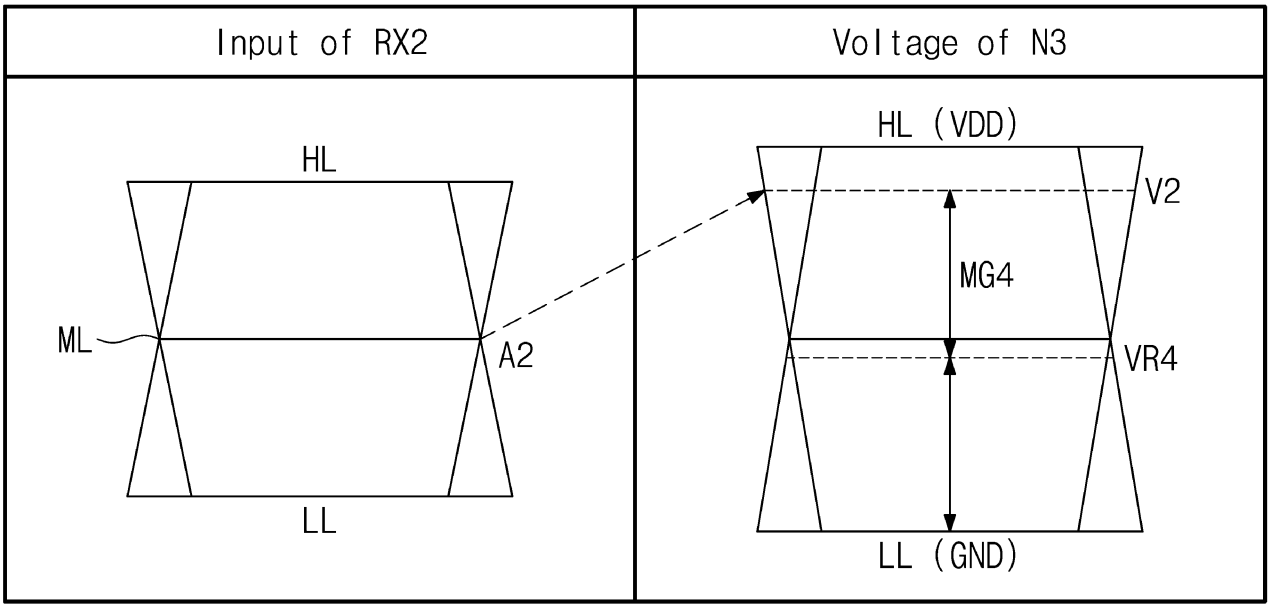

Input of RX2
Voltage of N3
HL
ML
A2
LL
HL (VDD)
V2
MG4
VR4
LL (GND)

FIG. 11

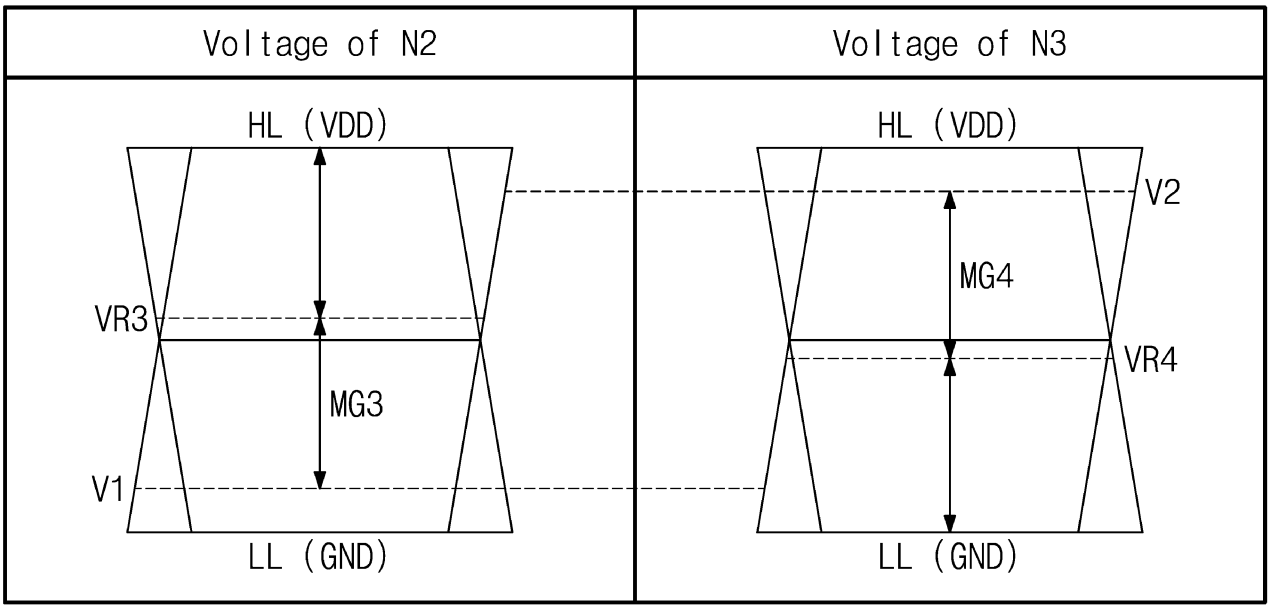

Voltage of N2
Voltage of N3
HL (VDD)
VR3
MG3
V1
LL (GND)
HL (VDD)
V2
MG4
VR4
LL (GND)

FIG. 12

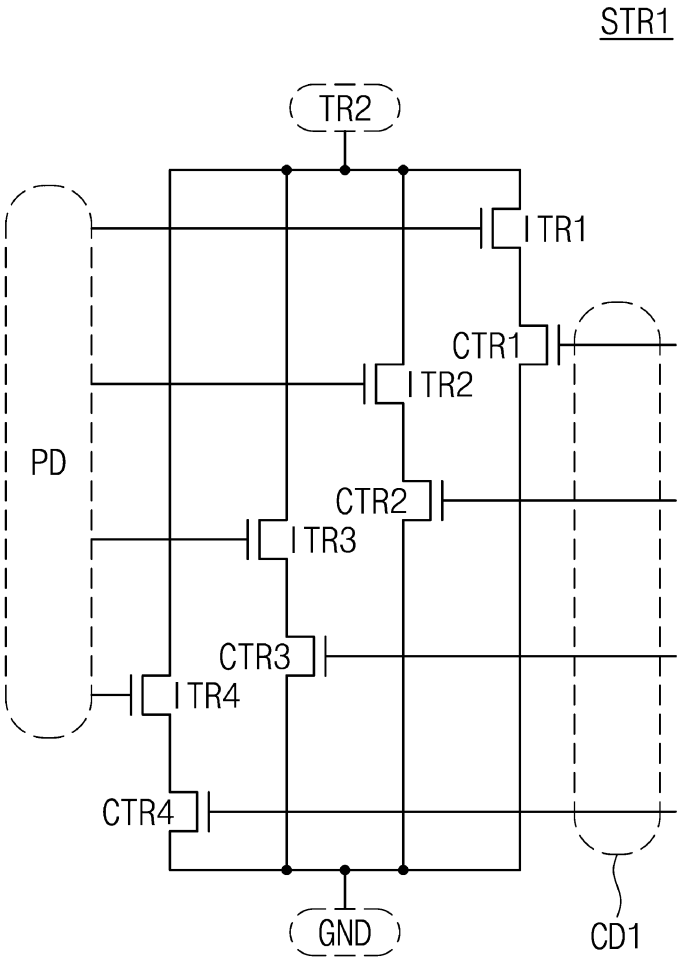


FIG. 13

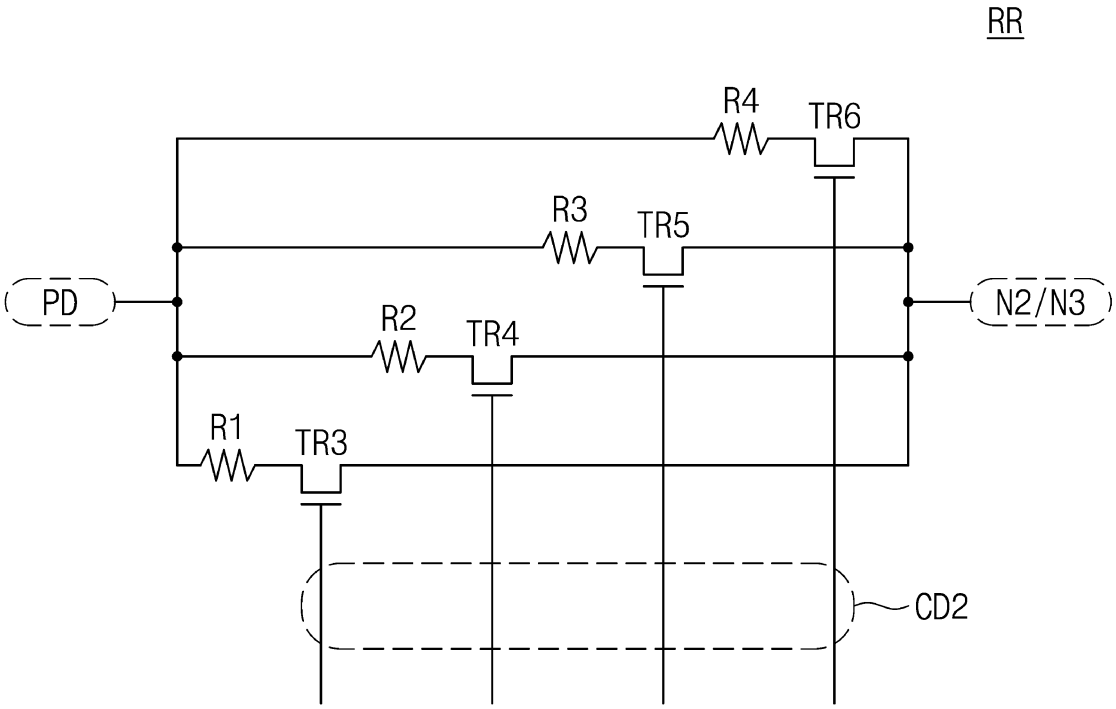

RR
R4
TR6
R3
TR5
PD
N2/N3
R2
TR4
R1
TR3
CD2

FIG. 14

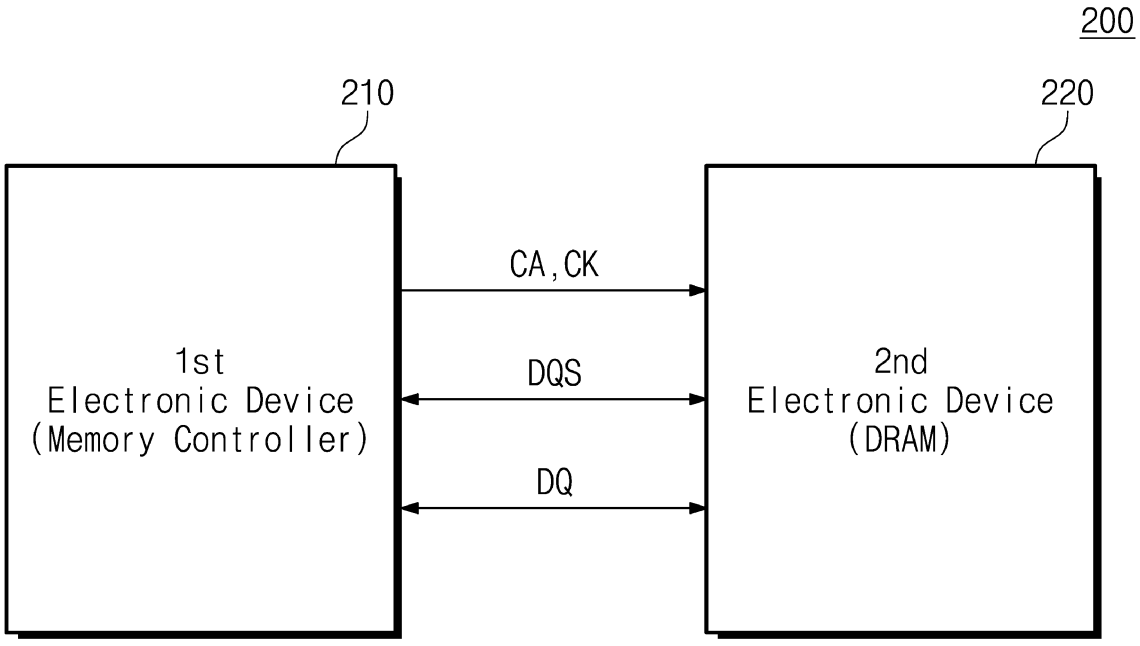

200
210
220
CA,CK
DQS
DQ
1st
Electronic Device
(Memory Controller)
2nd
Electronic Device
(DRAM)

FIG. 15

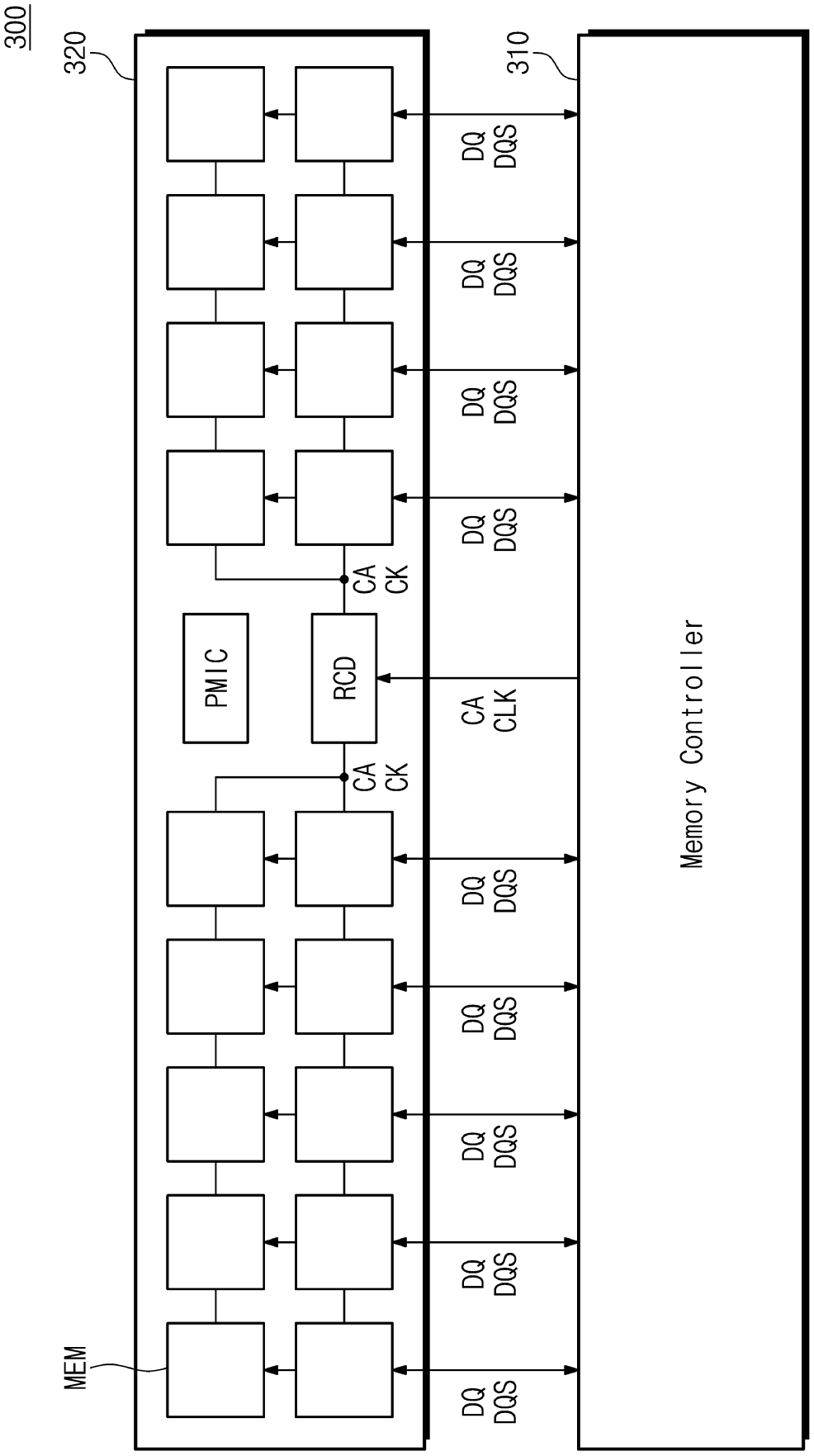
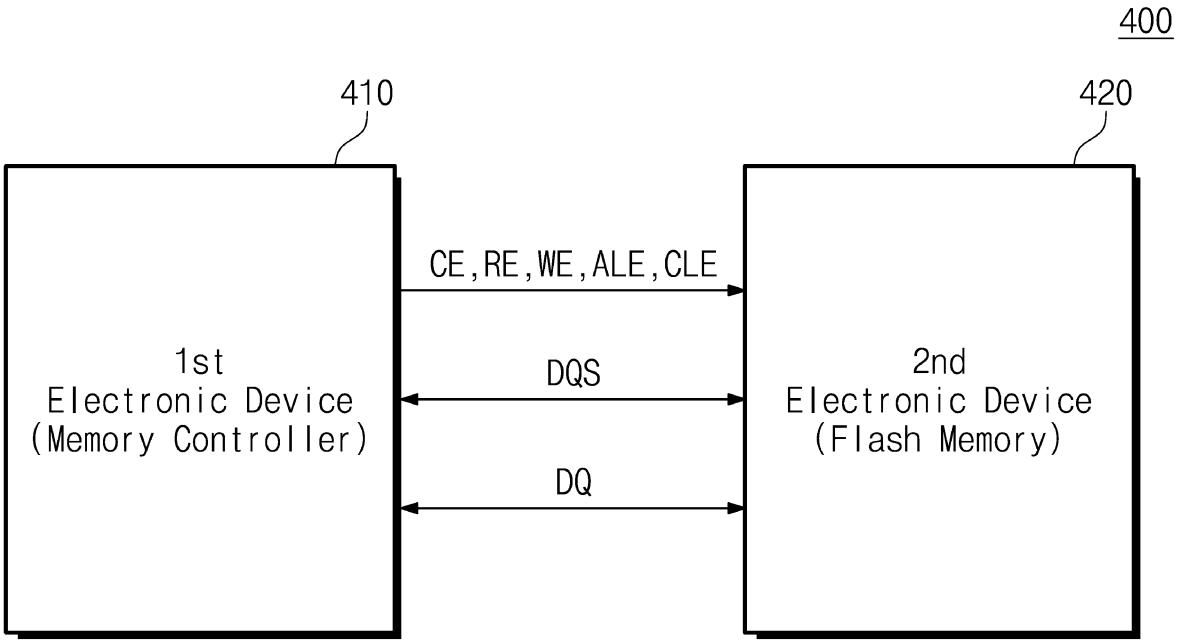


FIG. 16


400
410
420
1st
Electronic Device
(Memory Controller)
CE,RE,WE,ALE,CLE
DQS
DQ
2nd
Electronic Device
(Flash Memory)