Description

BACKGROUND OF THE INVENTION

This invention relates generally to integrated circuits and more particularly to a novel method of fabricating a semiconductor device in an integrated circuit by capping a conductive layer with a nitride layer during salicidation.

In recent years the advancement of very large scale integration ("VLSI") technology has resulted in a need to fit more and more individual semiconductor devices such as transistors into smaller and smaller areas of an integrated circuit chip. The dimensions of these devices have reached the submicron range, and it has become increasingly difficult to make adequate electrical contacts for interconnecting such devices.

A relatively recent development in the art of fabricating semiconductors has been the self-aligning silicide process ("salicidation"). During this process successive layers of a conductive material and silicon are deposited over a substrate and then are annealed at a high temperature, forming a conductive silicide layer which then can be utilized for the establishment of electrical contacts with the various regions of the device. This process offers numerous advantages including reduced parasitic resistance in gate, diffusion and interconnect areas of the device and improved circuit packing density.

Titanium is nearly always used as the conductive material because the annealing of titanium and silicon yields titanium silicide ($TiSi_2$) which is characterized by relatively low resistivity and good thermal stability and because of the ability of titanium to dissolve silicon native oxide during annealing to form silicide more consistently than other conductive materials.

Successful formation of titanium silicide is dependent on an absence of impurities between the titanium and the silicon. Any thin oxide or polymer residue left over from a previous step can prevent silicide formation. In addition, titanium reacts readily with any traces of oxygen that may be present. Oxygen contamination in the furnace must be less than about three parts per million ("PPM") in order to prevent such a titanium-oxygen reaction and permit the formation of titanium silicide to proceed reliably. This requires a leakproof system and a high rate of flow of very pure nitrogen gas during wafer loading and annealing, requirements which make the process costly to carry out and difficult to repeat.

Moreover, to successfully accomplish salicidation in a device having dimensions in the submicron range requires the solution of several other problems, among them minimizing drain-to-gate, source-to-gate, and junction leakage, preserving gate oxide integrity, and avoiding any adverse effects of dopant restribution or discontinuity of long polycides.

As a result of all these limitations, the depositing of the titanium and the subsequent high-temperature annealing are extremely difficult to control.

It has been proposed (Tang, T., C. C. Wei, R. Haken, H. Kawasaki, and R. Chapman in *Symposium on VLSI Technology* 1988, page 69; and US-A-4 657 628; US-A-4 701 349; US-A-4 690 730) to add a sacrificial dielectric cap layer after depositing the titanium and strip back after sintering. However, the etch back process which must be performed as part of this techique has created many device and process complexities.

From the foregoing it will be apparent that there remains a need for a practical way to obtain the benefits of salicidation during fabrication of a semiconductor device.

SUMMARY OF THE INVENTION

The present invention provides a method of realizing the benefits of the self-aligning silicide process in fabricating a semiconductor device by capping a conductive layer with a nitride prior to annealing. The resulting structure is relatively immune from any adverse effects of the presence of oxygen or other contaminants during the deposit of the conductive layer and the subsequent annealing and therefore gives improved yield while reducing the cost of fabrication.

Briefly and in general terms, the invention is embodied in a method of fabricating a semiconductor device by means of the following steps: forming field oxide regions in a planar surface of a substrate; creating a gate region between the oxide regions; forming source and drain diffusion regions in the substrate; covering the substrate with a conductive layer such as titanium; covering the conductive layer with a nitride such as titanium nitride; annealing at a relatively low temperature to form a silicon compound wherever the conductive material is touching silicon and to combine any remaining conductive material with the nitride to form a generally homogeneous layer of nitride covering the device; etching to remove the nitride; and annealing at a relatively high temperature to convert the silicon compound into a silicide.

Preferably the nitride is deposited immediately after the conductive material, for example by reactive sputtering, without any change in ambient atmosphere. The ambient atmosphere is preferably nitrogen.

The etching preferably comprises wet etching, for example with sulfuric acid or ammonium hydroxide.

The gate region is created, for example, by forming a gate oxide layer on the substrate and forming a silicon pad on the gate oxide layer. The diffusion regions are formed, for example, by coating the pad and the substrate with a dielectric layer, directionally etching the dielectric layer to provide oxide spacers around the pad, and performing ion implantation and drive-in to form the diffusion regions. The pad itself can be formed by depositing a polysilicon layer over the gate oxide layer and then etching the polysilicon and the underlying gate oxide.

Other aspects and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is an enlarged sectional view of a semiconductor device being fabricated according to the method of the invention after the step of forming field oxide regions and including a gate oxide layer therebetween;

FIG. 2 shows the device of FIG. 1 after forming a polysilicon layer over the field and gate oxide regions;

FIG. 3 shows the device of FIG. 2 after etching the polysilicon layer and the gate oxide layer to form a gate region;

FIG. 4 shows the device of FIG. 3 after forming source and drain regions;

FIG. 5 shows the device of FIG. 4 after covering with a conductive layer;

FIG. 6 shows the device of FIG. 5 after covering with a nitride layer;

FIG. 7 shows the device of FIG. 6 after annealing at a low temperature; and

FIG. 8 shows the device of FIG. 7 after etching to remove the nitride and annealing at a high temperature.

DESCRIPTION OF THE PREFERRED EMBODIMENT

As shown in the drawings for purposes of illustration, the invention is embodied in a method of fabricating a semiconductor device by capping a conductive layer with a nitride layer during salicidation.

There has been a continuing effort to fit more and more semiconductor devices onto an integrated circuit chip. As the dimensions of these devices have become smaller, it has become more and more difficult to fabricate adequate electrical connections with the devices. Forming such contacts by salicidation offers numerous benefits, but it has been difficult to achieve consistent results due to the extreme vulnerability of this process to the effects of very small concentrations of impurities and the need to solve various other problems associated with salicidation.

During salicidation, a layer of conductive material such as titanium is deposited over a partially-formed semiconductor device. According to the method of the present invention, this conductive layer is covered with titanium nitride rather than silicon, a low temperature anneal is performed, and any excess nitride is etched away. A high temperature anneal completes the salicidation. This novel process results in the formation of a smoother and thicker layer of titanium silicide than existing methods of salicidation and is easier to carry out because it is relatively immune from any adverse effects of impurities.

More particularly, FIGURES 1 through 8 illustrate successive stages of the fabrication of a semiconductor device according to a preferred embodiment of the method of the invention. Spaced-apart first and second field oxide regions 11 and 13 are formed in a planar surface 15 of a substrate 17, and a gate region generally designated 19 is created between the field oxide regions 11 and 13.

The gate region 19 is preferably created by forming a gate oxide layer 21 in the planar surface 15 of the substrate 17 and forming a silicon pad 23 on the gate oxide layer 21 to create the gate region 19. The silicon pad 23 is formed, for example, by forming a polysilicon layer 25 over the gate oxide 21 and then etching the polysilicon layer 25 and the underlying gate oxide 21, a portion 27 of the gate oxide layer 21 remaining under the silicon pad 23 after this etching.

Next a source diffusion region 29 is formed between the gate region 19 and the first field oxide region 11, and a drain diffusion region 31 is formed between the gate region 19 and the second field oxide region 13. The diffusion regions 29 and 31 are preferably formed by coating the pad 23 and the substrate 17 with a dielectric layer, directionally etching the dielectric layer to provide oxide spacers 33 and 35 around the pad 23, and performing ion implantation and drive-in to form the diffusion regions 29 and 31.

Then the device is covered with a conductive layer 37 such as titanium, and the conductive layer 37 in turn is covered with a nitride layer 39 such as titanium nitride. The nitride layer 39 is preferably reactively sputtered on immediately after deposition of the conductive layer 37 without breaking vacuum or changing the ambient atmosphere.

The next step is annealing at a relatively low temperature whereby those portions of the conductive layer 37 which overlie silicon react therewith to form a conductive silicon compound such as a titanium silicon compound of the form $TiNi_x$ and any remaining portions of the conductive layer 37 react with the nitride layer 39 to form a generally homogeneous nitride layer 41 covering the device, as best shown in FIG. 7.

More particularly, that portion of the conductive layer 37 which immediately overlies the source region 29 reacts with the silicon at the surface 15 of the substrate 17 to form a conductive layer 43 of silicon compound on the source region 29. Similarly, a conductive layer 45 of silicon compound is formed on the drain region 31 and a conductive layer 47 of silicon compound is formed on the pad 23.

Then the nitride layer 41 is removed by etching, preferably in a wet etch by means of a solution of sulfuric acid, ammonium hydroxide or the like. The solution preferably includes hydrogen peroxide, for example in a ratio of two parts of sulfuric acid to one part of hydrogen peroxide.

Finally, a second annealing at a relatively high temperature converts the layers 43, 45 and 47 into silicide (such as titanium silicide $TiNi_2$) layers 49, 51 and 53, respectively.

The nitride layer 39 plays several important roles during the first anneal. One, it prevents the titanium (or other conductive material) of which the layer 37 is comprised from reacting with the ambient nitrogen atmosphere. This forces the titanium to dissolve any oxide residue which may have formed on the surface of the device prior to deposition of the layer 37 and "snow-plow" the oxygen from the residue into the nitride layer 41. Then this unwanted oxygen is removed when the nitride is etched away.

Another role played by the nitride layer 39 is to force that portion of the titanium which is immediately adjacent the silicon surfaces to react therewith to form the silicide, thereby alleviating the strict requirements of titanium-silicon interface cleanliness.

In addition, silicide formation according to the method of the invention is much less subject to adverse effects of oxygen contamination of the ambient atmosphere during high temperature annealing. Whereas conventional salicidation requires an atmosphere having less than about three PPM of oxygen, the method of the invention works even if oxygen is present in amounts of 10,000 PPM. Residue oxide dissolubility can be as much as about 75 Angstroms (10 Angstroms = 1nm) as opposed to 35 Angstroms for conventional salicidation.

The titanium silicide which results from the process of the invention is smoother and thicker than that which can be obtained by conventional methods. Surface morphology of titanium silicide formed by the method of the invention is about 50 Angstroms as opposed to 1,500 Angstroms when formed by conventional methods. The interface roughness between the titanium silicide and the underlying silicon, for example the source and drain regions 43 and 45, is about 20 Angstroms in opposed to 200 Angstroms in devices formed in other ways.

Not only can semiconductor devices be fabricated more reliably and less expensively according to the method of the invention, but in addition the electrical parameters of devices fabricated according to the invention have been found to be significantly superior to those of conventionally-made devices, as can be seen by reference to the following Table 1:

Parameter	Invention	Conventional
Field leakage current (amps)	1e-11	8e-10
N-Well leakage current (amps)	2e-10	2e-9
Substrate leakage current (amps)	2e-11	5e-7
NMOS G/S,D leakage current (amps)	5e-12	2e-10
PMOS G/S,D leakage current (amps)	1e-11	5e-9
Area gate cap leakage current (amps)	6e-10	3e-10
Peri gate cap leakage current (amps)	2e-10	5e-9
Drain saturation current (amps)	7.3e-3	7.2e-3
N+ island Rs (ohm/sq)	1.6	2.8
P+ island Rs (ohm/sq)	1.4	2.4
N+ poly Rs (ohm/sq)	1.9	3.6
PMOS series resistance (ohms)	90	400
NMOS series resistance (ohms)	50	48

TABLE 1
Comparison of Silicide-Related Electrical Parameters

From the foregoing it will be apparent that the present invention provides a novel method of fabricating a semiconductor device by capping a conductive layer with a nitride layer prior to annealing during the formation of conductive silicides. Fabrication of semiconductor devices according to the method of the invention is more reliable, consistent and economical than is fabrication according to other methods. Titanium silicides formed according to the invention are thicker and smoother than those formed by other means, and semiconductor devices having such silicides have superior electrical characteristics.

Claims

1. A method of fabricating a semiconductor device, comprising the steps of
forming spaced-apart first and second field oxide regions (11,13) in a planar surface of a substrate (17);
creating a gate region (19) between the field oxide regions;
forming a source diffusion region (29) between the gate region (19) and the first field oxide region (11) and a drain diffusion region (31) between the gate region (19) and the second field oxide region (13);
covering the substrate with a conductive layer (37);
characterized by the further steps of
covering the conductive layer with a nitride layer (39);
annealing at a relatively low temperature whereby those portions of the conductive layer (37) which overlie silicon react therewith to form a silicon compound and any remaining portions of the conductive layer (37) react with the nitride layer (39) to form a generally homogeneous nitride layer covering the device;
etching to remove the nitride layer (39); and annealing at a relatively high temperature to convert the silicon compound into a silicide.

2. A method according to claim 1, **characterized** in that the conductive layer (37) comprises titanium and the nitride layer (39) comprises titanium nitride.

3. A method according to claim 2, **characterized** in that the titanium nitride coating is applied immediately after the titanium coating without any change in ambient atmosphere.

4. A method according to one of claims 1 to 3, **characterized** in that the etching comprises wet etching.

5. A method according to claim 4, **characterized** in that the wet etching is performed by means of sulfuric acid.

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N+ island Rs (ohm/sq)	1.6	2.8
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creating a gate region (19) between the field oxide regions;
forming a source diffusion region (29) between the gate region (19) and the first field oxide region (11) and a drain diffusion region (31) between the gate region (19) and the second field oxide region (13);
covering the substrate with a conductive layer (37);
characterized by the further steps of
covering the conductive layer with a nitride layer (39);
annealing at a relatively low temperature whereby those portions of the conductive layer (37) which overlie silicon react therewith to form a silicon compound and any remaining portions of the conductive layer (37) react with the nitride layer (39) to form a generally homogeneous nitride layer covering the device;
etching to remove the nitride layer (39); and annealing at a relatively high temperature to convert the silicon compound into a silicide.

2. A method according to claim 1, **characterized** in that the conductive layer (37) comprises titanium and the nitride layer (39) comprises titanium nitride.

3. A method according to claim 2, **characterized** in that the titanium nitride coating is applied immediately after the titanium coating without any change in ambient atmosphere.

4. A method according to one of claims 1 to 3, **characterized** in that the etching comprises wet etching.

5. A method according to claim 4, **characterized** in that the wet etching is performed by means of sulfuric acid.

6. A method according to claim 4, **characterized** in that the wet etching is performed by means of ammonium hydroxide.

7. A method according to one of the preceding claims, **characterized** in that the step of creating a gate region (19) comprises forming a gate oxide layer (21) in the planar surface (15) of the substrate (17) and forming a silicon pad (23) on the gate oxide layer to create the gate region.

8. A method according to claim 7, **characterized** in that the step of forming the diffusion regions (29,31) comprises:
coating the pad and the substrate with a dielectric layer;
directionally etching the dielectric layer to provide oxide spacers (33,35) around the pad (23); and performing ion implantation and drive-in to form the diffusion regions.

9. A method according to claim 7, **characterized** in that the step of forming the pad (23) comprises forming a polysilicon layer (25) over the gate oxide (21) and then etching the polysilicon layer and the underlying gate oxide.

Patentansprüche

1. Verfahren zum Herstellen einer Halbleitervorrichtung, welches die folgenden Schritte umfaßt:
Bilden von voneinander abgesetzten ersten und zweiten Feldoxidbereichen (11, 13) in einer ebenen Oberfläche eines Substrats (17),
Bilden eines Gatebereichs (19) zwischen den Feldoxidbereichen, Bilden eines Source-Diffusionsbereichs (29) zwischen dem Gatebereich (19) und dem ersten Feldoxidbereich (11) und eines Drain-Diffusionsbereichs (31) zwischen dem Gatebereich (19) und dem zweiten Feldoxidbereich (13),
Bedecken des Substrats mit einer leitenden Schicht (37), gekennzeichnet durch die weiteren Schritte:
Bedecken der leitenden Schicht mit einer Nitridschicht (39), Tempern bei einer relativ geringen Temperatur, wodurch die Teile der leitenden Schicht (37), welche Silicium überlagern, mit diesem reagieren, um eine Siliciumverbindung zu bilden, und alle restlichen Teile der leitenden Schicht (37) mit der Nitridschicht (39) reagieren, um eine allgemein homogene Nitridschicht zu bilden, welche die Vorrichtung überdeckt, Ätzen zum Entfernen der Nitridschicht (39) und
Tempern bei einer relativ hohen Temperatur, um die Siliciumverbindung in ein Silicid umzuwandeln.

2. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß die leitende Schicht (37) Titan enthält und die Nitridschicht (39) Titannitrid enthält.

3. Verfahren nach Anspruch 2, dadurch gekennzeichnet, daß die Titannitrid-Beschichtung unmittelbar nach der Titan-Beschichtung ohne eine Änderung der Umgebungsatmosphäre aufgebracht wird.

4. Verfahren nach einem der Ansprüche 1 bis 3, dadurch gekennzeichnet, daß das Ätzen Naßätzen umfaßt.

5. Verfahren nach Anspruch 4, dadurch gekennzeichnet, daß das Naßätzen mit Hilfe von Schwefelsäure durchgeführt wird.

6. Verfahren nach Anspruch 4, dadurch gekennzeichnet, daß das Naßätzen mit Hilfe von Ammoniumhydroxid durchgeführt wird.

7. Verfahren nach einem der Vorangehenden Ansprüche, dadurch gekennzeichnet, daß der Schritt des Erzeugens eines Gatebereichs (19) das Bilden einer Gateoxid-Schicht (21) in der ebenen Oberfläche (15) des Substrats (17) und das Bilden eines Siliciumflecks (23) auf der Gateoxid-Schicht umfaßt, um den Gatebereich zu bilden.

8. Verfahren nach Anspruch 7, dadurch gekennzeichnet, daß der Schritt des Bildens der Diffusionsbereiche (29, 31) umfaßt: Beschichten des Flecks und des Substrats mit einer dielektrischen Schicht, gerichtetes Ätzen der dielektrischen Schicht, um Oxid-Abstandshalter (33, 35) um den Fleck (23) herum zu schaffen, und Durchführen einer Ionenimplantation und -diffusion, um die Diffusionsbereiche zu bilden.

9. Verfahren nach Anspruch 7, dadurch gekennzeichnet, daß der Schritt des Bildens des Flecks (23) das Bilden einer Polysiliciumschicht (25) über dem Gateoxid (21) und das nachfolgende Ätzen der Polysiliciumschicht und des darunterliegenden Gateoxids umfaßt.

Revendications

1. Procédé de fabrication d'un dispositif semi-conducteur, comprenant les étapes consistant à :
   - former des première et seconde zones d'oxyde de champ (11, 13) espacées l'une de l'autre dans une surface plane d'un substrat (17) ;
   - créer une zone de grille (19) entre les zones d'oxyde de champ ;
   - former une zone de diffusion de source (29) entre la zone de grille (19) et la première zone d'oxyde de champ (11) ainsi qu'une zone de diffusion de drain (31) entre la zone de grille (19) et la seconde zone d'oxyde de champ (13) ;
   - couvrir le substrat d'une couche conductrice (37) ; procédé caractérisé par les autres étapes consistant à :
   - couvrir la couche conductrice avec une couche de nitrure (39) ;
   - effectuer un recuit à une température relativement basse de façon que les parties de la couche conductrice (37) qui recouvrent le silicium réagissent avec lui pour former un composé de silicium et que toutes les parties restantes de la couche conductrice (37) réagissent avec la couche de nitrure (39) pour former une couche de nitrure homogène dans l'ensemble et couvrant le dispositif;
   - effectuer une gravure pour enlever la couche de nitrure (39) ; et
   - effectuer un recuit à une température relativement haute pour convertir le composé de silicium en un siliciure.

2. Procédé selon la revendication 1, caractérisé en ce que la couche conductrice (37) contient du titane et la couche de nitrure (39) contient du nitrure de titane.

3. Procédé selon la revendication 2, caractérisé en ce que le revêtement de nitrure de titane est déposé immédiatement après le revêtement de titane sans aucun changement dans l'atmosphère ambiante.

4. Procédé selon une des revendications 1 à 3, caractérisé en ce que la gravure comprend une gravure en voie humide.

5. Procédé selon la revendication 4, caractérisé en ce que la gravure en voie humide est effectuée au moyen d'acide sulfurique.

6. Procédé selon la revendication 4, caractérisé en ce que la gravure en voie humide est effectuée au moyen d'hydroxyde d'ammonium.

7. Procédé selon une des revendications précédentes, caractérisé en ce que l'étape de création d'une zone de grille (19) consiste à former une couche d'oxyde de grille (21) dans la surface plane (15) du substrat (17) et à former un plot de silicium (23) sur la couche d'oxyde de grille pour créer la zone de grille.

8. Procédé selon la revendication 7, caractérisé en ce que l'étape de formation des zones de diffusion (29, 31) consiste à :
   - recouvrir le plot et le substrat d'une couche diélectrique ;
   - effectuer une gravure directionnelle de la couche diélectrique pour former des espaceurs d'oxyde (33, 35) autour du plot (23) ; et
   - effectuer une implantation et une redistribution d'ions pour former des zones de diffusion.

9. Procédé selon la revendication 7, caractérisé en ce que l'étape de formation du plot (23) consiste à former une couche de polysilicium (25) sur l'oxyde de grille (21) puis à effectuer la gravure de la couche de polysilicium et de l'oxyde de grille sous-jacent.