

ABSTRACT OF THE DISCLOSURE

An interface device between a plurality of memory devices and a memory controller includes processing circuitry configured to provide a plurality of controller channels for communicating with the memory controller, to provide a plurality of memory channels for communicating with the plurality of memory devices, and to connect each of the plurality of controller channels to at least one of the plurality of memory channels in a first mode and disconnect the plurality of controller channels from the plurality of memory channels in a second mode.

FIG. 1