

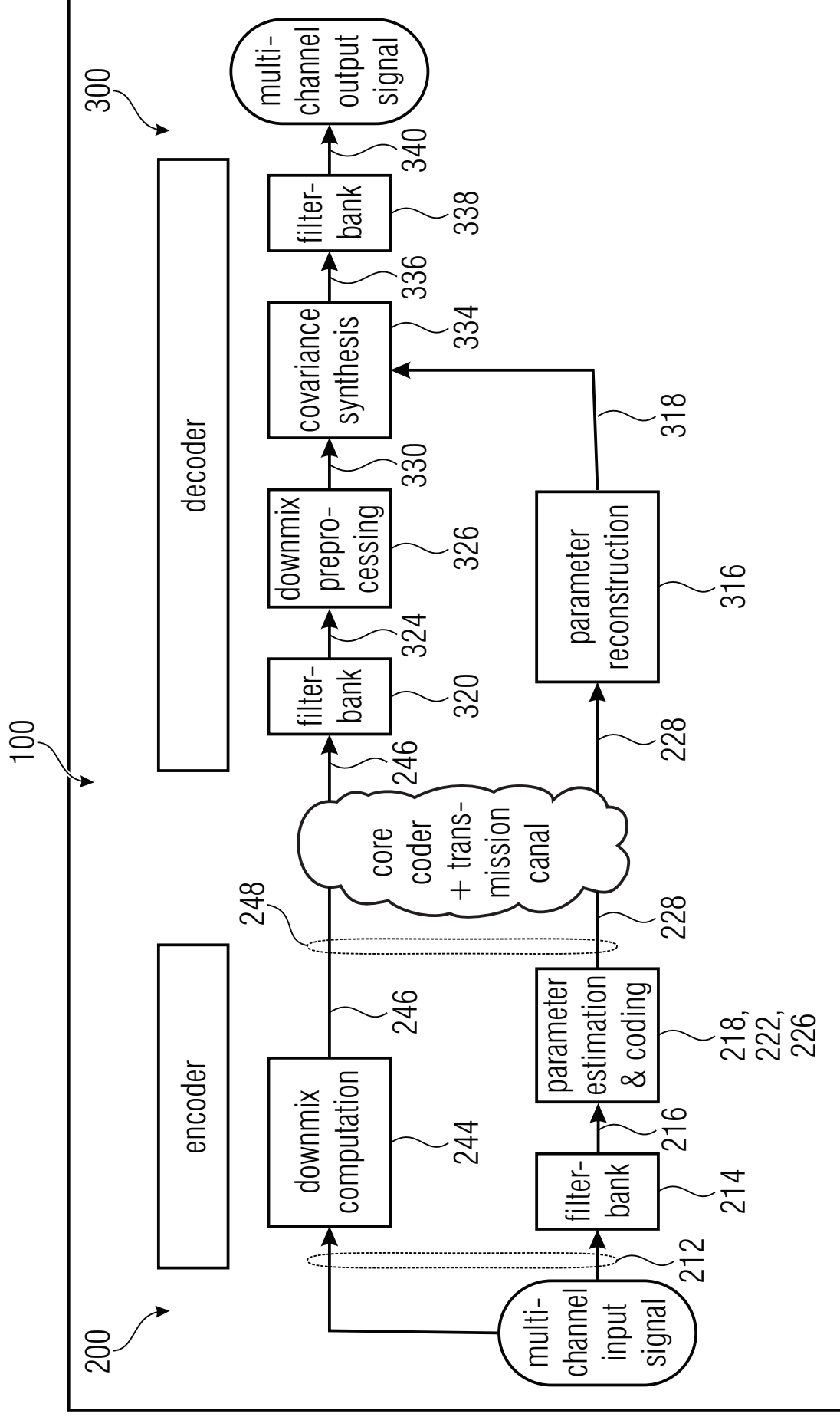


Fig. 1
simplified overview of the whole processing

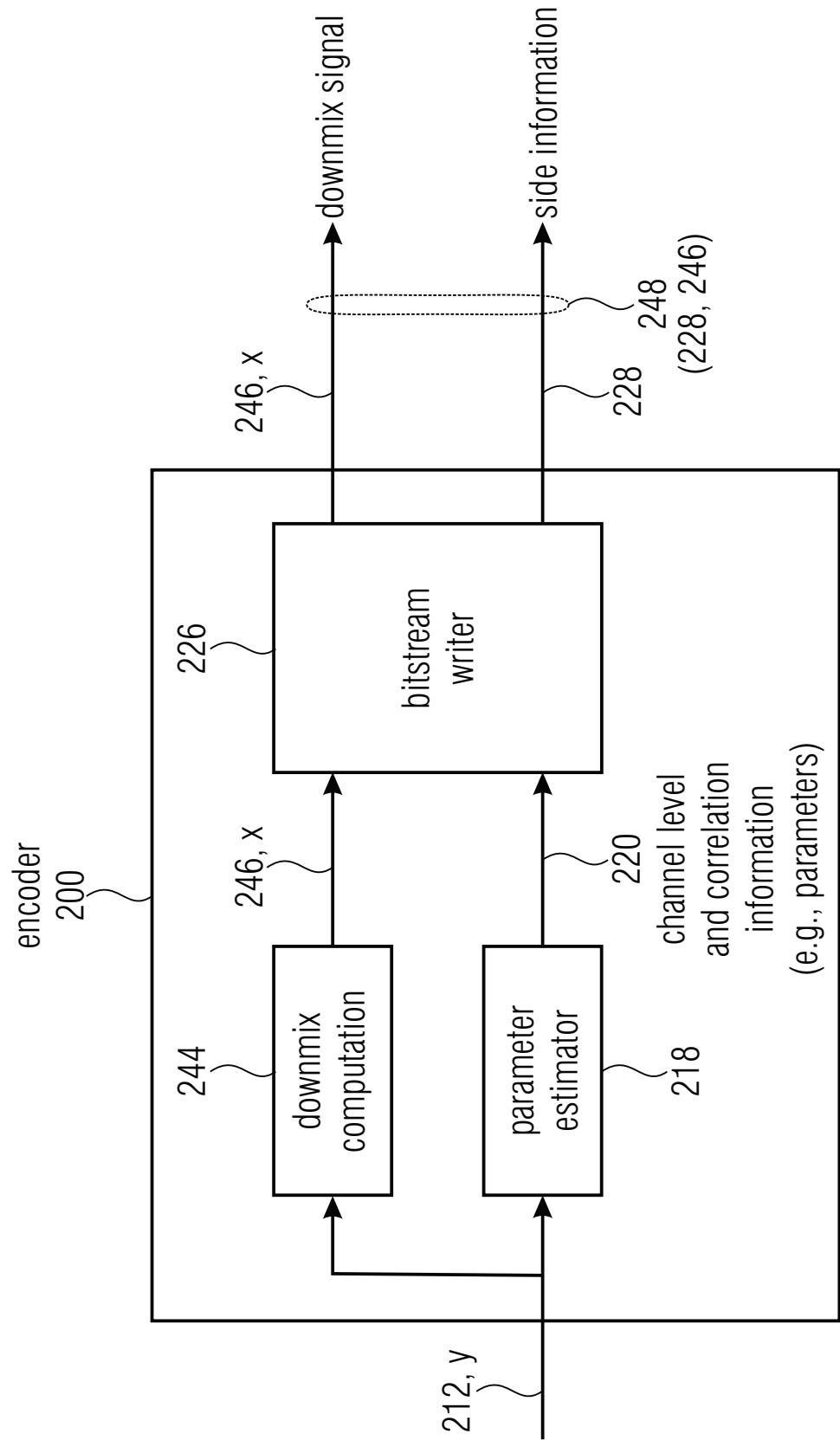


Fig. 2a

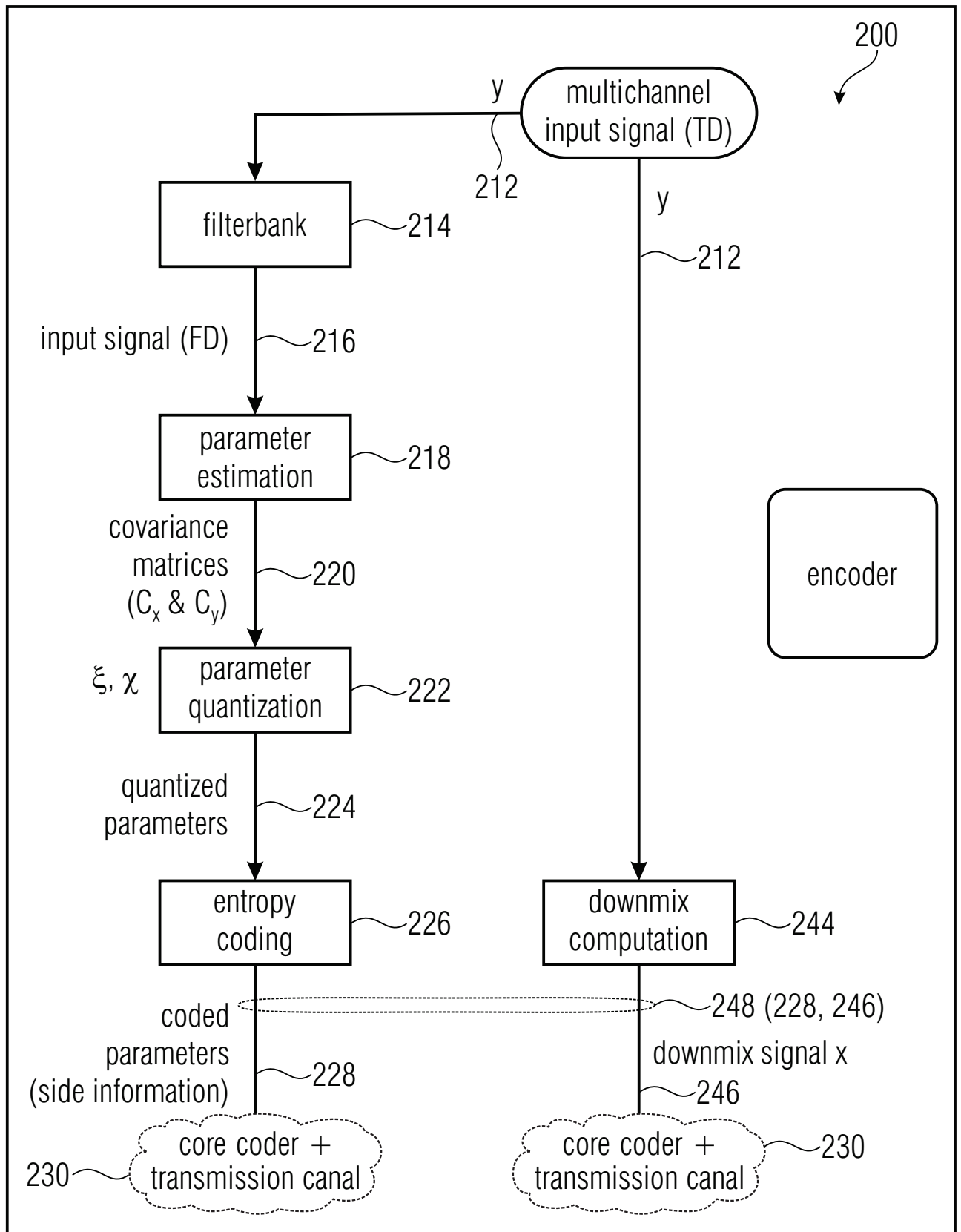


Fig. 2b
detailed overview of encoder

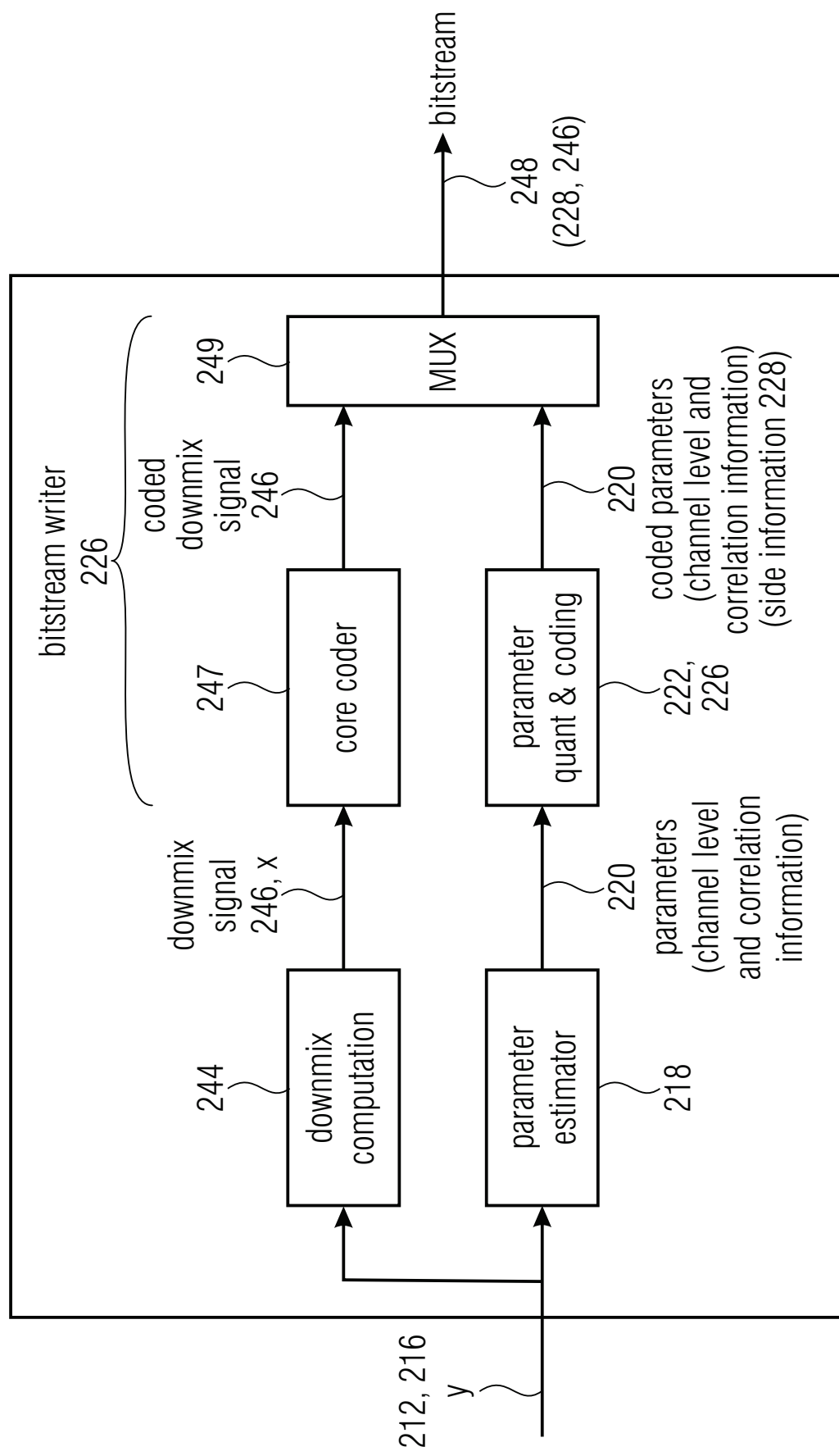


Fig. 2c

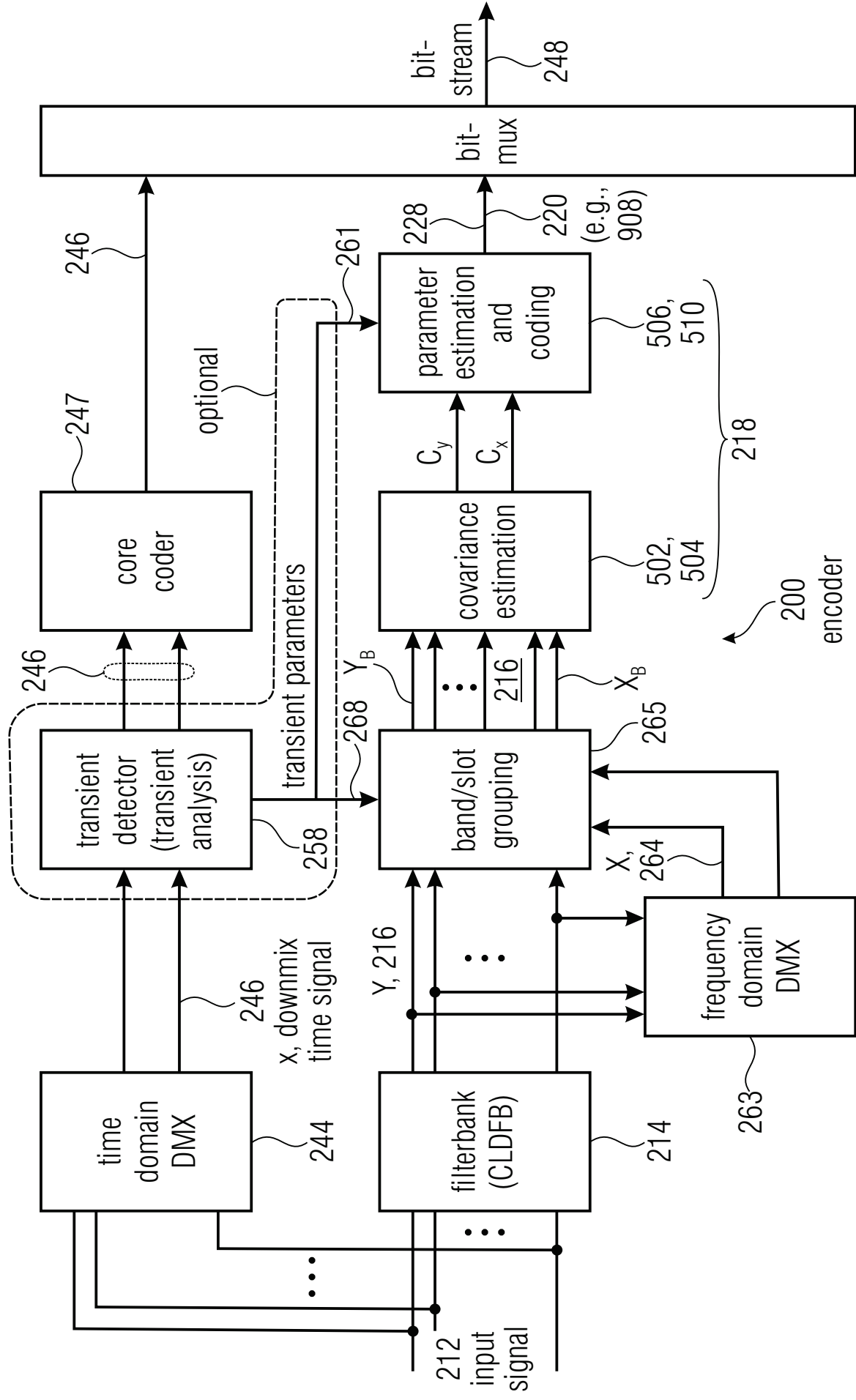


Fig. 2d

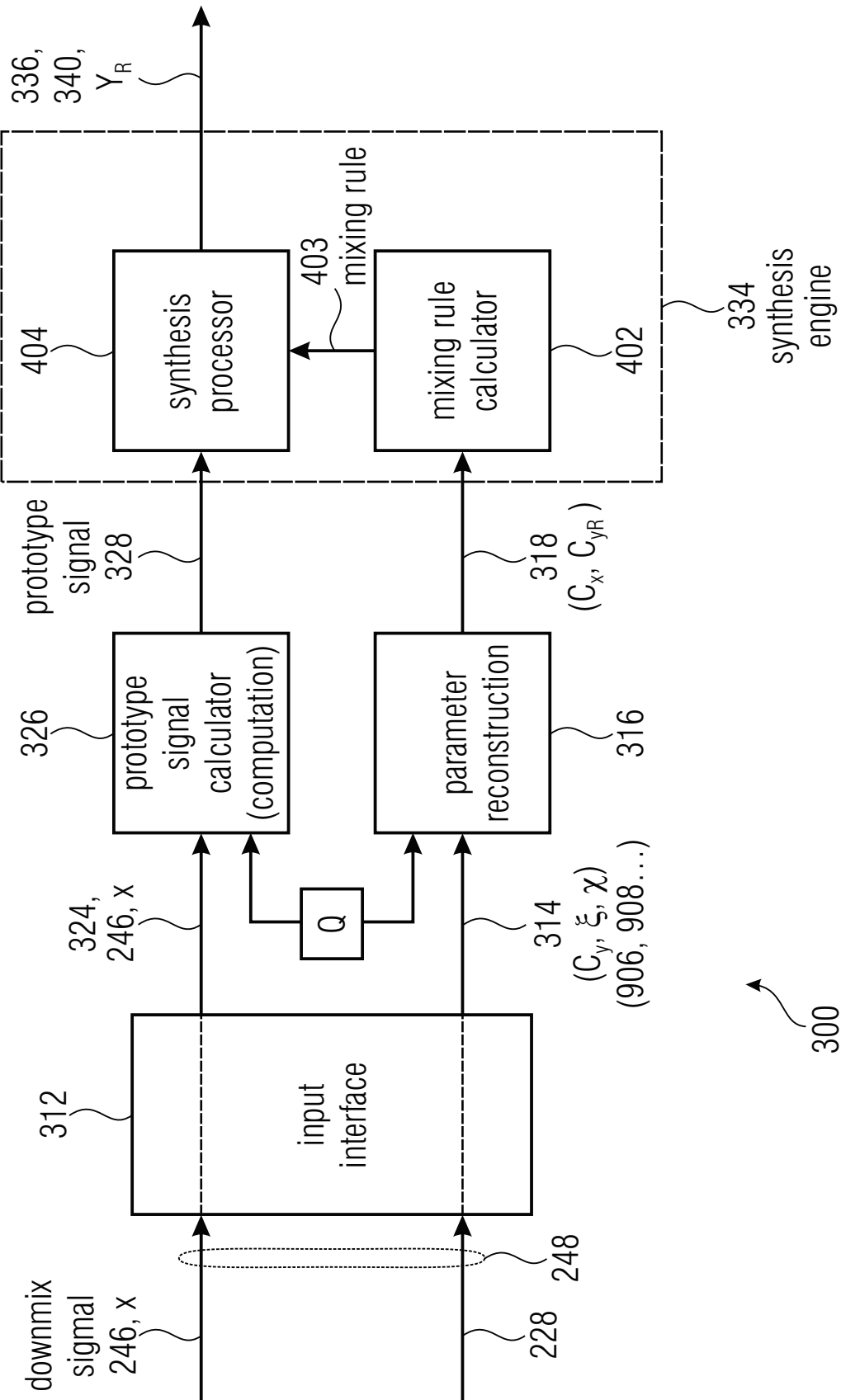


Fig. 3a

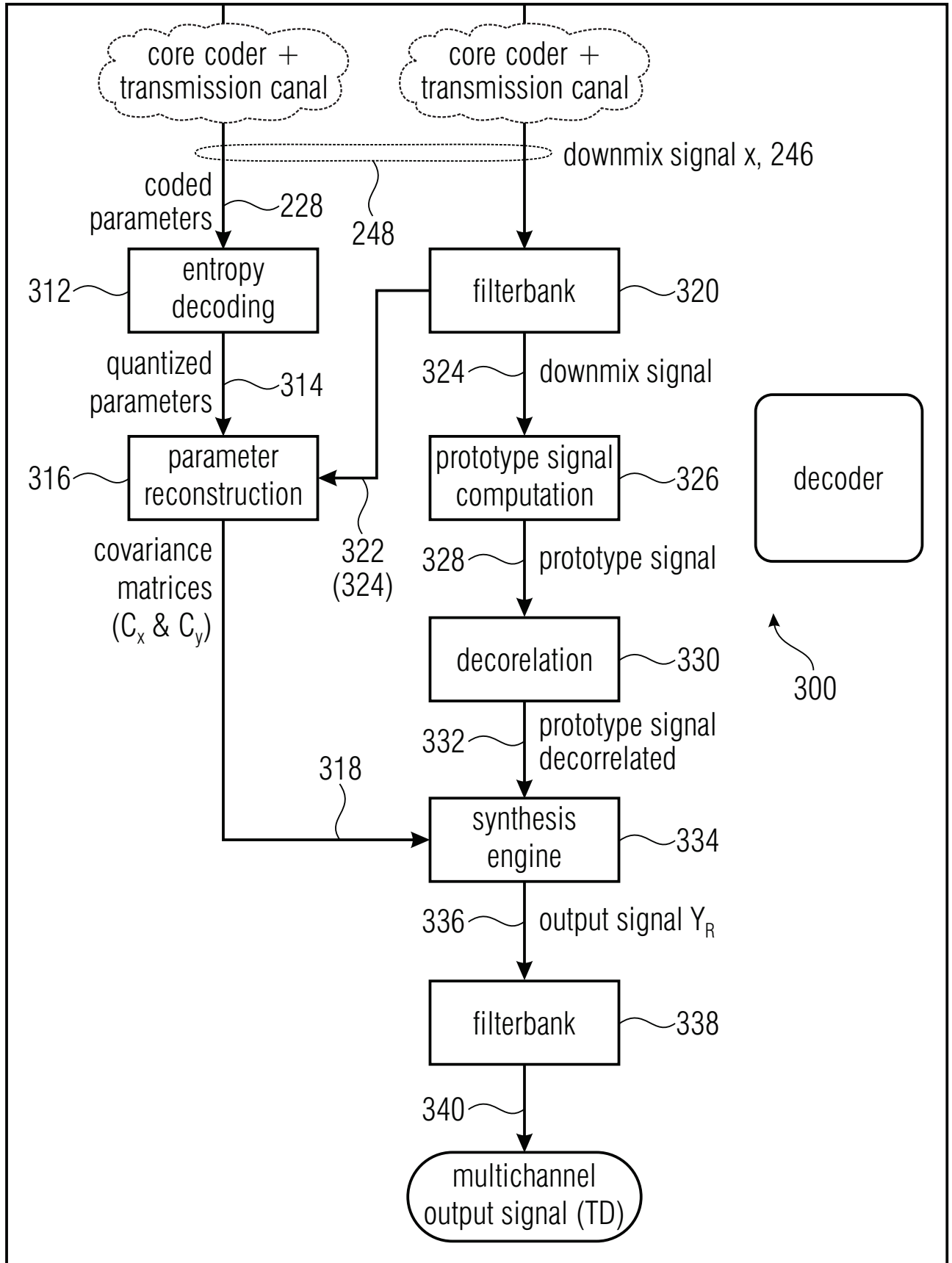


Fig. 3b
overview of decoder modules

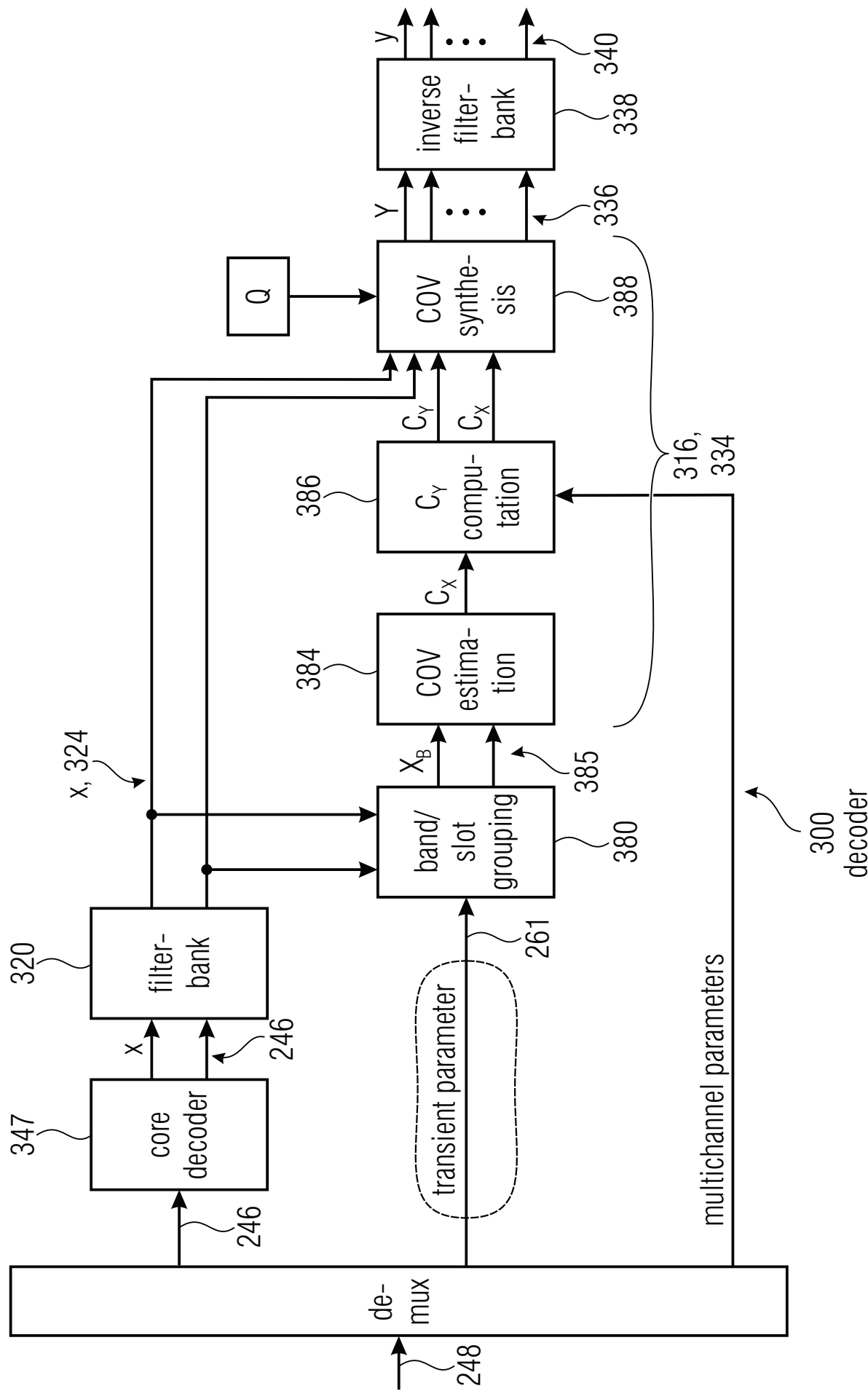


Fig. 3c

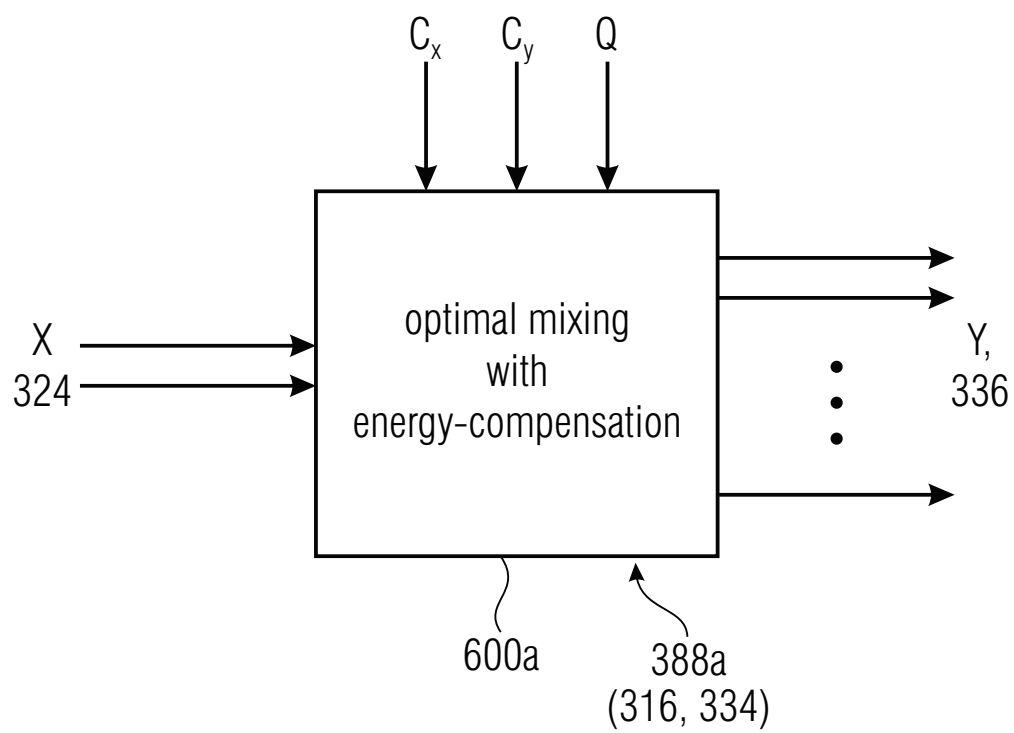


Fig. 4a

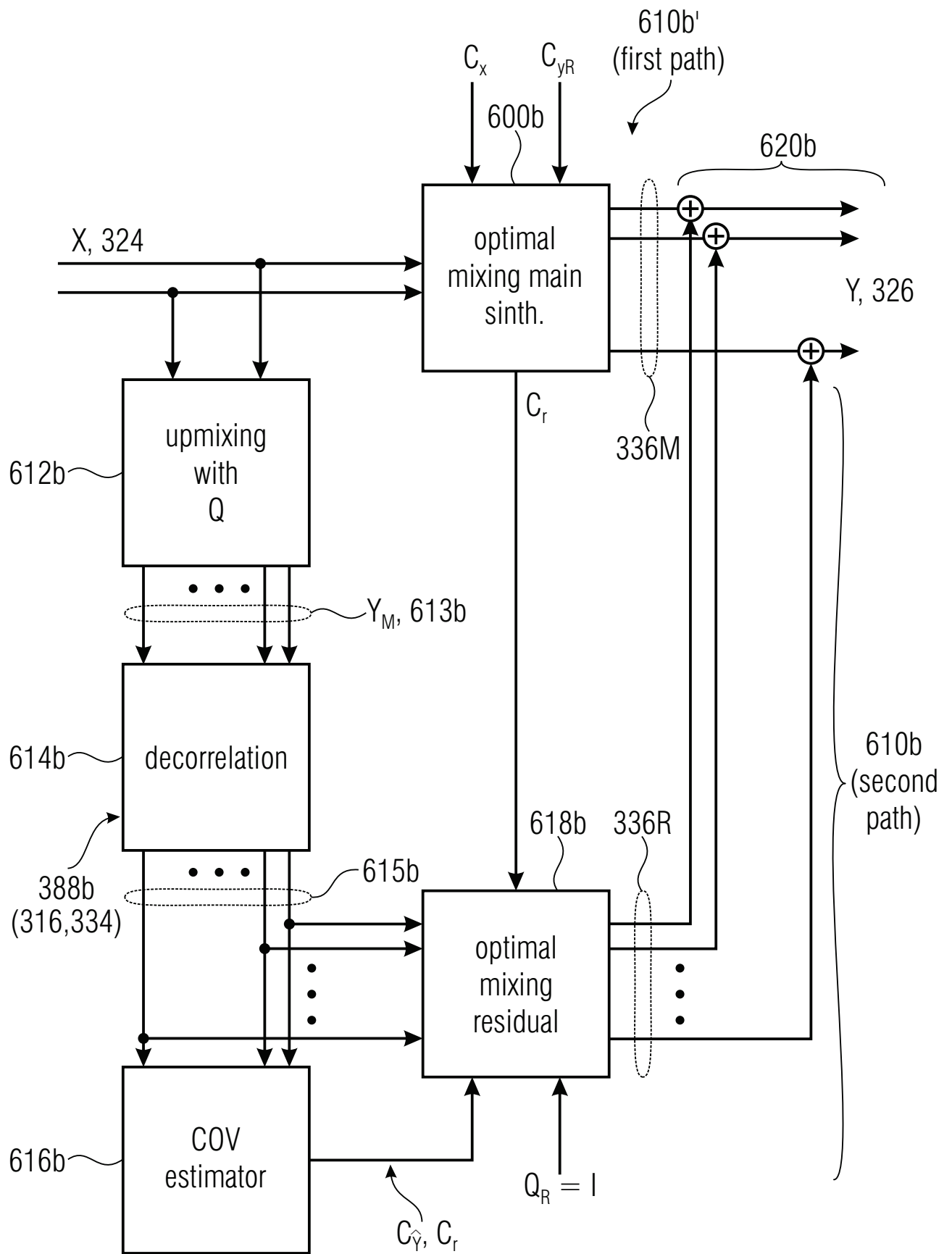


Fig. 4b

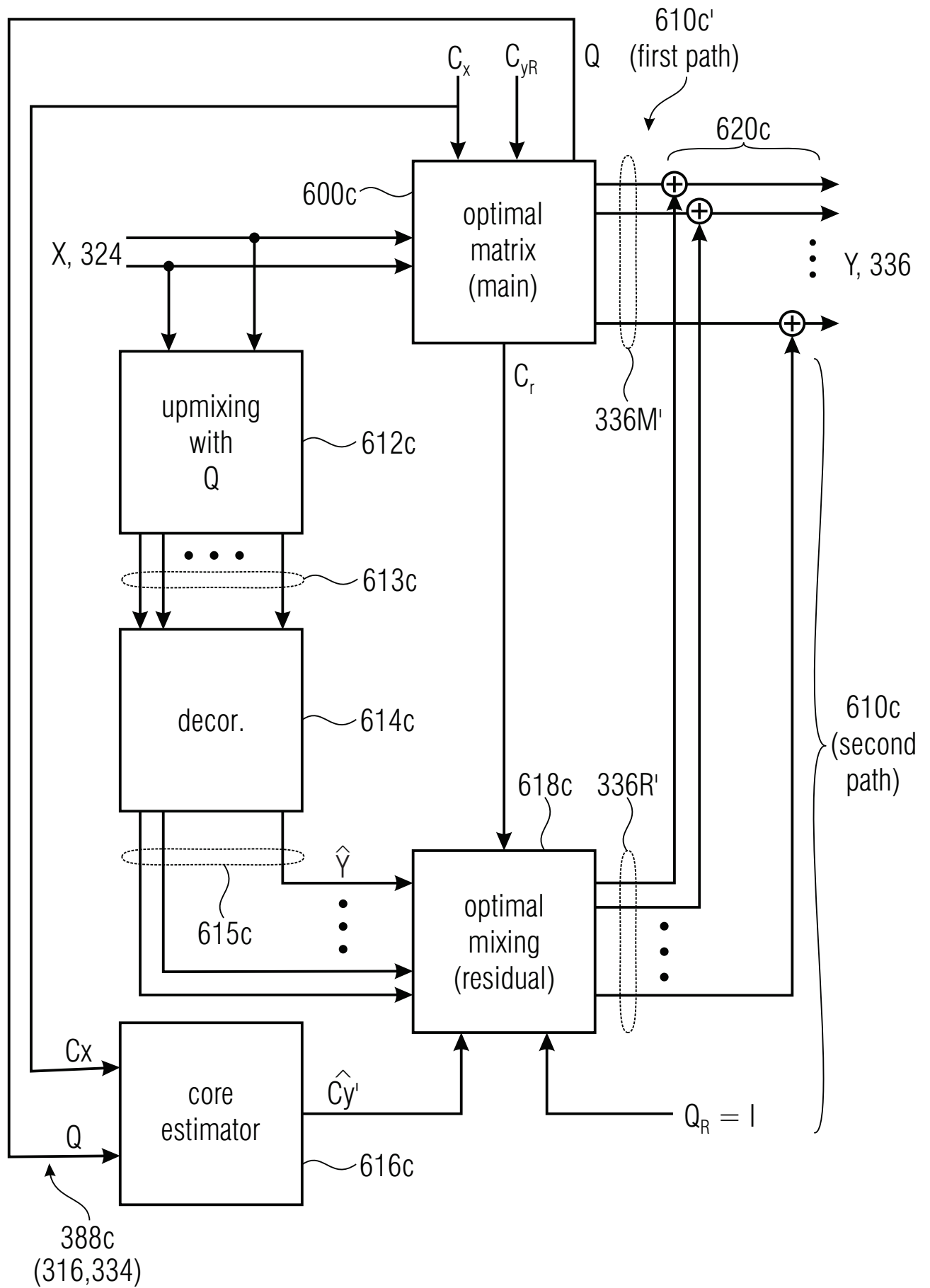


Fig. 4c

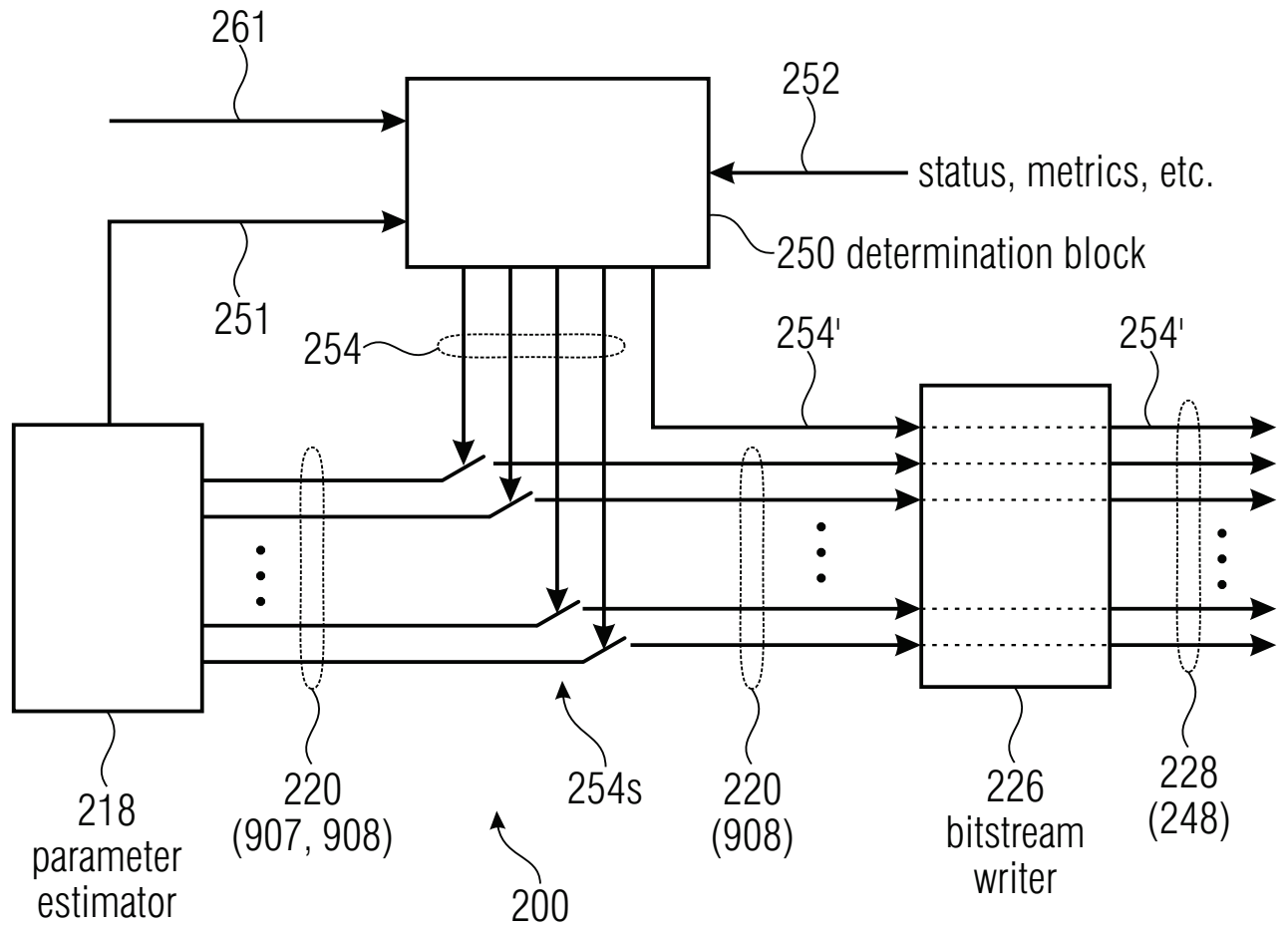


Fig. 6a

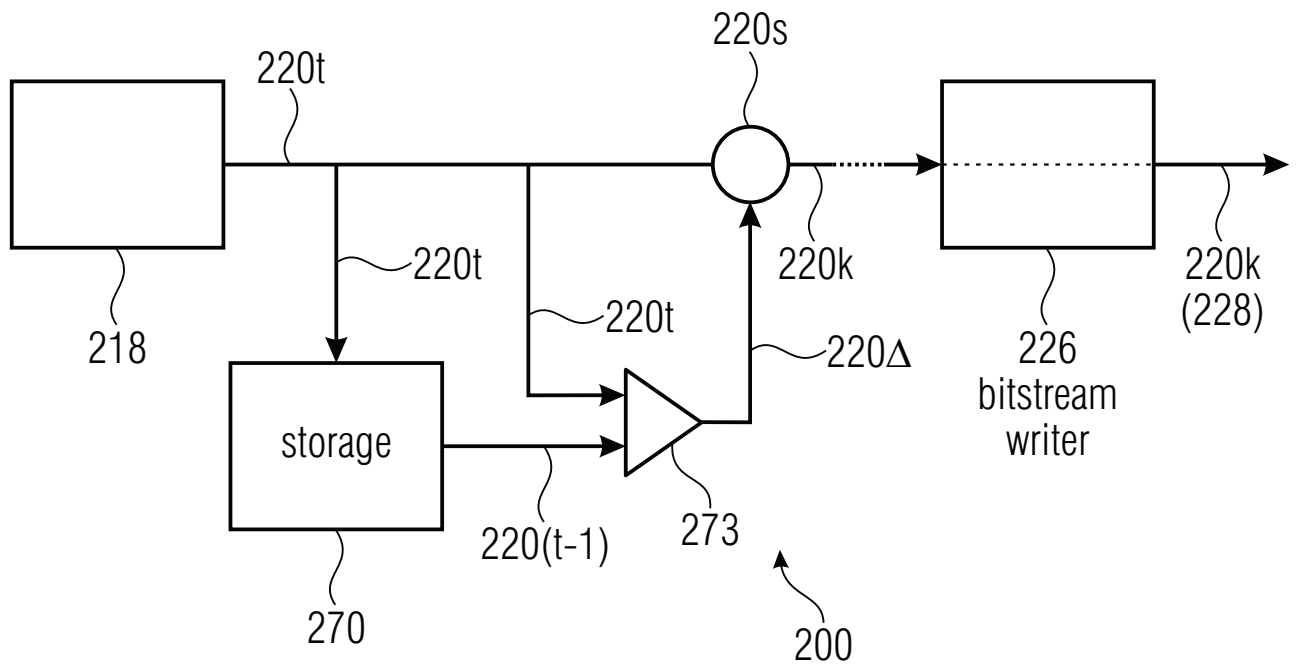


Fig. 6b

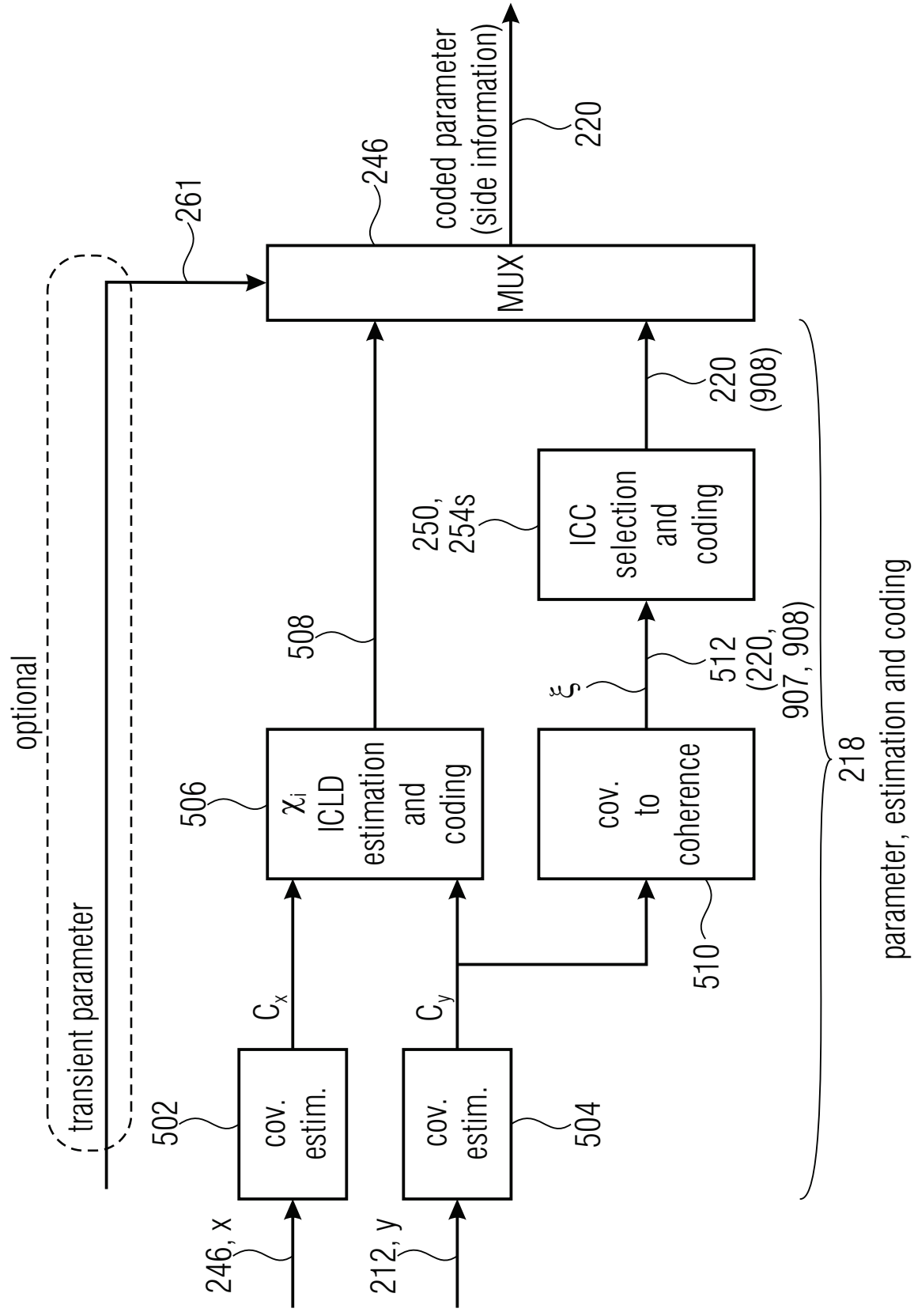


Fig. 6c

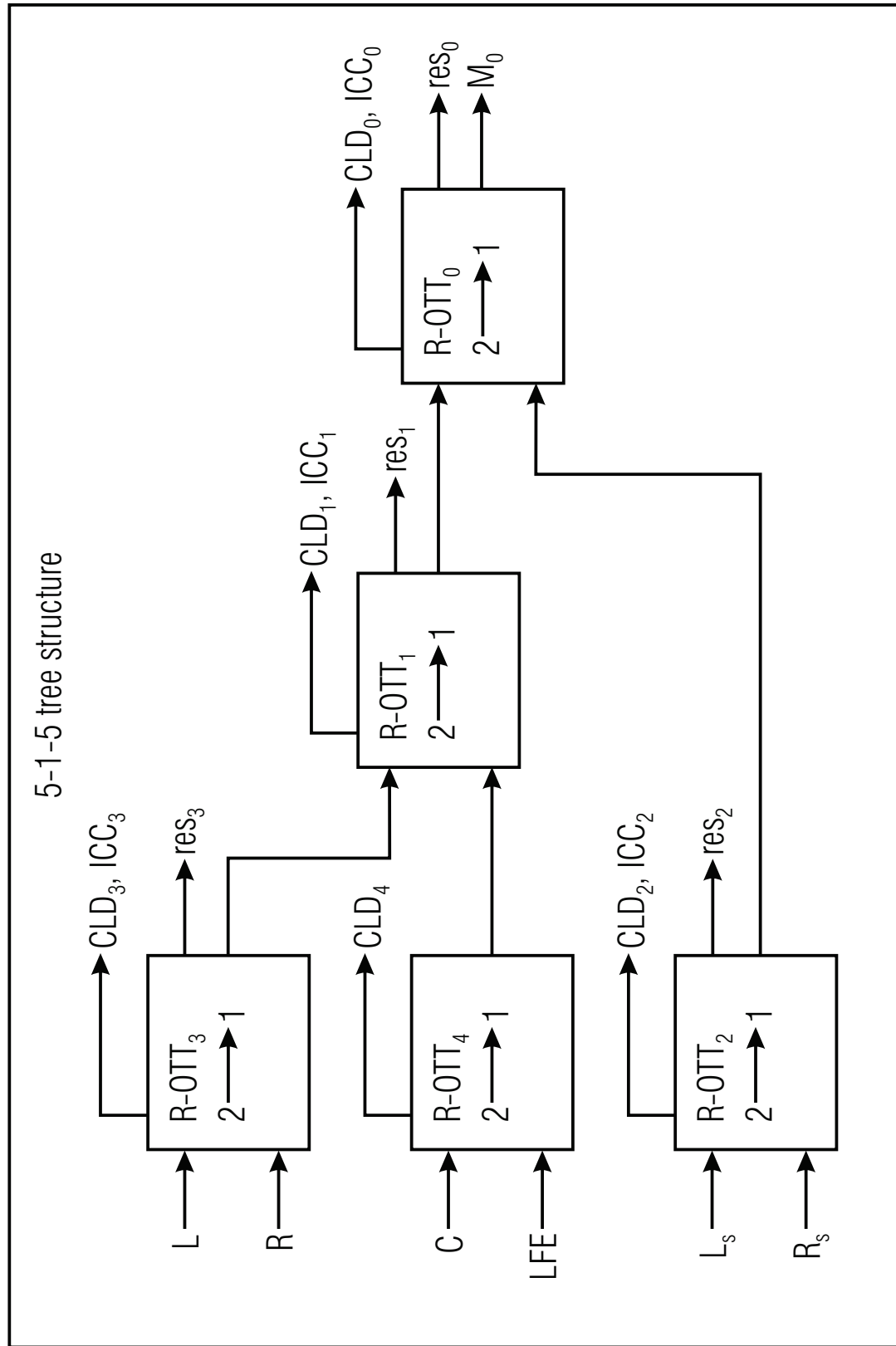


Fig. 7
(PRIOR ART)

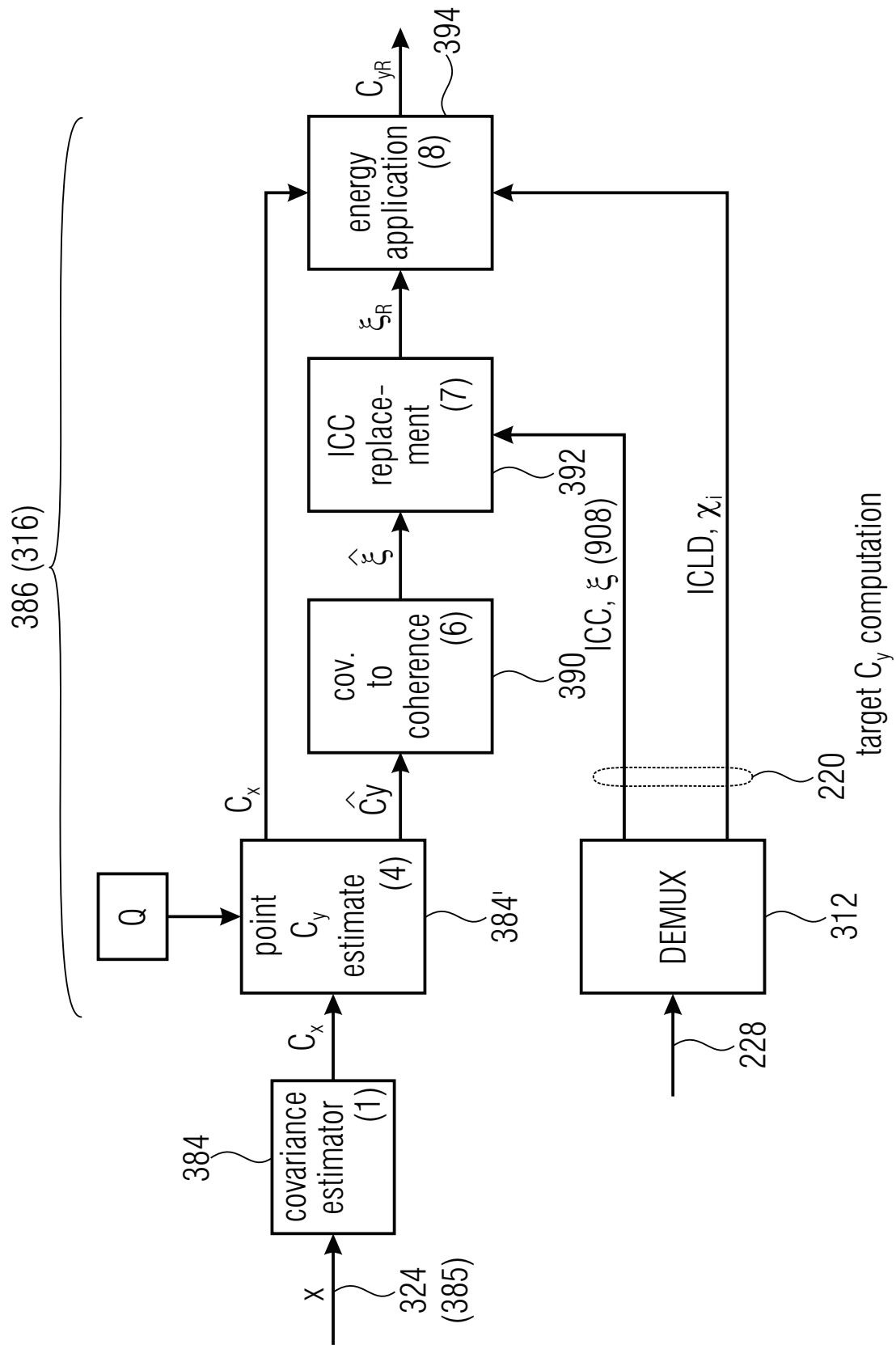


Fig. 8a

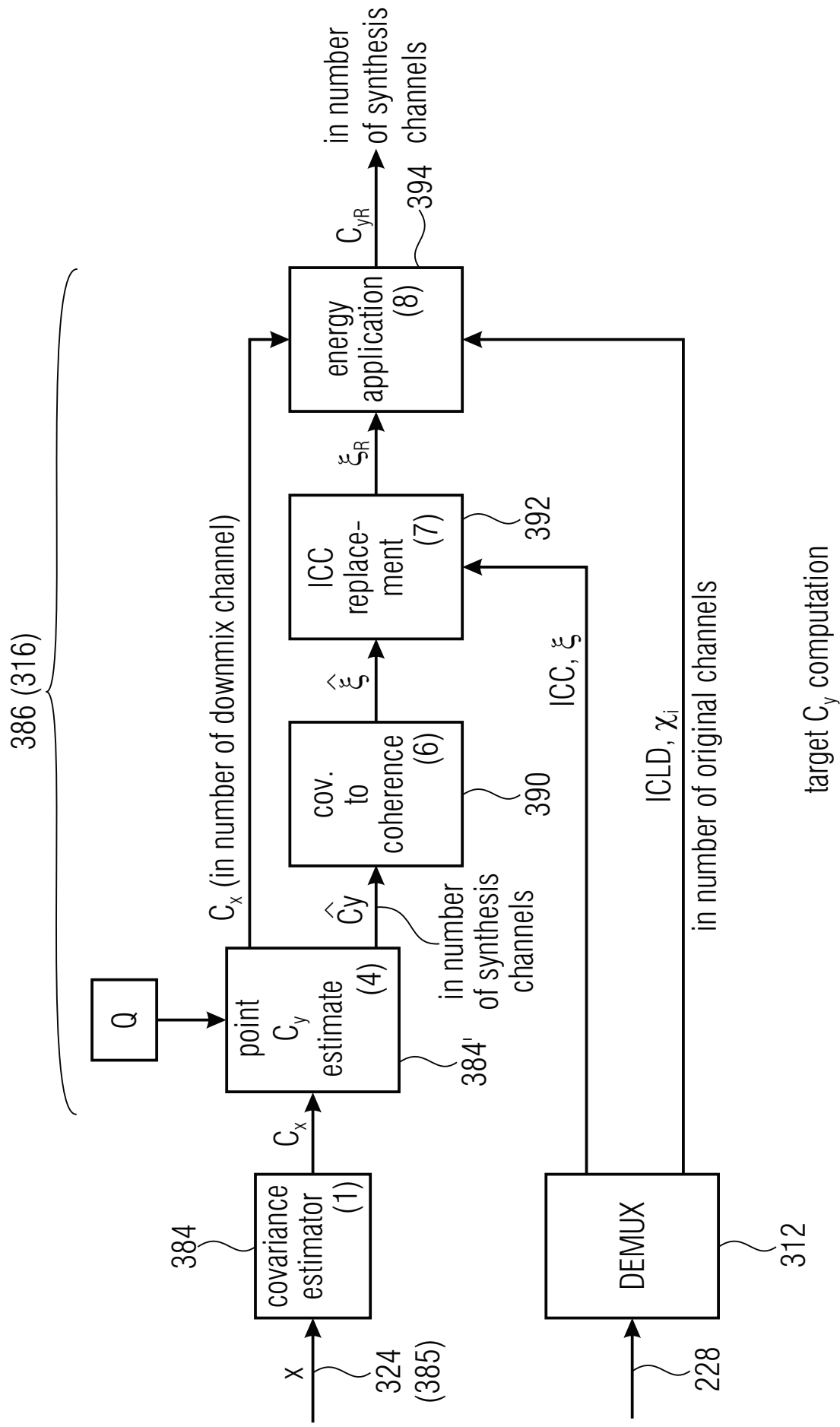


Fig. 8b

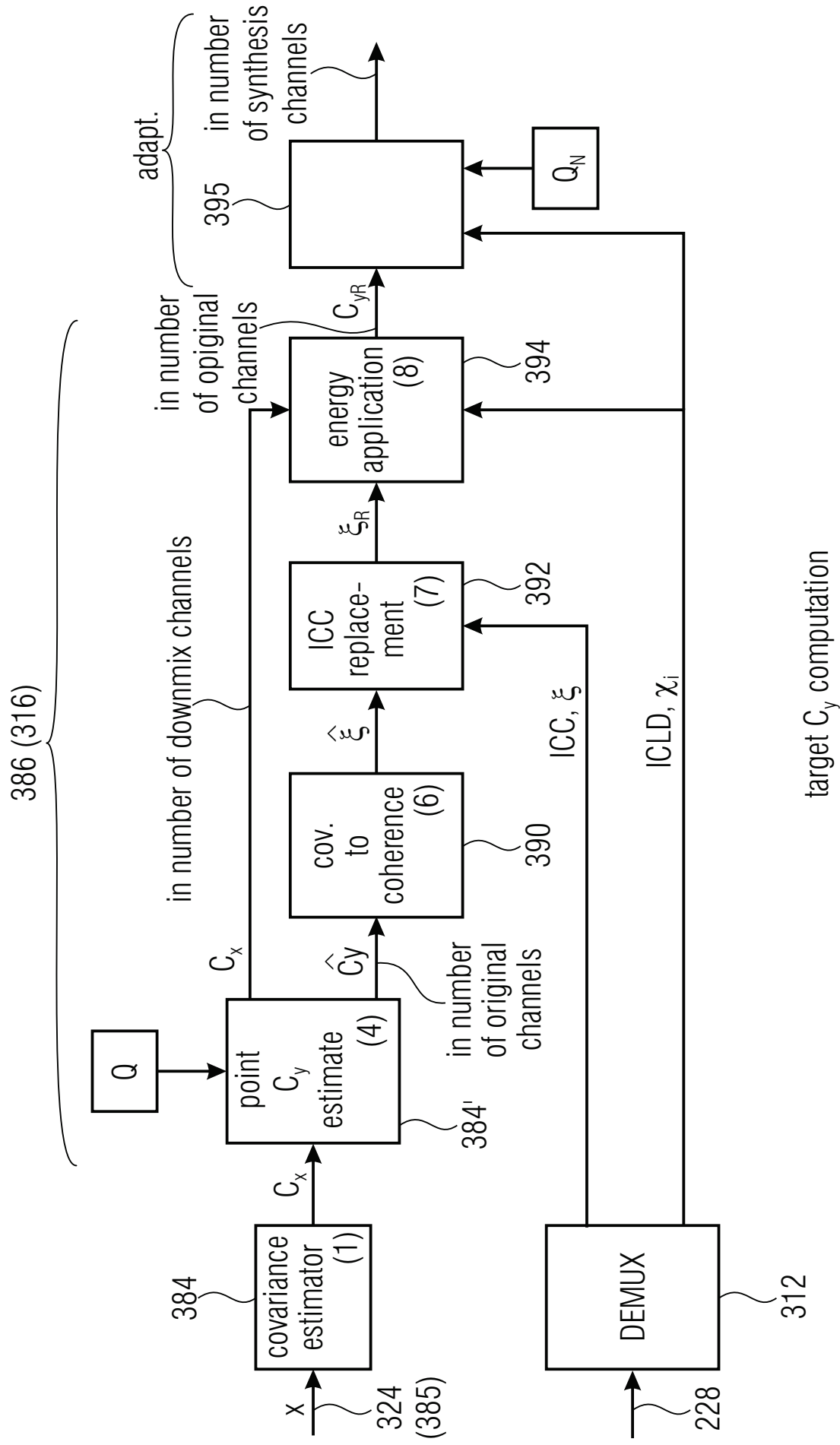


Fig. 8c

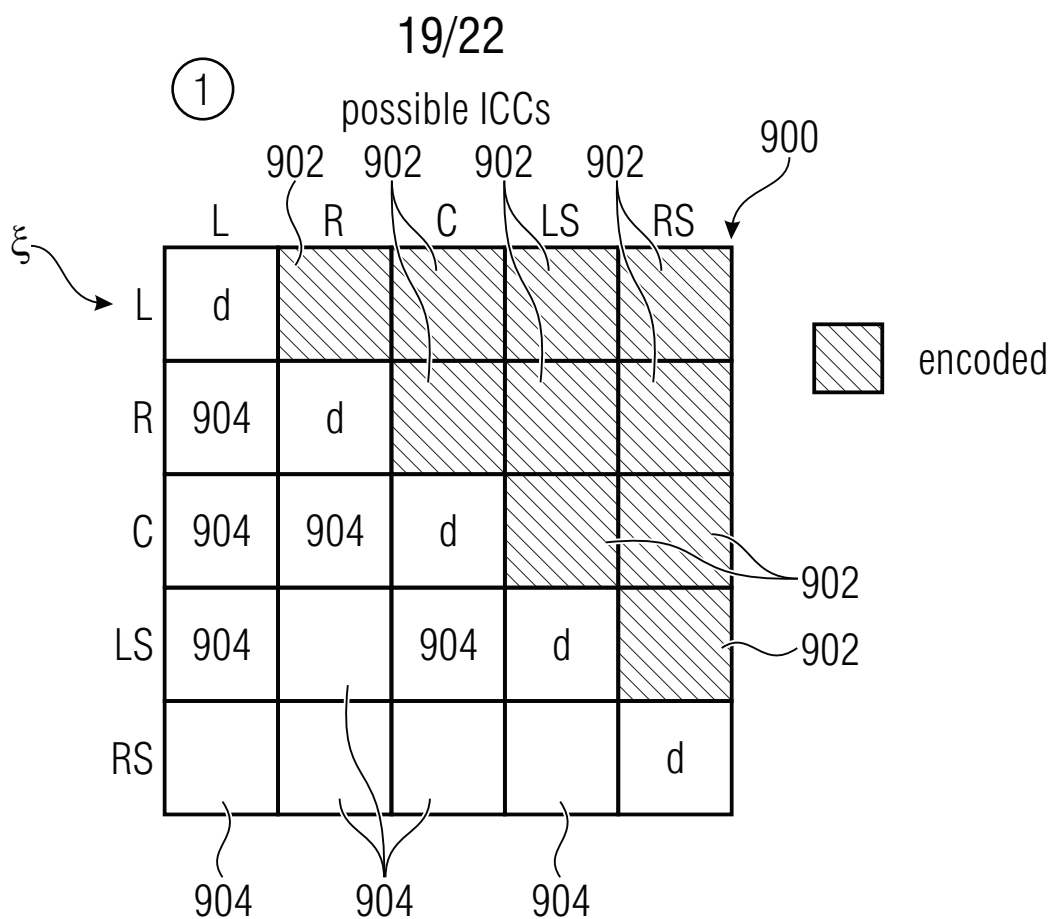


Fig. 9a

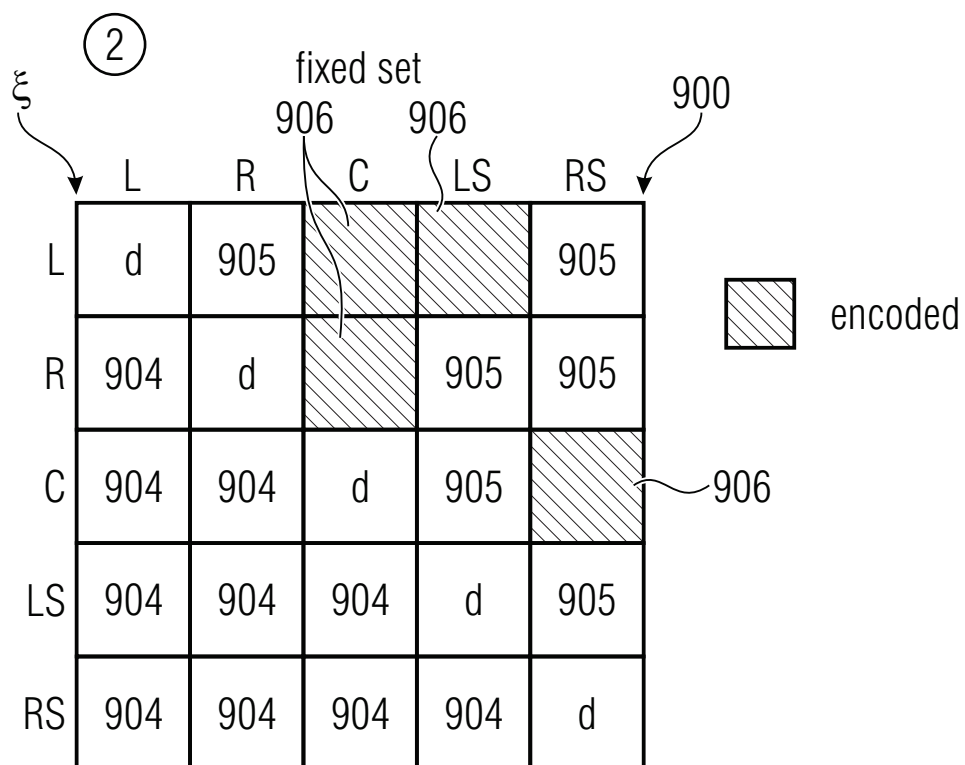


Fig. 9b

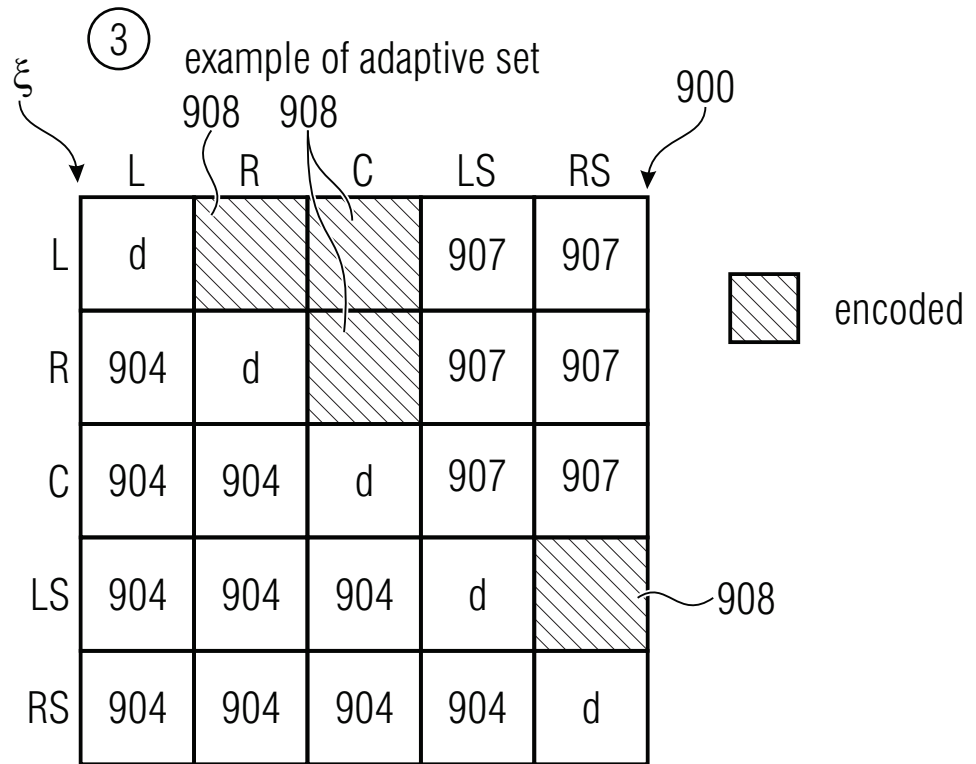


Fig. 9c

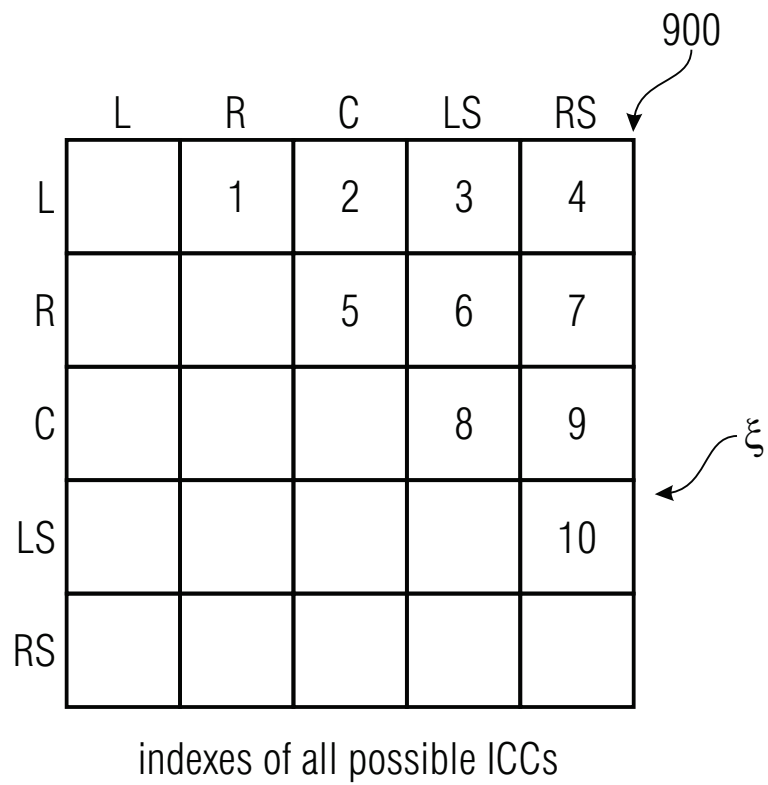


Fig. 9d

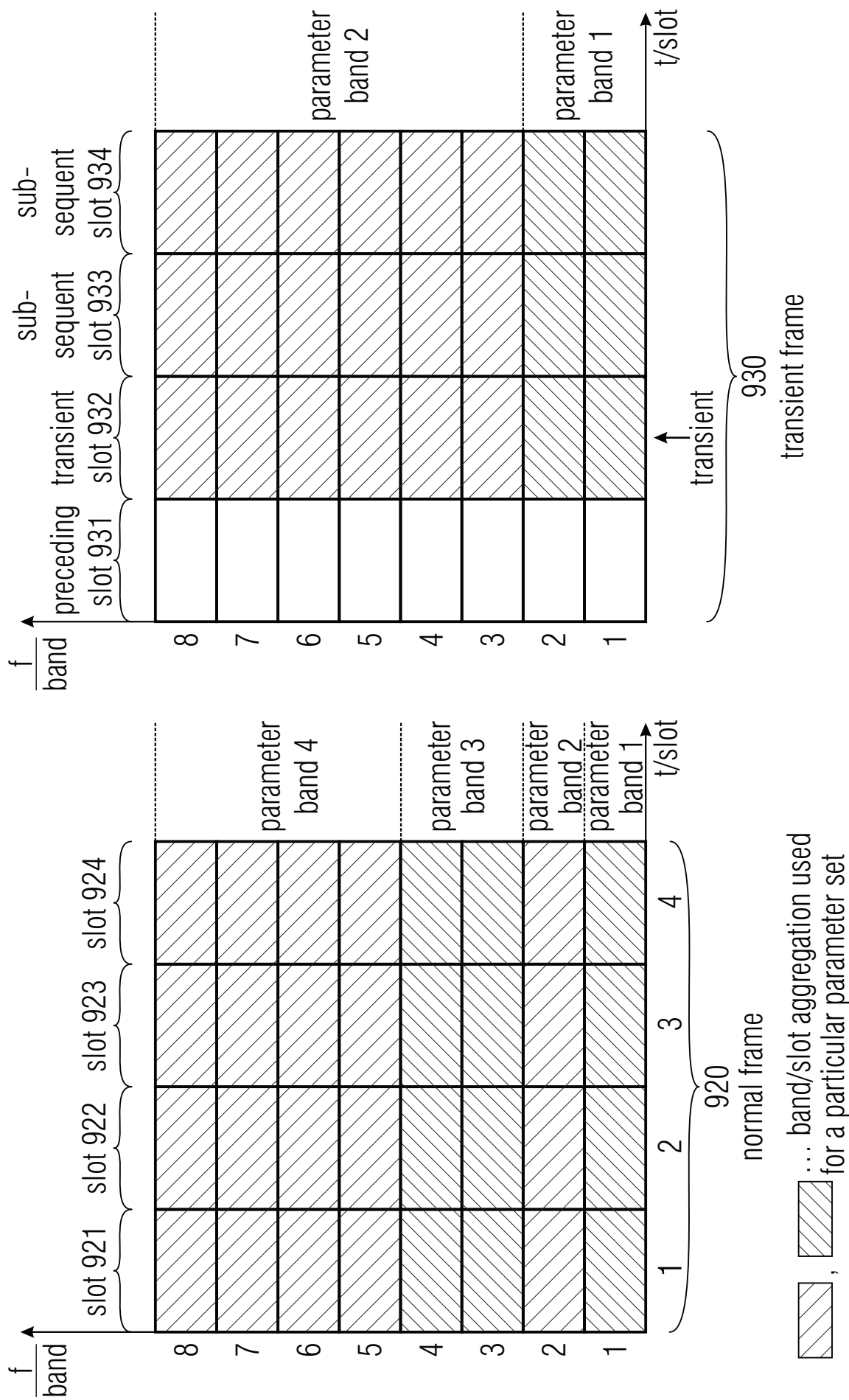


Fig. 10a

Fig. 10b

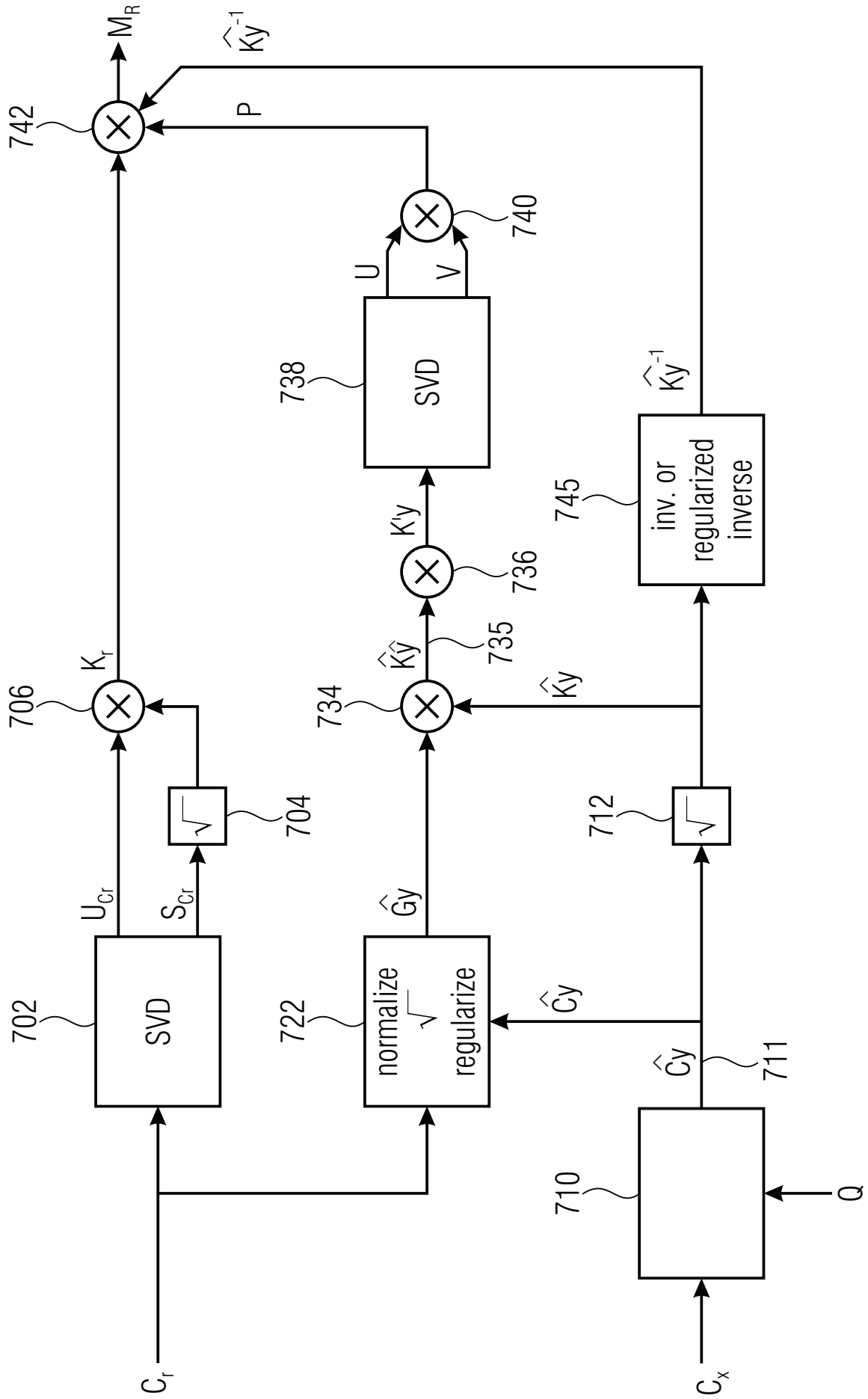


Fig. 11