

Description

This invention is directed to a circuit arrangement for delaying control circuit operation with respect to the application of operating voltage to the circuit's voltage supply input. The circuit may be of the integrated type.

Such a control circuit ordinarily includes a slow-start section. The slow-start section suppresses control circuit operation until voltage at a slow-start section input rises to a certain level.

A typical prior art arrangement: (a) applies to a resistive-capacitive (RC) network, external to the control circuit, a voltage derived from the same external supply which also is connected to the control circuit's voltage supply input and (b) connects a capacitor of the network to the slow-start section input. At start-up, i.e., when the capacitor is uncharged and voltage is first applied to the control circuit's voltage supply input, voltage across the network capacitor starts to rise. Control circuit operation is suppressed or inhibited for a delay interval sufficient to allow the control circuit to become operative. The interval is determined by the time needed for the voltage on the capacitor to reach a certain level. In this way, the control circuit is given the opportunity to become fully effective before undertaking its operational function(s).

The slow-start system or arrangement typically has the RC network coupled to the same supply used to supply voltage to the voltage input of the control circuit. Assuming that voltage present at the circuit voltage supply input rises rapidly to the nominal level of the external source, the interval provided to develop the certain voltage at the network capacitor is determined by the values of the network's serially-connected resistors and the value of the network's capacitor, which typically is connected across one of the resistors.

This prior art arrangement presents a problem, in that the delay interval is not related to the time actually needed, for example, by devices within an internal voltage supply of the control circuit to develop the required voltage levels for distribution to the remainder of the control circuit. Another problem is that the level of voltage obtained from the external network is not related to levels of voltage developed by devices within the internal supply of the control circuit.

According to the present invention there is provided a circuit arrangement that provides for a start-up delay in normal performance of a principal circuit (30) operation, comprising: a first voltage reference device circuit (40) for developing an energizing voltage (on 36) upon initiation of said start-up; a control circuit (24,26,28) that is incapable of providing said normal performance of said principal circuit operation until a supply voltage applied

thereto attains an operating level; a stabilized power supply (22) including a second voltage reference device circuit (212) coupled via a biasing arrangement (211) to said energizing voltage (on 36) for generating and stabilizing said supply voltage at a stabilized supply terminal (7.5V), the operating level of said stabilized supply voltage being related in level to that of said second voltage reference device circuit (212) and attaining said operating level after a first delay interval from said initiation of said start-up; an inhibiting circuit (29) coupled to said control circuit (24,26,28) and including a semiconductor element (291) controllable in conduction in accordance with an input voltage (at pin 10) and said stabilized supply voltage (7.5V), said inhibiting circuit (29) inhibiting said normal performance until said input voltage exceeds a threshold level; and an integrating network (50A) coupled to said semiconductor element (291) for providing said input voltage; Characterized That said integrating network (50A) is coupled to said second voltage reference device circuit (211,212) for integrating said second reference voltage so that the said input voltage (at pin 10) varies in level during start-up so as to exceed said threshold level after elapse of a second delay interval from initiation of start-up, thereby inhibiting said normal performance until elapse of said second delay interval.

By connecting the integrating network to the said second voltage reference device circuit of the stabilized power supply, the said second delay interval relates directly to the time needed within the control circuit to develop voltage across the second reference device of the stabilized power supply, so that the delay interval is measured in terms of the circuit's ability to function.

Another problem of the prior art arrangement is that the above-mentioned external network typically continues to draw current from the external source after the delay interval ends and during the time the control circuit is operational, i.e., when the circuit is carrying out its expected functions.

In an embodiment of the invention, the integrating network is a series arrangement of a resistive means and a capacitive means. With such a series arrangement, once the capacitive means is charged no more current is drawn by it.

In the following detailed description of an embodiment of the invention, reference is made to the next-identified drawing figures, in which elements common to the figures bear like numbers.

In the drawing:

FIGURE 1 is a prior art system for delaying the start of operation of a typical control circuit, which is incorporated in a power supply; and FIGURE 2 shows a system embodying the present invention having such a control circuit and an external RC network.

In order to provide background to the present invention, reference first is made to the prior art power supply 10 shown in FIGURE 1. Supply 10 includes a regulator 30, which is controlled by control circuit 20. Regulator 30 draws power from an unregulated voltage source connectable to terminals 11 and 12 of system 10. Control circuit 20 may be the CA1523 Variable Interval Pulse Regulator (VIPUR) circuit made by RCA Corporation.

The system of FIGURE 1 operates as follows. When regulator 30 and control circuit 20 are operating, voltage of unregulated level appearing at terminals 11 and 12 is applied to the serially-connected primary winding P1 of transformer T1 and the conduction path of switching transistor 31 of regulator 30. Each pulse, in a stream of switching pulses produced at pin 6 by control circuit 20, is applied to the control electrode of transistor 31 to switch transistor 31 to its conducting condition. The consequent intermittent current flow in primary P1 induces current flow in each of transformer T1's secondary windings, S1 and S2.

Current induced in secondary winding S1 is rectified by diode 32; and the resulting direct voltage appearing across winding S1 and diode 32 is averaged by capacitor 33. The smoothed voltage is connected to supply output terminals 14 and 15. As is brought out below, the level of the output voltage is regulated in accordance with the operation of control circuit 20.

Current induced in secondary winding S2 of transformer T1 is rectified by diode 34, and the resulting voltage across winding S2 and diode 34 is averaged by capacitor 35 and applied to conductor 36. Voltage on conductor 36 is a smooth level and is applied to a voltage supply input (at pin 7) and to an error input (at pin 1) of control circuit 20.

In the following description, description of elements of control circuit 20 and their operation is not set forth in detail, because such detailed description is not necessary to the understanding of the present invention.

Voltage appearing on regulator output conductor 36 is applied via pin 7 to the input of internal voltage supply 22, which is internal to control circuit 20. More specifically, such voltage is applied to serially-connected, resistor 211 and zener diode 212, so that there appears on the cathode electrode of zener diode 212 a voltage, which stabilizes at a nominal 8.4 volt level when voltage on conductor 36 is at a nominal 13 volt level.

Internal supply 22 also includes other devices, such as transistor 213. Those other devices are interconnected to diode 212 and to each other. Diode 212 and the other devices in supply 22 produce at respective outputs of internal supply 22 voltages of levels suitable for use throughout the remainder of control circuit 20.

With the appearance of voltage on conductor 36 and with the production of the various levels of voltage by internal supply 22, current control circuit 24 admits current to modulator 26. Modulator 26 responds to such admitted current by causing output driver 28 to produce the previously mentioned stream of switching pulses at pin 6 for application to the control electrode of regulator transistor 31.

The level of voltage on conductor 36 and at error input pin 1 varies about some nominal level, differences between actual and nominal levels being caused, for example, by changes in voltage level of the unregulated supply connected to terminals 11 and 12 or by changes in current drawn from output terminals 14 and 15. Within control circuit 20, deviations from the nominal error voltage level at pin 1 are detected by current control circuit 24. Current control circuit 24 responds to detected level deviations at pin 1 by causing modulator 26 to change the frequency and duty cycle of switching pulses produced at output pin 6 in directions which tend to return the level of voltage on conductor 36 to the nominal error level. In summary, as used in power supply 10, control circuit 20 regulates the frequency and duty cycle of switching pulses at pin 6 to maintain voltage across output terminals 14 and 15 at a substantially constant level.

The above-given explanation of power supply 10 operation presupposes that the circuit 20 already is operating and producing the stream of switching pulses at output pin 6. However, at start-up of supply 10, i.e., immediately after voltage appears at input terminals 11 and 12, control circuit 20 is not producing switching pulses, so that transistor 31 is turned off. Consequently, at that time transformer T1 does not produce a voltage at secondary winding S2 for application to output conductor 36 and to the input of internal supply 22.

To provide operating voltage to the internal voltage supply 22 at start-up, the supply 10 additionally includes an alternate path between terminal 11 and conductor 36. The alternate path includes voltage divider 40, which in turn comprises resistor 41 and zener diode 42 serially connected across input terminals 11 and 12. A tap 43 of divider 40 is connected through diode 16 to conductor 36 and voltage supply input pin 7. When regulator 30 is not producing voltage for application to conductor 36, diode 16 is forward-biased. Therefore, the alternate path provides operating voltage at pin 7 for the voltage input of internal voltage supply 22. After regulator 30 and control circuit 20 become operative, the higher-level, rectified, smoothed voltage from the regulator 30 reverse-biases diode 16, to block the alternate path.

At start-up, i.e., when voltage first appears across input terminals 11 and 12, it is undesirable to allow switching transistor 31 to respond to the early pulses produced at output pin 6 of circuit 20. Such initial output pulses may be produced before operation of control circuit 20 stabilizes, for example before internal supply 22 produces stabilized voltage levels at its respective outputs. If such operation before stabilization is attempted, the frequency or duty cycle of the early produced pulses may not be properly regulated. Lack of regulation, in turn, may cause damage to elements within regulator 30, control circuit 20, or external devices connected to terminals 14 and 15.

To assure that production of output pulses by control circuit 20 is delayed from the time voltage first is applied to input terminals 11 and 12 until control circuit 20 stabilizes, a slow-start system is provided to delay the start of circuit 20 from the time voltage first appears on terminals 11 and 12. That prior art slow-start system is described next.

Control circuit 20 includes slow-start section 29. As earlier mentioned, detailed description of slow-start section 29 and of other elements of control circuit 20 is not necessary to an understanding of the present invention. Accordingly, the following description of section 29 and other parts of circuit 20 is generalized and is provided only by way of example of functions provided by control circuit 20, whose start-up is to be delayed.

An input to slow-start section 29 extends from pin 10 to a base electrode of slow-start transistor 291. In the absence of external voltage applied to slow-start pin 10, transistor 291 is biased (as voltage develops at devices within internal supply 22) into conduction, causing current-mirror, diode 295 and transistor 294, to conduct and therewith divert current from the modulator 26. Such current diversion inhibits the production of output pulses (for use by driver 28) by modulator 26. The collector current of transistor 291 is returned to ground via diode 295 which (with transistor 294) acts as a current mirror. As a result of conduction in transistor 294, operation of modulator 26 is inhibited. On the other hand, when external voltage applied to pin 10 rises above the abovementioned certain level, then conduction in transistor 291 is cut-off, causing transistor 294 to be non-conductive. Non-conduction in transistor 294 enables modulator 26 to function so that control circuit 20 supplies switching pulses at pin 6.

As indicated in FIGURE 1, the prior art system for controlling voltage applied to slow-start pin 10 includes an external RC network 50. Network 50 is connected across the input voltage supply by way of tap 43 of divider 40. At start-up, the appearance of voltage across input terminals 11 and 12 and zener diode 42 allows current flow through serially-

connected resistors 51 and 52 of network 50 and the accumulation of voltage across network capacitor 53. Capacitor 53 is connected in parallel with resistor 52 and at tap 54 to slow-start pin 10.

At the time voltage first appears across input terminals 11 and 12, at start-up, capacitor 53 is in a discharged state. As voltage levels develop at devices in supply 22, transistor 291 is biased to conduct, because the voltage at pin 10 is insufficient to cutoff transistor 291. During the delay interval, which is measured from the appearance of voltage across terminals 11 and 12, the voltage across capacitor 53 rises. The end of the delay interval is marked by the voltage across capacitor 53 reaching a certain level, which is sufficient to cut-off transistor 291.

The length of the delay interval is determined by factors such as the level of voltage developed at zener diode 42 and the values of resistors 51 and 52 and of capacitor 53, all of which are external to circuit 20 and none of which relates directly to the internal operation of circuit 20. The length of the delay interval provided by external network 50 is chosen to be at least as long as the estimated time needed by control circuit 20 to become operational. The described arrangement for providing the delay interval is not precise, because it is based on an interval calculated to be equal to or greater than the estimated time needed by circuit 20 to become operational. The described arrangement also is undesirable, because network 50 continues to draw current from tap 43 of divider 40 after the end of the delay interval.

In order to deal with the above-mentioned and other problems, an embodiment of the present invention uses an improved system illustrated in FIGURE 2. In FIGURE 2, slow-start section 29 of control circuit 20 is connected as indicated in FIGURE 2 to an external RC network 50A, which is substituted for network 50 indicated in FIGURE 1. Network 50A is connected via pin 13 of control circuit 20 to the cathode electrode of zener diode 212. RC network 50A consists of a single resistor 51A, serially-connected to capacitor 53A. The power supply, in which the control circuit 20 of FIGURE 2 and network 50A may be included, otherwise is similar to the power supply 10 indicated in FIGURE 1, and, except for the slow-starting system, the operation is as previously described.

During the start-up, the voltage appearing on conductor 36 from the power supply input places devices of internal supply 22 in condition to provide respective voltage levels for distribution within circuit 20. Circuit 20 is considered to be in condition to initiate the delay interval when devices, such as zener diode 212, of internal supply 22, deliver respective voltage levels to other parts of circuit 20, such as current control circuit 24. As a

consequence, the present invention is used to measure the delay interval by taking voltage for application to network 50 from such a device: namely, zener diode 212. The nominal voltage, 8.4 volts to be developed across diode 212 is greater than the certain voltage needed at pin 10 to cut-off conduction in slow-start transistor 291.

During start-up, the voltage across capacitor 53A of network 50A increases from zero as the voltage across zener diode 212 increases. When, as previously mentioned, the voltage at slow-start pin 10 reaches the certain level, transistor 291 is cutoff, and modulator 26 and the remainder of circuit 20 no longer is disabled from carrying out its expected functions.

In the specifically described embodiment of the invention, the ability of zener diode 212 within supply 22 to produce the required nominal output level of 8.4 volts may be regarded as an indication of the ability of the entire circuit 20 to perform its assigned function.

The delay interval is measured starting from the time at which voltage appears across diode 212 and the application of voltage to network 50A and ending when voltage at slow-start pin 10 reaches the level required to cutoff conduction in transistor 291. This relates the start of operation of circuit 20 to the ability of internal supply 22 to supply voltage levels to various parts of control circuit 24.

A second relationship between circuit 20 operation and the delay interval is provided by the connection of the emitter of slow-start transistor 291 through resistor 292 and the base-emitter junction of transistor 213 to the cathode of zener diode 212. This connection assures that the voltage present on diode 212 is higher (by the added V_{be} voltage drops across NPN type transistors 213 and 291) than the threshold of transistor 291 at the time the delay interval ends and control circuit 20 becomes operative.

The above-described system of FIGURE 2 offers a further advantage over the typical prior art system indicated in FIGURE 1, in that RC network 50A includes one less resistor than the corresponding traditional RC network 50 indicated in FIGURE 1. Still further, RC network 50A draws current only while capacitor 53A is being charged, in contrast to the prior art network 50, which continues to draw current during the time the control circuit 20 in FIGURE 1 is operational.

While use of control circuit 20, whose operation is controlled by the present inventive system, has been described within the context of power supply 10, those skilled in the art will realize that such use is not a limitation on the invention, as set forth in the following claims.

Claims

1. A circuit arrangement that provides for a start-up delay in normal performance of a principal circuit (30) operation, comprising:
 - a first voltage reference device circuit (40) for developing an energizing voltage (on 36) upon initiation of said start-up;
 - a control circuit (24,26,28) that is incapable of providing said normal performance of said principal circuit operation until a supply voltage applied thereto attains an operating level;
 - a stabilized power supply (22) including a second voltage reference device circuit (212) coupled via a biasing arrangement (211) to said energizing voltage (on 36) for generating and stabilizing said supply voltage at a stabilized supply terminal (7.5V), the operating level of said stabilized supply voltage being related in level to that of said second voltage reference device circuit (212) and attaining said operating level after a first delay interval from said initiation of said start-up;
 - an inhibiting circuit (29) coupled to said control circuit (24,26,28) and including a semiconductor element (291) controllable in conduction in accordance with an input voltage (at pin 10) and said stabilized supply voltage (7.5V), said inhibiting circuit (29) inhibiting said normal performance until said input voltage exceeds a threshold level; and an integrating network (50A) coupled to said semiconductor element (291) for providing said input voltage; Characterized That
 - said integrating network (50A) is coupled to said second voltage reference device circuit (211,212) for integrating said second reference voltage so that the said input voltage (at pin 10) varies in level during start-up so as to exceed said threshold level after elapse of a second delay interval from initiation of start-up, thereby inhibiting said normal performance until elapse of said second delay interval.
2. A circuit arrangement according to claim 1 where said control circuit (24,26,28) includes a regulator circuit (26,28) for generating a switching signal (at pin 6), said circuit arrangement further including a switched mode regulated supply (30) responsive to said switching signal (at pin 6) for creating a source of regulated output voltage (across 30) that substitutes for said first voltage reference device circuit (40) in developing said energizing voltage after elapse of said second delay interval.

consequence, the present invention is used to measure the delay interval by taking voltage for application to network 50 from such a device: namely, zener diode 212. The nominal voltage, 8.4 volts to be developed across diode 212 is greater than the certain voltage needed at pin 10 to cut-off conduction in slow-start transistor 291.

During start-up, the voltage across capacitor 53A of network 50A increases from zero as the voltage across zener diode 212 increases. When, as previously mentioned, the voltage at slow-start pin 10 reaches the certain level, transistor 291 is cutoff, and modulator 26 and the remainder of circuit 20 no longer is disabled from carrying out its expected functions.

In the specifically described embodiment of the invention, the ability of zener diode 212 within supply 22 to produce the required nominal output level of 8.4 volts may be regarded as an indication of the ability of the entire circuit 20 to perform its assigned function.

The delay interval is measured starting from the time at which voltage appears across diode 212 and the application of voltage to network 50A and ending when voltage at slow-start pin 10 reaches the level required to cutoff conduction in transistor 291. This relates the start of operation of circuit 20 to the ability of internal supply 22 to supply voltage levels to various parts of control circuit 24.

A second relationship between circuit 20 operation and the delay interval is provided by the connection of the emitter of slow-start transistor 291 through resistor 292 and the base-emitter junction of transistor 213 to the cathode of zener diode 212. This connection assures that the voltage present on diode 212 is higher (by the added V_{be} voltage drops across NPN type transistors 213 and 291) than the threshold of transistor 291 at the time the delay interval ends and control circuit 20 becomes operative.

The above-described system of FIGURE 2 offers a further advantage over the typical prior art system indicated in FIGURE 1, in that RC network 50A includes one less resistor than the corresponding traditional RC network 50 indicated in FIGURE 1. Still further, RC network 50A draws current only while capacitor 53A is being charged, in contrast to the prior art network 50, which continues to draw current during the time the control circuit 20 in FIGURE 1 is operational.

While use of control circuit 20, whose operation is controlled by the present inventive system, has been described within the context of power supply 10, those skilled in the art will realize that such use is not a limitation on the invention, as set forth in the following claims.

Claims

1. A circuit arrangement that provides for a start-up delay in normal performance of a principal circuit (30) operation, comprising:
 - a first voltage reference device circuit (40) for developing an energizing voltage (on 36) upon initiation of said start-up;
 - a control circuit (24,26,28) that is incapable of providing said normal performance of said principal circuit operation until a supply voltage applied thereto attains an operating level;
 - a stabilized power supply (22) including a second voltage reference device circuit (212) coupled via a biasing arrangement (211) to said energizing voltage (on 36) for generating and stabilizing said supply voltage at a stabilized supply terminal (7.5V), the operating level of said stabilized supply voltage being related in level to that of said second voltage reference device circuit (212) and attaining said operating level after a first delay interval from said initiation of said start-up;
 - an inhibiting circuit (29) coupled to said control circuit (24,26,28) and including a semiconductor element (291) controllable in conduction in accordance with an input voltage (at pin 10) and said stabilized supply voltage (7.5V), said inhibiting circuit (29) inhibiting said normal performance until said input voltage exceeds a threshold level; and an integrating network (50A) coupled to said semiconductor element (291) for providing said input voltage;
 Characterized That
 - said integrating network (50A) is coupled to said second voltage reference device circuit (211,212) for integrating said second reference voltage so that the said input voltage (at pin 10) varies in level during start-up so as to exceed said threshold level after elapse of a second delay interval from initiation of start-up, thereby inhibiting said normal performance until elapse of said second delay interval.
2. A circuit arrangement according to claim 1 where said control circuit (24,26,28) includes a regulator circuit (26,28) for generating a switching signal (at pin 6), said circuit arrangement further including a switched mode regulated supply (30) responsive to said switching signal (at pin 6) for creating a source of regulated output voltage (across 30) that substitutes for said first voltage reference device circuit (40) in developing said energizing voltage after elapse of said second delay interval.



3. A circuit arrangement according to claim 1 or 2 wherein said semiconductor element (291) includes a first transistor (291), said stabilized supply voltage (7.5V) biasing one (emitter) of a base and an emitter electrode of said transistor (291), and said input voltage (at pin 10) biasing the other electrode (base).
4. A circuit arrangement according to claim 3 wherein said inhibiting circuit includes a second transistor (294 coupled to said first transistor (291) in a manner that enables current in said second transistor (294) to mirror current in said first transistor (291).
5. A circuit arrangement according to claim 3 or 4 wherein said other electrode (base) is coupled to a junction terminal (10) of a resistive capacitive voltage divider (51A, 53A) of said integrating network (50A) such that a direct current path is provided between said junction terminal (10) and said second voltage reference device circuit (212) via said base and emitter electrodes of said first transistor (291).
6. A circuit arrangement according to claim 5 wherein said biasing arrangement includes a second transistor (213) having its base-emitter path coupled to said second voltage reference device circuit (212) in a series relationship with said direct current path (from pin 10 to pin 13).
7. A circuit arrangement according to any preceding claim, wherein the integrating network (50A) is a series arrangement of a resistive means (51A) and a capacitive means (53A).

Revendications

1. Système de circuit qui fournit un retard de démarrage dans la performance normale du fonctionnement d'un circuit principal (30) comprenant :
un premier circuit de dispositif de référence de tension (40) pour développer une tension d'excitation (sur 36) lors de limitation dudit démarrage ;
un circuit de commande (24, 26, 28) qui est incapable de fournir ladite performance normale dudit fonctionnement de circuit principal jusqu'à ce que une tension d'alimentation qui lui est appliquée atteigne un niveau de fonctionnement ;
une source d'énergie stabilisée (22) incluant un second circuit de dispositif de référence de tension (212) couplé par l'intermédiaire d'un système de polarisation (211) à ladite tension d'excitation (sur 36) pour générer et stabiliser

ladite tension d'alimentation à une borne d'alimentation stabilisée (7,5 V), le niveau de fonctionnement de ladite tension d'alimentation stabilisée étant fonction du niveau de celle dudit second circuit du dispositif de référence de tension (212) et atteignant ledit niveau de fonctionnement après un premier intervalle de retard à partir de ladite initiation dudit démarrage

un circuit d'inhibition (29) couplé audit circuit de commande (24, 26, 28) et incluant un élément semi conducteur (291) dont la conduction peut être commandée en fonction d'une tension d'entrée (sur la broche 10) et de ladite tension d'alimentation stabilisée (7,5 v), ledit circuit d'inhibition (29) empêchant ladite performance normale jusqu'à ce que la tension d'entrée dépasse une valeur de seuil ; et un réseau d'intégration (50 A) couplé audit élément semi conducteur (291) pour fournir ladite tension d'entrée caractérisé en ce que ledit réseau d'intégration (50 A) est couplé audit second circuit de dispositif de référence de tension (211, 212) pour intégrer ladite seconde tension de référence afin que le niveau de ladite tension d'entrée (sur la broche 10) varie durant le démarrage pour dépasser ladite valeur de seuil après disparition d'un second intervalle de retard à partir de l'initiation du démarrage, empêchant ainsi ladite performance normale jusqu'à disparition dudit second intervalle de retard.

2. Système de circuit selon la revendication 1 dans lequel ledit circuit de commande (24, 26, 28) comprend un circuit régulateur (26, 28) pour générer un signal de commutation (sur la broche 6), ledit arrangement de circuit comprenant en outre une alimentation régulée en mode commutée (30) en réponse audit signal de commutation (sur la broche 6) pour créer une source de tension de sortie régulée (sur 30) qui se substitue audit premier circuit de dispositif de référence de tension (40) en développant ladite tension d'excitation après disparition dudit second intervalle de retard.

3. Système de circuit selon la revendication 1 ou 2 dans lequel ledit élément semi-conducteur (291) comprend un premier transistor (291), ladite tension d'alimentation stabilisée (7,5 V) polarisant un (émetteur) d'une base et une électrode d'émetteur dudit transistor (291) et ladite tension d'entrée (sur la broche 10) polarisant l'autre électrode (base).



4. Système de circuit selon la revendication 3 dans lequel ledit circuit d'inhibition comprend un second transistor (294) couplé audit premier transistor (291) de manière à permettre au courant dans ledit second transistor (294) d'être un courant image dans un miroir dudit premier transistor (291). 5
5. Système de circuit selon la revendication 3 ou 4 dans lequel ladite autre électrode (base) est couplée à une borne de jonction (10) d'un diviseur de tension à capacité et résistance (51A, 53 A) dudit réseau d'intégration (50 A) de manière qu'un trajet de courant direct soit fourni entre ladite borne de jonction (10) et ledit second circuit de dispositif de référence de tension (212) via les électrodes de base et d'émetteur dudit premier transistor (291). 10 15
6. Système de circuit selon la revendication 5 dans lequel ledit système de polarisation comprend un second transistor (213) dont le trajet base-émetteur est couplé audit second circuit de dispositif de référence de tension (212), en série avec ledit trajet de courant direct (de la broche 10 à la broche 13). 20 25
7. Système de circuit selon l'une quelconque des revendications précédentes dans lequel le réseau d'intégration (50 A) est un arrangement en série de moyens résistifs (51 A) et de moyens capacitifs (53 A). 30

Patentansprüche

1. Schaltungsanordnung, in welcher eine Einschaltverzögerung für die Normalleistung des Betriebs einer Hauptschaltung (30) vorgesehen ist, mit:
 - einer ersten Spannungsreferenzvorrichtungsschaltung (40) zum Erzeugen einer Erregerspannung (an 36) bei Beginn des Einschaltvorganges; 40
 - einer Steuerschaltung (24, 26, 28), welche so lange außerstande ist, die Normalleistung des Betriebs der Hauptschaltung zu liefern, bis eine ihr zugeführte Versorgungsspannung einen Betriebspegel erreicht; 45
 - einem stabilisierten Netzteil (22) mit einer über eine Vorspannungs-Anordnung (211) mit der Erregerspannung (an 36) verbundenen zweiten Spannungsreferenzvorrichtungsschaltung (212) zum Erzeugen und Stabilisieren der Versorgungsspannung an einem stabilisierten Versorgungsanschluß (7,5 V), wobei der Betriebspegel der stabilisierten Versorgungsspannung auf den Pegel der zweiten Spannungsreferenzvorrichtungsschaltung 50 55

- (212) bezogen ist und den Betriebspegel nach einem ersten Verzögerungsintervall von dem Beginn des Einschaltvorganges ab erreicht; einer mit der Steuerschaltung (24, 26, 28) verbundenen Hemmschaltung (29) mit einem in Übereinstimmung mit einer Eingangsspannung (an Pin 10) und der stabilisierten Versorgungsspannung (7,5 V) in der Leitfähigkeit steuerbaren Halbleiterbaustein (291), wobei die Hemmschaltung (29) die Normalleistung so lange hemmt, bis die Eingangsspannung einen Schwellwert überschreitet; und einem mit dem Halbleiterbaustein (291) verbundenen integrierenden Netzwerk (50A) zum Liefern der Eingangsspannung; dadurch gekennzeichnet, daß das integrierende Netzwerk (50A) mit der zweiten Spannungsreferenzvorrichtungsschaltung (211, 212) verbunden ist zum Integrieren der zweiten Referenzspannung, so daß sich der Pegel der Eingangsspannung (an Pin 10) während des Einschaltvorganges derart ändert, daß der Schwellenpegel nach Ablauf eines zweiten Verzögerungsintervalls vom Beginn des Einschaltvorganges ab überschritten wird, wodurch die Normalleistung bis zum Ablauf des zweiten Verzögerungsintervalls gehemmt wird.
2. Schaltungsanordnung gemäß Anspruch 1, wobei die Steuerschaltung (24, 26, 28) eine Regulatorschaltung (26, 28) zum Erzeugen eines Schaltsignals (an Pin 6) enthält, wobei die Schaltungsanordnung außerdem ein reguliertes Schaltnetzteil (30) enthält, das auf das Schaltsignal (an Pin 6) anspricht, wodurch eine Quelle einer regulierten Ausgangsspannung (über 30) geschaffen wird, die anstelle der ersten Spannungsreferenzvorrichtungsschaltung (40) nach Ablauf des zweiten Verzögerungsintervalls die Erregerspannung erzeugt.
3. Schaltungsanordnung gemäß Anspruch 1 oder 2, wobei das Halbleiterbauteil (291) einen ersten Transistor (291) enthält, wobei die stabilisierte Versorgungsspannung (7,5 V) eine Elektrode (Emitter) von einer Basis- und einer Emittierelektrode des Transistors (291) mit Vorspannung versieht und die Eingangsspannung (an Pin 10) die andere Elektrode (Basis) mit Vorspannung versieht.
4. Schaltungsanordnung gemäß Anspruch 3, wobei die Hemmschaltung einen zweiten Transistor (294) enthält, welcher derart mit dem ersten Transistor (291) verbunden ist, daß der Strom in dem zweiten Transistor (294) den Strom in dem ersten Transistor (291) spiegeln kann.



5. Schaltungsanordnung gemäß Anspruch 3 oder 4, wobei die andere Elektrode (Basis-) mit einem Verbindungsanschluß (10) eines RC-Spannungsteilers (51A, 53A) des integrierenden Netzwerks (50A) derart verbunden ist, daß eine Gleichstrom-Leitungsstrecke zwischen dem Verbindungsanschluß (10) und der zweiten Spannungsreferenzvorrichtungsschaltung (212) über die Basis- und Emittierelektroden des ersten Transistors (291) besteht.

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6. Schaltungsanordnung gemäß Anspruch 5, wobei die Vorspannungs-Anordnung einen zweiten Transistor (213) enthält, dessen Basis-Emitter-Strecke in Reihe mit der Gleichstrom-Leitungsstrecke (von Pin 10 nach Fin 13) mit der zweiten Spannungsreferenzvorrichtungsschaltung (212) verbunden ist.

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7. Schaltungsanordnung gemäß einem der vorstehenden Ansprüche, wobei das integrierende Netzwerk (50A) eine Reihenschaltung von Widerstandsmitteln (51A) und kapazitiven Mitteln (53A) ist.

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* C L M S *