CLAIMS:

1. An Express Traversal (EXTRA) Network on Chip (NoC) comprising a plurality of EXTRA routers, the EXTRA NoC comprising:

a buffer write and route computation (BW/RC) pipeline configured to write an incoming flit to an input buffer of a start EXTRA router and compute a route for the incoming head flit by selecting an output port to depart from the start EXTRA router;

a switch allocation-local (SA-L) pipeline configured to arbitrate the start EXTRA router to choose an input port and an output port for a winning flit;

a setup request (SR) pipeline configured to handle transmission of a plurality of SR signals from the start EXTRA router to downstream EXTRA routers via SR wires;

a switch allocation-global (SA-G) pipeline configured to:

receive the SR signals from the start EXTRA router via the SR wires; and

arbitrate, based on the SR signals received from the start EXTRA router, three signals including: a buffer write enable (BW_{ena}) signal for a local buffered flit, a bypass mux (BM_{sel}) signal for a first crossbar switch, and a crossbar select (XB_{sel}) signal for a second crossbar switch of a selected output port, to build an express path for the winning flit to traverse multiple hops to a destination EXTRA router within one cycle of the start EXTRA router; and

a switch traversal and link traversal (ST/LT) pipeline configured to: traverse the winning flit to the selected output port of the start EXTRA router, and transmit the winning flit to the destination EXTRA router bypassing, via the express path, at least one EXTRA router between the start EXTRA router and destination EXTRA router.

2. The EXTRA NoC according to claim 1 wherein the plurality of SR signals are generated by the SA-L pipeline.

3. The EXTRA NoC according to claim 1 wherein the plurality of SR signals are generated by the SR pipeline.

4. The EXTRA NoC according to claim 1 further comprising a plurality of registers inserted between any two adjacent pipelines of the BW/RC, SA-L, SR, SA-G, and ST/LT pipelines.

5. The EXTRA NoC according to claim 4, wherein the plurality of registers are clocked synchronously.

6. A method of traversing flits in an Express Traversal (EXTRA) Network on Chip (NoC) having a plurality of EXTRA routers, the method comprising:

(A) in a buffer write and route computation (BW/RC) pipeline:

writing an incoming flit to an input buffer(s) of a start EXTRA router, and

computing a route for the incoming head flit by selecting an output port to depart from the start EXTRA router;

(B) in a switch allocation-local (SA-L) pipeline:

arbitrating the start EXTRA router to choose an input port and an output port for a winning flit;

(C) in a setup request (SR) pipeline:

handling transmission of a plurality of SR signals from the start EXTRA router to downstream EXTRA routers via SR wires;

(D) in a switch allocation-global (SA-G) pipeline:

receiving the SR signals from the start EXTRA router via the SR wires, and

arbitrating, based on the SR signals received from the start EXTRA router, three signals including: a buffer write enable (BW_{ena}) signal for a local buffered flit, a bypass mux (BM_{sel}) signal for a first crossbar switch, and a crossbar select (XB_{sel}) signal for a second crossbar switch of a selected output port, to build an express path for the winning flit to traverse multiple hops to a destination EXTRA router within one cycle of the start EXTRA router; and

(E) in a switch traversal and link traversal (ST/LT) pipeline:

traversing the winning flit to the selected output port of the start EXTRA router,

transmiting the winning flit to a destination EXTRA router, and

bypassing, via the express path, at least one EXTRA router between the start EXTRA router and destination EXTRA router.

7. The method according to claim 6 wherein the plurality of SR signals are generated by the SA-L pipeline.

8. The method according to claim 6 wherein the plurality of SR signals are generated by the SR pipeline.

9. The method according to claim 6 wherein a time period of the pipelines are regulated by a plurality of registers inserted between any two adjacent pipelines of the BW/RC, SA-L, SR, SA-G, and ST/LT pipelines.

10. The method according to claim 9, wherein the plurality of registers are clocked synchronously.