Multi-layer Substrate For Semiconductor Packaging

Field of Invention

[001] The present invention relates to multi-layer substrates for semiconductor packaging and methods of manufacturing such substrates.

Background

[002] Conventional semiconductor dies are mounted on leadframes. These leadframes are usually formed by coating a copper substrate with a photoresist layer, exposing a pattern on the photoresist layer using a mask, positively or negatively removing the photoresist layer and then etching away the copper to give a patterned leadframe. However, such a patterned leadframe formed by etching is not suitable for use with dies that require finer and closer conductive traces than conventional leadframe. Etching inherently causes undercutting and fine conductive traces thus formed may have reliability issue for high throughput manufacturing.

[003] US Patent No. 7,795,071, assigned to Advanpack Solutions, describes a method for forming a single-layer patterned substrate for semiconductor packaging. A gang of patterned conductor layouts is formed on a steel carrier, and insulating material is injected in a mold cavity to seal the conductive traces of the patterned conductor layouts. After removing the steel carrier, a substrate containing a gang of patterned conductor layouts, is formed. Advantageously, the patterned conductor layouts are embedded or recessed in the insulating material of the substrate such that finer and closer conductive traces are fabricated effectively. The patterned conductor layouts are electrically isolated from each other, whereas on a conventional leadframe, each conductor layout corresponding to each die is electrically connected to an adjacent layout.

[004] It can thus be seen that there exists a need to form a multi-layer substrate with more complex routing of conductive traces to support future designs of integrated circuits. Advantageously, these multi-layer substrates allow separate conductor layers to be used for signal, power, digital, analogue circuits and so on.