

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:
 - a body conductive layer including a cell array portion and a peripheral circuit portion;
 - an electrode structure on the cell array portion of the body conductive layer, the electrode structure including a plurality of electrodes that are stacked on top of each other;
 - vertical structures penetrating the electrode structure, the vertical structures connected to the cell array portion of the body conductive layer;
 - a residual substrate on the peripheral circuit portion of the body conductive layer;and
 - a connection conductive pattern penetrating the residual substrate, the connection conductive pattern connected to the peripheral circuit portion of the body conductive layer;
 - wherein the body conductive layer includes a polycrystalline semiconductor layer.
2. The semiconductor memory device of claim 1, wherein
 - the connection conductive pattern contacts a top surface of the body conductive layer,
 - a width of a lower portion of the connection conductive pattern is less than a width of an upper portion of the connection conductive pattern, and
 - the lower portion of the connection conductive pattern is in contact with the top surface of the body conductive layer.
3. The semiconductor memory device of claim 1, wherein a bottom surface of the connection conductive pattern is disposed at substantially a same level as a top surface of the body conductive layer.

4. The semiconductor memory device of claim 1, wherein
the residual substrate includes a peripheral active layer on a buried insulation layer,
and
the connection conductive pattern penetrates the buried insulation layer and the
peripheral active layer.
5. The semiconductor memory device of claim 4, wherein the peripheral active
layer is substantially single-crystalline.
6. The semiconductor memory device of claim 1, wherein a top surface of the
connection conductive pattern is at a higher level than a top surface of the residual substrate.
7. The semiconductor memory device of claim 6, further comprising:
a peripheral gate electrode on the residual substrate, wherein
the top surface of the connection conductive pattern is at a higher level than a top
surface of the peripheral gate electrode.
8. The semiconductor memory device of claim 1, further comprising:
an insulating spacer between a sidewall of the connection conductive pattern and the
residual substrate.
9. The semiconductor memory device of claim 1, further comprising:
a through-electrode penetrating the peripheral circuit portion of the body conductive
layer, wherein
the through-electrode is connected to the connection conductive pattern.

10. The semiconductor memory device of claim 1, wherein the connection conductive pattern includes dopants, and a conductivity type of the dopants in the connection conductive pattern is the same as a conductivity type of the body conductive layer.
11. The semiconductor memory device of claim 1, wherein a thickness of the body conductive layer is less than a thickness of the residual substrate.
12. The semiconductor memory device of claim 1, wherein each of the vertical structures includes a channel semiconductor layer and a data storage layer, and the body conductive layer is connected to the channel semiconductor layer.
13. The semiconductor memory device of claim 12, wherein a bottom surface of the channel semiconductor layer and a bottom surface of the data storage layer are at substantially a same level.
14. The semiconductor memory device of claim 13, wherein a bottom surface of the connection conductive pattern is at substantially a same level as the bottom surface of the channel semiconductor layer.
15. A semiconductor memory device comprising:
a body conductive layer including a cell array portion and a peripheral circuit portion;

an electrode structure on the cell array portion of the body conductive layer, the electrode structure including a plurality of electrodes stacked on top of each other;

vertical structures penetrating the electrode structure,

the vertical structures connected to the cell array portion of the body conductive layer;

a residual substrate on the peripheral circuit portion of the body conductive layer; and

a connection conductive pattern penetrating the residual substrate,

the connection conductive pattern connected to the body conductive layer, and

a bottom surface of the connection conductive pattern is at substantially a same level as bottom surfaces of the vertical structures;

wherein the body conductive layer includes a polycrystalline semiconductor layer.

16. The semiconductor memory device of claim 15, wherein
the residual substrate includes a peripheral active layer on a buried insulation layer,
and
the connection conductive pattern penetrates the peripheral active layer.

17. The semiconductor memory device of claim 16, wherein a sidewall of the connection conductive pattern is connected to the peripheral active layer.

18. The semiconductor memory device of claim 15, wherein
the bottom surface of the connection conductive pattern is electrically and physically connected to a top surface of the body conductive layer.

19. The semiconductor memory device of claim 15, wherein
the connection conductive pattern includes dopants, and a conductivity type of the

dopants in the connection conductive pattern is the same as a conductivity type of the body conductive layer.

20. The semiconductor memory device of claim 1, wherein the residual substrate includes a single-crystalline layer.