

LIGHT-EMITTING DIODE AND METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

5 Field of the Invention

[0001]

The present invention relates to a light-emitting diode and a method of manufacturing the same.

Priority is claimed on Japanese Patent Application No. 2011-277536, filed on
10 December 19, 2011, the content of which is incorporated herein by reference.

Description of Related Art

[0002]

A point light source type light-emitting diode is known in which light generated
15 by a light-emitting layer is extracted from a portion of the upper surface of an element.
In this type of light-emitting diode, a light-emitting diode is known which has a current
blocking structure for limiting an electrically conductive region of a light-emitting layer
to a portion of the plane of the light-emitting layer (for example, see Patent Document 1).
In the light-emitting diode having the current blocking structure, a light-emitting region
20 is limited. Since light is emitted from a light emission hole which is provided
immediately above this light-emitting region, it is possible to obtain a high light output
and to input the emitted light to, for example, an optical component with high efficiency.

[0003]

In the point-light-source-type light-emitting diode, a structure is known in which
25 an active layer has a pillar structure in order to narrow a light-emitting region in a

direction parallel to a substrate and a layer including a light emission opening (light emission hole) is provided on a light emission surface of the top of the pillar structure (for example, see Patent Document 2).

FIG. 15 shows a resonator-type light-emitting diode in which a lower mirror layer 132, an active layer 133, an upper mirror layer 134, and a contact layer 135 are sequentially formed on a substrate 131; a pillar structure 137 includes the active layer 133, the upper mirror layer 134, and the contact layer 135; the pillar structure 137 and the periphery thereof are covered with a protective film 138; an electrode film 139 is formed on the protective film 138; and a light emission opening 139a is formed in the electrode film 139 on the top surface 137a (light emission surface) of the pillar structure 137. Reference numeral 140 indicates a rear surface electrode.

Prior Art Documents

Patent Documents

[0004]

[Patent Document 1] Japanese Unexamined Patent Application, First Publication No. 2003-31842

[Patent Document 2] Japanese Unexamined Patent Application, First Publication No. 9-283862

SUMMARY OF THE INVENTION

[0005]

When the pillar structure is formed, a portion other than the pillar structure is removed by anisotropic dry etching after the active layer is formed. Therefore, as shown in FIG. 15, a side surface 137b of the pillar structure 137 is vertical or steeply inclined with respect to the substrate 131. In general, a protective film is formed on the

side surface of the pillar structure by a vapor deposition method or a sputtering method and an electrode metal (for example, Au) film is formed on the side surface by a vapor deposition method. However, it is not easy to form the protective film or the electrode metal film on the vertical side surface or the steeply inclined side surface with a uniform thickness and the protective film or the electrode metal film is likely to be a discontinuous film. When the protective film is a discontinuous film (letter A in FIG. 15), the electrode metal film enters the discontinuous portion and contacts the active layer, which causes the leakage of light. In addition, when the electrode metal film is the discontinuous film (letter B in FIG. 15), an electrical conduction failure occurs.

[0006]

When the portion other than the pillar structure is removed by dry etching, an expensive apparatus is required and the etching time increases.

[0007]

In the point-light-source-type light-emitting diode as shown in FIG. 15 in which the light emission hole is provided on the top surface of the pillar structure, a current flows in the entire light-emitting layer of the pillar structure. Therefore, a large amount of light is emitted from a portion other than the portion which is arranged immediately below the light emission hole in the light-emitting layer, and the light which is emitted from the portion other than the portion which is arranged immediately below the light emission hole is less likely to be emitted to the outside of the light-emitting diode than light emitted from the portion which is arranged immediately below the light emission hole. Therefore, light extraction efficiency is not improved.

[0008]

The invention has been made in view of the above-mentioned problems and an object of the invention is to provide a light-emitting diode in which a protective film and

an electrode film formed on the protective film are formed with a uniform thickness and which has high light extraction efficiency, and a light-emitting diode producing method which can reduce leakage or electrical conduction failure, improve yield, and produce a light-emitting diode at a lower cost than in the related art.

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[0009]

The invention provides the following means.

- (1) A light-emitting diode that outputs light from a light emission hole to the outside, comprising: a reflecting layer that consists of metal; a transparent film; and a compound semiconductor layer that sequentially includes an active layer and a contact layer; on a supporting substrate in this order, wherein a flat portion and a mesa structure portion including an inclined side surface and a top surface are provided in an upper part of the light-emitting diode, at least a part of the flat portion and at least a part of the mesa structure portion are sequentially covered with a protective film and an electrode film,
- 10 the mesa structure portion includes at least a portion of the active layer, the inclined side surface is formed by wet etching, a cross-sectional area of the mesa structure portion in a horizontal direction is continuously reduced toward the top surface, the protective film covers at least a part of the flat portion, the inclined side surface of the mesa structure portion, and a peripheral region of the top surface of the mesa structure portion and
- 15 includes an electrical conduction window which is provided inside the peripheral region in plane view and is arranged around the light emission hole and from which a portion of a surface of the compound semiconductor layer is exposed, the electrode film is a continuous film that comes into direct contact with the surface of the compound semiconductor layer which is exposed from the electrical conduction window, covers at
- 20 least a portion of the protective film formed on the flat portion, and has the light emission
- 25

hole on the top surface of the mesa structure portion, the transparent film is formed between the reflecting layer and the compound semiconductor layer, and a through-electrode is provided in a range of the transparent film which overlaps the light emission hole in plane view so as to come into contact with the compound semiconductor layer and the reflecting layer.

(2) A light-emitting diode that outputs light from a light emission hole to the outside, comprising: a reflecting layer that consists of metal; a transparent film; and a compound semiconductor layer that sequentially includes an active layer and a contact layer; on a supporting substrate in this order, wherein a flat portion and a mesa structure portion including an inclined side surface and a top surface are provided in an upper part of the light-emitting diode, at least a part of the flat portion and at least a part of the mesa structure portion are sequentially covered with a protective film and an electrode film, the mesa structure portion includes at least a portion of the active layer, the inclined side surface is formed by wet etching, a cross-sectional area of the mesa structure portion in a horizontal direction is continuously reduced toward the top surface, the protective film covers at least a part of the flat portion, the inclined side surface of the mesa structure portion, and a peripheral region of the top surface of the mesa structure portion and includes an electrical conduction window which is provided inside the peripheral region in plane view and is arranged around the light emission hole and from which a portion of a surface of the compound semiconductor layer is exposed, the electrode film is a continuous film that comes into direct contact with the surface of the compound semiconductor layer which is exposed from the electrical conduction window, covers at least a portion of the protective film formed on the flat portion, and has the light emission hole on the top surface of the mesa structure portion, the transparent film is formed between the reflecting layer and the compound semiconductor layer, and a

through-electrode is provided in the transparent film at a position that overlaps the electrical conduction window in plane view so as to come into contact with the compound semiconductor layer and the reflecting layer.

(3) In the aspect stated in the above (1), the through-electrode may be formed in a range of a reduced and projected figure of the light emission hole which is reduced and projected onto the transparent film by extending a segment that connects each point on the outer circumference of the electrical conduction window and each point on the outer circumference of a figure obtained by projecting the light emission hole onto the active layer at the shortest distance.

(4) In the aspect stated in the above any one of (1) to (3), the through-electrode may consist of AuBe or AuZn.

(5) In the aspect stated in the above any one of (1) to (4), the transparent film may consist of any one of SiO₂, SiN, SiON, Al₂O₃, MgF₂, TiO₂, TiN, and ZnO.

(6) In the aspect stated in the above any one of (1) to (5), the contact layer may come into contact with the electrode film.

(7) In the aspect stated in the above any one of (1) to (6), the mesa structure portion may have a rectangular shape in plane view.

(8) In the aspect stated in the above (7), each inclined side surface of the mesa structure portion may be formed so as to be offset from an orientation flat of the substrate.

(9) In the aspect stated in the above any one of (1) to (8), the mesa structure portion may have a height of 3 μm to 7 μm , and the width of the inclined side surface in plane view may be in the range of 0.5 μm to 7 μm .

(10) In the aspect stated in the above any one of (1) to (9), the light emission hole may have a circular shape or an elliptical shape in plane view.

(11) In the aspect stated in the above (10), the light emission hole may have a diameter of 50 μm to 150 μm .

(12) In the aspect stated in the above any one of (1) to (11), a bonding wire may be provided on the flat portion of the electrode film.

5 (13) In the aspect stated in the above any one of (1) to (12), a light-emitting layer that is included in the active layer may have a multiple quantum well structure.

(14) In the aspect stated in the above any one of (1) to (13), the light-emitting layer that is included in the active layer may consist of any one of $(\text{Al}_{X1}\text{Ga}_{1-X1})_{Y1}\text{In}_{1-Y1}\text{P}$ ($0 \leq X1 \leq 1$, $0 < Y1 \leq 1$), $(\text{Al}_{X2}\text{Ga}_{1-X2})\text{As}$ ($0 \leq X2 \leq 1$), and $(\text{In}_{X3}\text{Ga}_{1-X3})\text{As}$ ($0 \leq X3 \leq 1$).

10 (15) A method for producing a light-emitting diode that includes a reflecting layer made of metal, a transparent film, and a compound semiconductor layer sequentially including an active layer and a contact layer, which are sequentially provided on a supporting substrate, in this order, and that emits light from a light emission hole to the outside, the method comprising: a step of forming the compound
15 semiconductor layer that sequentially includes the contact layer and the active layer on a growth substrate; a step of forming the transparent film and forming a through-electrode in a range of the transparent film which overlaps the light emission hole to be formed in plane view so as to come into contact with the compound semiconductor layer and the reflecting layer, on the compound semiconductor layer; a step of forming the reflecting
20 layer made of metal on the transparent film and the through-electrode; a step of bonding the supporting substrate to the reflecting layer; a step of removing the growth substrate; a step of performing wet etching for the compound semiconductor layer to form a mesa structure portion which is formed such that a cross-sectional area thereof in a horizontal direction is continuously reduced toward a top surface and a flat portion which is
25 arranged around the mesa structure portion; a step of forming a protective film that

covers, at least, a part of the flat portion, the inclined side surface of the mesa structure portion, and a peripheral region of the top surface of the mesa structure portion, and that includes an electrical conduction window which is provided inside the peripheral region and is arranged around the light emission hole in plane view and from which a portion of
5 a surface of the compound semiconductor layer is exposed; and a step of forming an electrode film which is a continuous film that comes into direct contact with the surface of the compound semiconductor layer exposed from the electrical conduction window, that covers at least a portion of the protective film formed on the flat portion, and that has the light emission hole on the top surface of the mesa structure portion.

- 10 (16) A method for producing a light-emitting diode that includes a reflecting layer made of metal, a transparent film, and a compound semiconductor layer sequentially including an active layer and a contact layer, which are sequentially provided on a supporting substrate, in this order and that emits light from a light emission hole to the outside, the method comprising: a step of forming the compound
15 semiconductor layer that sequentially includes the contact layer and the active layer on a growth substrate; a step of forming the transparent film and forming a through-electrode in the transparent film at a position that overlaps an electrical conduction window to be formed in plane view so as to come into contact with the compound semiconductor layer and the reflecting layer, on the compound semiconductor layer; a step of forming the
20 reflecting layer made of metal on the transparent film and the through-electrode; a step of bonding the supporting substrate to the reflecting layer; a step of removing the growth substrate; a step of performing wet etching for the compound semiconductor layer to form a mesa structure portion which is formed such that a cross-sectional area thereof in a horizontal direction is continuously reduced toward a top surface and a flat portion
25 which is arranged around the mesa structure portion; a step of forming a protective film

that covers, at least, a part of the flat portion, the inclined side surface of the mesa structure portion, and a peripheral region of the top surface of the mesa structure portion, and that includes the electrical conduction window which is provided inside the peripheral region and is arranged around the light emission hole in plane view and from which a portion of a surface of the compound semiconductor layer is exposed; and a step of forming an electrode film which is a continuous film that comes into direct contact with the surface of the compound semiconductor layer exposed from the electrical conduction window, that covers at least a portion of the protective film formed on the flat portion, and that has the light emission hole on the top surface of the mesa structure portion.

(17) In the aspect stated in the above (15) or (16), the wet etching may be performed with at least one of a mixture of phosphoric acid, hydrogen peroxide, and water, a mixture of ammonia, hydrogen peroxide, and water, a mixture of bromine and methanol, and a mixture of potassium iodide and ammonia.

[0010]

A light-emitting diode according to an aspect of the invention includes a reflecting layer that consists of metal, a transparent film, and a compound semiconductor layer sequentially including an active layer and a contact layer, which are sequentially provided on a supporting substrate, and outputs light from a light emission hole to the outside. A protective film includes an electrical conduction window which is provided inside a peripheral region of a top surface of a mesa structure portion and is arranged around the light emission hole and from which a portion of a surface of the compound semiconductor layer is exposed. An electrode film comes into direct contact with the surface of the compound semiconductor layer which is exposed from the electrical

conduction window. A through-electrode (penetrating electrode, penetration electrode) is provided in a range of the transparent film which overlaps the light emission hole in plane view so as to come into contact with the compound semiconductor layer and the reflecting layer. As a result, a current is concentrated between the through-electrode and a portion of the electrode film which fills the electrical conduction window. Then, the amount of light emitted from a portion of the active layer which is arranged immediately below the light emission hole is more than the amount of light emitted from a portion other than the portion which is arranged immediately below the light emission hole. As a result, the percentage of light which travels toward the light emission hole increases and light extraction efficiency is improved.

The light-emitting diode according to the aspect of the invention includes the flat portion and the mesa structure portion including the inclined side surface and the top surface that are provided in its upper part. As a result, it is possible to obtain a high light output and to input the emitted light to, for example, an optical component with high efficiency.

In the light-emitting diode according to the invention, the inclined side surface of the mesa structure portion is formed by wet etching such that the cross-sectional area thereof in the horizontal direction is continuously reduced toward the top surface. As a result, it is easy to sequentially form the protective film and the electrode film on the side surface of the mesa structure portion, as compared to a case in which the mesa structure portion has a vertical side surface. Therefore, a continuous film with a uniform thickness is formed. As a result, leakage or electrical conduction failure caused by a discontinuous film does not occur and stable and high-brightness light emission is ensured. This effect is obtained by the mesa structure portion with the inclined side surface which is formed by wet etching, regardless of the internal laminated structure of

the light-emitting diode or the structure of the substrate.

[0011]

A light-emitting diode according to an aspect of the invention includes a reflecting layer that is made of metal, a transparent film, and a compound semiconductor layer sequentially including an active layer and a contact layer, which are sequentially provided on a supporting substrate, and outputs light from a light emission hole to the outside. A through-electrode is provided in the transparent film at a position that overlaps an electrical conduction window in plane view so as to come into contact with the compound semiconductor layer and the reflecting layer. As a result, a current is concentrated between the through-electrode and a portion of an electrode film which fills the electrical conduction window. Then, the amount of light emitted from a portion of the active layer which is arranged immediately below the electrical conduction window is more than the amount of light emitted from a portion other than the portion which is arranged immediately below the electrical conduction window. As a result, the percentage of light which travels toward the light emission hole increases and light extraction efficiency is improved.

[0012]

In the light-emitting diode according to the aspect of the invention, the through-electrode is formed in a range of a reduced and projected figure of the light emission hole which is reduced and projected onto the transparent film by extending a segment that connects each point on the outer circumference of the electrical conduction window and each point on the outer circumference of a figure obtained by projecting the light emission hole onto the active layer at the shortest distance. As a result, the amount of light emitted from a portion of the active layer which is arranged immediately below a range narrower than the range that overlaps the light emission hole is more than the

amount of light emitted from a portion other than the portion which is arranged immediately below the range. As a result, the percentage of light which travels toward the light emission hole further increases and the light extraction efficiency is further improved.

5 [0013]

In the light-emitting diode according to the aspect of the invention, the through-electrode is made of AuBe or AuZn. As a result, contact resistance with the compound semiconductor layer and the reflecting layer is reduced and low-voltage driving can be performed.

10 [0014]

In the light-emitting diode according to the aspect of the invention, the transparent film is made of any one of SiO₂, SiN, SiON, Al₂O₃, MgF₂, TiO₂, TiN, and ZnO. As a result, high transmittance of light reflected from the reflecting layer is ensured and a high output is obtained.

15 [0015]

In the light-emitting diode according to the aspect of the invention, the contact layer comes into contact with the electrode film. As a result, the contact resistance of an ohmic electrode is reduced and low-voltage driving can be performed.

[0016]

20 In the light-emitting diode according to the aspect of the invention, the mesa structure portion has a rectangular shape in plane view. As a result, a change in the shape of a mesa, which depends on an etching depth, due to the influence of the anisotropy of wet etching during production is prevented. Therefore, it is easy to control the area of a mesa portion and a high-accuracy dimensional shape is obtained.

25 [0017]

In the light-emitting diode according to the aspect of the invention, each inclined side surface of the mesa structure portion is formed so as to be offset from an orientation flat of the substrate. As a result, the influence of anisotropy on four sides of the rectangular mesa structure portion due to the orientation of the substrate is reduced and
5 uniform mesa shape and gradient are obtained.

[0018]

In the light-emitting diode according to the aspect of the invention, the mesa structure portion has a height of 3 μm to 7 μm and the width of the inclined side surface in plane view is in the range of 0.5 μm to 7 μm . As a result, it is easy to sequentially
10 form the protective film and the electrode film on the side surface, as compared to the case in which the mesa structure portion has a vertical side surface. Therefore, a continuous film with a uniform thickness is formed. As a result, leakage or electrical conduction failure caused by a discontinuous film does not occur and stable and high-brightness light emission is ensured.

15 [0019]

In the light-emitting diode according to the aspect of the invention, the light emission hole has a circular shape or an elliptical shape in plane view. As a result, it is easy to form a uniform contact region, as compared to a structure in which the light emission hole has an angular shape, such as a rectangular shape, and it is possible to
20 prevent, for example, the concentration of a current on the corner. In addition, this structure is suitable for coupling to a fiber in a light-receiving side.

[0020]

In the light-emitting diode according to the aspect of the invention, the light emission hole has a diameter of 50 μm to 150 μm . As a result, when the diameter is
25 less than 50 μm , current density increases in the mesa structure portion and an output is

saturated with a small amount of current. In contrast, when the diameter is greater than 150 μm , it is difficult to diffuse the current to the entire mesa structure portion.

Therefore, the problem of output saturation is solved.

[0021]

5 In the light-emitting diode according to the aspect of the invention, a bonding wire is provided in a flat portion of the electrode film. As a result, since wire bonding is performed on the flat portion to which a sufficient load (and ultrasonic waves) is applied, wire bonding with high bonding strength is achieved.

[0022]

10 In the light-emitting diode according to the aspect of the invention, a light-emitting layer that is included in the active layer has a multiple quantum well structure. As a result, a sufficient number of injected carriers are confined in a well layer and current density in the well layer increases. Therefore, the radiative recombination probability increases and a response speed increases.

15 [0023]

According to an aspect of the invention, a method is provided for producing a light-emitting diode that includes a reflecting layer that consists of metal, a transparent film, and a compound semiconductor layer sequentially including an active layer and a contact layer, which are sequentially provided on a supporting substrate, and emits light
20 from a light emission hole to the outside. The method includes a step of forming the compound semiconductor layer that sequentially includes the contact layer and the active layer on a growth substrate and a step of forming the transparent film on the compound semiconductor layer and forming a through-electrode in a range of the transparent film which overlaps the light emission hole to be formed in plane view so as to come into
25 contact with the compound semiconductor layer and the reflecting layer. As a result, a

current is concentrated between the through-electrode and a portion, which fills an electrical conduction window, of an electrode film. Then, the amount of light emitted from a portion, which is arranged immediately below the light emission hole, of the active layer is more than the amount of light emitted from other portion of the active layer. As a result, the ratio of light which travels toward the light emission hole increases and it is possible to manufacture a light-emitting diode with high light extraction efficiency.

The method for producing a light-emitting diode according to the invention includes a step of bonding the supporting substrate to the reflecting layer and a step of removing the growth substrate. As a result, It is possible to avoid the absorption of light by the growth substrate, such as a GaAs substrate which is generally used as the growth substrate for the compound semiconductor layer, and it is possible to manufacture a light-emitting diode with a high light emission output.

The method of manufacturing a light-emitting diode according to the invention includes: a step of performing wet etching for the compound semiconductor layer to form a mesa structure portion which is formed such that a cross-sectional area thereof in a horizontal direction is continuously reduced toward a top surface and a flat portion which is arranged around the mesa structure portion; a step of forming a protective film on the flat portion and the mesa structure portion such that an electrical conduction window from which a portion of a surface of the compound semiconductor layer is exposed is formed on the top surface of the mesa structure portion; and a step of forming an electrode film which is a continuous film that comes into direct contact with the surface of the compound semiconductor layer exposed from the electrical conduction window, covers at least a portion of the protective film formed on the flat portion, and has the light emission hole on the top surface of the mesa structure portion. As a result, it is possible

to obtain a high light emission output and to input the emitted light to, for example, an optical component with high efficiency. In addition, it is easy to sequentially form the protective film and the electrode film on the inclined side surface, as compared to the case in which the mesa structure portion has a vertical side surface. Therefore, a continuous film with a uniform thickness is formed. As a result, it is possible to manufacture a light-emitting diode which does not have leakage or electrical conduction failure caused by a discontinuous film and ensures stable and high-brightness light emission. When the pillar structure is formed by anisotropic dry etching as in the related art, the side surface is vertically formed. However, when the mesa structure portion is formed by wet etching, it is possible to form a side surface which is gently inclined. In addition, when the mesa structure portion is formed by wet etching, it is possible to reduce the manufacturing time, as compared to the case in which the pillar structure is formed by dry etching as in the related art.

[0024]

According to an aspect of the invention, a method is provided for producing a light-emitting diode that includes a reflecting layer that consists of metal, a transparent film, and a compound semiconductor layer sequentially including an active layer and a contact layer, which are sequentially provided on a supporting substrate, and emits light from a light emission hole to the outside. The method includes a step of forming the compound semiconductor layer that sequentially includes the contact layer and the active layer on a growth substrate and a step of forming the transparent film and forming a through-electrode in the transparent film at a position that overlaps an electrical conduction window to be formed in plane view so as to come into contact with the compound semiconductor layer and the reflecting layer on the compound semiconductor layer. As a result, the amount of light emitted from a portion, which is arranged

immediately below the electrical conduction window, of the active layer is more than the amount of light emitted from a portion, other than the portion which is arranged immediately below the electrical conduction window, of the active layer. Therefore, the percentage of light which travels toward the light emission hole increases and it is possible to produce a light-emitting diode with high light extraction efficiency.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025]

FIG. 1 is a schematic cross-sectional view illustrating a light-emitting diode according to a first embodiment of the invention.

FIG. 2 is a perspective view illustrating the light-emitting diode according to the first embodiment of the invention.

FIG. 3 is an electron micrograph illustrating the cross-section of an inclined surface of a mesa structure portion of the light-emitting diode according to the invention.

FIG. 4 is an enlarged cross-sectional view illustrating the vicinity of a through-electrode and an electrical conduction window of the light-emitting diode according to the first embodiment of the invention.

FIG. 5 is a schematic cross-sectional view illustrating an active layer of the light-emitting diode according to the first embodiment of the invention.

FIG. 6 is an enlarged cross-sectional view illustrating the vicinity of a through-electrode and an electrical conduction window of a light-emitting diode according to a second embodiment of the invention.

FIG. 7 is a schematic cross-sectional view illustrating a light-emitting diode according to a third embodiment of the invention.

FIG. 8 is a process cross-sectional view illustrating an example of a process of manufacturing a metal substrate used as a supporting substrate according to the

invention.

FIG. 9 is a schematic cross-sectional view illustrating a method of manufacturing the light-emitting diode according to the first embodiment of the invention.

5 FIG. 10A is a process cross-sectional view illustrating an example of the method of manufacturing the light-emitting diode according to the first embodiment of the invention.

 FIG. 10B is a process cross-sectional view illustrating an example of a method of manufacturing a light-emitting diode according to a modification example of the first
10 embodiment of the invention.

FIG. 11 is a process cross-sectional view illustrating an example of the method of manufacturing the light-emitting diode according to the first embodiment of the invention.

 FIG. 12 is a process cross-sectional view illustrating an example of the method
15 of manufacturing the light-emitting diode according to the first embodiment of the invention.

FIG. 13 is a graph illustrating the relationship between a depth, a width, and the etching time for wet etching.

 FIG. 14 is a plane view illustrating an electrical conduction window of a
20 protective film of the light-emitting diode according to the first embodiment of the invention.

FIG. 15 is a cross-sectional view illustrating a light-emitting diode according to the related art.

Description of Embodiments

25 [0026]

Hereinafter, the structure of a light-emitting diode and a method for producing the same according to the invention will be described with reference to the drawings. In the drawings used in the following description, in some cases, for ease of understanding of characteristics, a characteristic portion is enlarged and the dimensions and scale of each component are different from the actual dimensions and scale. For example, materials and dimensions which are exemplified in the following description are illustrative and the invention is not limited thereto. Various modifications and changes of the invention can be made without departing from the scope and spirit of the invention.

The invention may include layers which are not described in the following as long as the effect of the invention is maintained.

[0027]

[Light-emitting Diode (First Embodiment)]

FIG. 1 is a schematic cross-sectional view illustrating an example of a light-emitting diode to which the invention is applied. FIG. 2 is a perspective view illustrating the light-emitting diode formed on a wafer including the light-emitting diode shown in FIG. 1.

Hereinafter, a light-emitting diode according to an embodiment of the invention will be described in detail with reference to FIGS. 1 and 2.

[0028]

A light-emitting diode 100 shown in FIG. 1 includes a reflecting layer 2 that consists of metal, a transparent film 30, and a compound semiconductor layer 20 (see FIG. 4) that includes an active layer 4 and a contact layer 5 in this order, which are sequentially provided on a supporting substrate 1, and emits light from a light emission hole 9b to the outside. The light-emitting diode includes a flat portion 6 and a mesa

structure portion 7 including an inclined side surface 7a and a top surface 7b in its upper part. The flat portion 6 and the mesa structure portion 7 are at least partially covered with a protective film 8 and an electrode film 9, respectively. The mesa structure portion 7 includes at least a portion of the active layer 4. The inclined side surface 7a is
5 formed by wet etching so that the cross-sectional area thereof in the horizontal direction is continuously reduced toward the top surface 7b. The protective film 8 covers at least a portion of the flat portion 6, the inclined side surface 7a of the mesa structure portion 7, and a peripheral region 7ba of the top surface 7b of the mesa structure portion 7. In addition, the protective film 8 includes an electrical conduction window 8b which is
10 provided around the light emission hole 9b inside the peripheral region 7ba in plane view and from which a portion of the surface of the compound semiconductor layer 20 (contact layer 5) is exposed. The electrode film 9 comes into contact with the surface of the compound semiconductor layer 20 (contact layer 5) exposed from the electrical conduction window 8b. The electrode film 9 is a continuous film which is formed so as
15 to cover at least a portion of the protective film 8 formed on the flat portion 6 and to have the light emission hole 9b on the top surface 7b of the mesa structure portion 7. The transparent film 30 is formed between the reflecting layer 2 and the compound semiconductor layer 20. A through-electrode 31 is formed in the transparent film 30 so as to come into contact with the compound semiconductor layer 20 and the reflecting
20 layer 2 in the range which overlaps the light emission hole 9b in plane view. In addition, a bonding (contact) layer 3 is provided between the reflecting layer 2 and the active layer 4.

In the light-emitting diode according to this embodiment, the mesa structure portion 7 has a rectangular shape in plane view and the light emission hole 9b of the
25 electrode film 9 has a circular shape in plane view. The shape of the mesa structure

portion 7 in plane view is not limited to a rectangle and the shape of the light emission hole 9b in plane view is not limited to a circle.

A light leakage prevention film 16 for preventing the leakage of light from the side surface is provided on the electrode film of the mesa structure portion 7.

5 In addition, a back electrode (lower electrode) 40 is provided on the lower surface of the substrate 1.

[0029]

As shown in FIG. 2, the light-emitting diode according to the invention can be produced by forming a plurality of light-emitting diodes 100 on a wafer-shaped substrate and cutting the wafer-shaped substrate into each light-emitting diode along streets (lines
10 scheduled to be cut) 21 (a one-dot chain line 22 is a center line of the street 21 in the longitudinal direction). That is, a laser beam or a blade contacts the streets 21 along the one-dot chain line 22 to cut the wafer-shaped substrate into each light-emitting diode.

[0030]

15 The mesa structure portion 7 protrudes upward from the flat portion 6 and includes the inclined side surface 7a and the top surface 7b. In the example shown in FIG. 1, the inclined side surface 7a consists of the inclined cross-sectional surface of the entire active layer 4 and the inclined cross-sectional surface of the contact layer 5. The protective film 8, the electrode film (upper electrode film) 9, and the light leakage
20 prevention film 16 are sequentially provided on the inclined side surface 7a. The top surface 7b consists of the surface of the contact layer 5. The protective film 8 (portions denoted by reference numeral 8ba and 8d) and the electrode film 9 (portions denoted by reference numerals 9ba, 9bb and 9d) are provided on the top surface 7b.

[0031]

25 The contact layer 5 and at least a portion of the active layer 4 are included in the

mesa structure portion 7 according to the invention.

In the example shown in FIG. 1, the contact layer 5 and the entire active layer 4 are included in the mesa structure portion 7. Only a portion of the active layer 4 may be included in the mesa structure portion 7. It is preferable that the entire active layer 4 are included in the mesa structure portion 7. The reason is that light emitted in the active layer 4 is all generated in the mesa structure portion and light extraction efficiency is improved.

[0032]

The inclined side surface 7a of the mesa structure portion 7 is formed by wet etching. In addition, the mesa structure portion 7 is formed so that the cross-sectional area of the mesa structure portion in the horizontal direction is continuously reduced from the supporting substrate 1 to the top surface 7b. Since the inclined side surface 7a is formed by wet etching, the inclination of the mesa structure portion 7 from the top surface to the supporting substrate 1 is gentle. It is preferable that the height h of the mesa structure portion 7 is in the range of $3\text{ }\mu\text{m}$ to $7\text{ }\mu\text{m}$ and the width w of the inclined side surface 7a in plane view is in the range of $0.5\text{ }\mu\text{m}$ to $7\text{ }\mu\text{m}$. In addition, it is more preferable that the height h is in the range of $5\text{ }\mu\text{m}$ to $7\text{ }\mu\text{m}$. The width w is more preferably in the range of $3\text{ }\mu\text{m}$ to $7\text{ }\mu\text{m}$ and most preferably, in the range of $4\text{ }\mu\text{m}$ to $6\text{ }\mu\text{m}$. The reason is as follows. Since the side surface of the mesa structure portion 7 is not vertical or steeply inclined, but is gently inclined, it is easy to form the protective film or the electrode metal film with a uniform thickness and there is no concern that a discontinuous film will be formed. Therefore, light leakage or poor electrical connection due to a discontinuous film is not caused and stable and high-brightness light emission is ensured.

When the wet etching is performed until the height is greater than 7 μm , the inclined side surface is likely to have an overhang shape (reverse tapered shape, inverse tapered shape), which is not preferable. This is because, when the inclined side surface has the overhang shape (reverse tapered shape), it is more difficult to form the protective
 5 film or the electrode film with a uniform thickness, without any discontinuous portion, than when the side surface is vertical.

In the specification, the height h means a distance (see FIG. 1) in the vertical direction from the surface of the electrode film 9 (a portion denoted by reference numeral 9c) which is formed on the flat portion 6, with the protective film interposed
 10 therebetween, to the surface of the electrode film 9 (a portion denoted by reference numeral 9ba) which covers a portion denoted by reference numeral 8ba in the protective film 8. The width w means a distance (see FIG. 1) in the horizontal direction from the edge of the electrode film 9 (a portion denoted by reference numeral 9ba) which covers a portion denoted by reference numeral 8ba in the protective film 8 to the lowest edge of
 15 the electrode film 9 (a portion denoted by reference numeral 9a) on the inclined side surface which is connected to the edge.

[0033]

FIG. 3 is an electron micrograph of the cross-section in the vicinity of the mesa structure portion 7.

20 The layer structure shown in FIG. 3 is the same as that in the following example except that a contact layer consists of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ and has a thickness of 3 μm .

[0034]

Since the mesa structure portion according to the invention is formed by wet etching, the rate of increase in the horizontal cross-sectional area (or the width or
 25 diameter) of the mesa structure portion increases from the top surface toward the

substrate (toward the lower side in FIG. 3). It is possible to determine that the mesa structure portion is not formed by dry etching, but is formed by wet etching on the basis of this shape.

In the example shown in FIG. 3, the height h was $7\text{ }\mu\text{m}$ and the width w was in
5 the range of $3.5\text{ }\mu\text{m}$ to $4.5\text{ }\mu\text{m}$.

[0035]

It is preferable that the mesa structure portion 7 have a rectangular shape in plane view. The reason is as follows. It is possible to suppress a change in the mesa shape depending on an etching depth due to the anisotropy of wet etching during
10 manufacturing and it is easy to control the area of each surface of the mesa structure portion. Therefore, required size and shape are obtained with high-accuracy.

[0036]

It is preferable that the mesa structure portion 7 is disposed in the light-emitting diode so as to lean to one side in the long axis direction of the light-emitting diode in
15 order to reduce the size of an element, as shown in FIGS. 1 and 2. The reason is as follows. Since the flat portion 6 needs to have a width required to attach bonding wires (not shown), there is a limit in reducing the width of the flat portion 6. When the mesa structure portion 7 leans to one side, it is possible to minimize the range of the flat portion 6 and reduce the size of an element.

20 [0037]

The flat portion 6 is arranged around the mesa structure portion 7. In the invention, since wire bonding is performed on the flat portion of the electrode film to which sufficient load and/or ultrasonic waves are applied, it is possible to achieve wire bonding with high bonding strength.

25 [0038]

The protective film 8 and the electrode film (front surface electrode film, upper electrode) 9 are sequentially formed on the flat portion 6 and a bonding wire (not shown) is attached onto the electrode film 9. The material forming a portion of the flat portion 6 which is arranged immediately below the protective film 8 is determined by the internal
5 structure of the mesa structure portion 7.

[0039]

The protective film 8 includes a portion 8a which covers the inclined side surface 7a of the mesa structure portion 7, a portion 8c (including a portion 8cc which is opposite to the portion 8c, with the mesa structure portion 7 interposed therebetween, and
10 covers an opposite flat portion) which covers at least a portion of the flat portion 6, a portion 8ba which covers the peripheral region 7ba of the top surface 7b of the mesa structure portion 7, and a portion 8d which covers a central portion of the top surface 7b. The protective film 8 includes the electrical conduction window 8b which is provided inside the peripheral region 7ba in plane view and from which a portion of the surface of
15 the contact layer 5 is exposed.

In this embodiment, a region (ring-shaped region) between two concentric circuits with different diameters which are provided between the portion 8ba that is disposed below the peripheral region 7ba and a portion that is disposed below the portion 8d covering the central portion on the surface of the contact layer 5 in the top surface 7b
20 of the mesa structure portion 7 is exposed from the electrical conduction window 8b.

The shape of the electrical conduction window 8b is not limited. The electrical conduction window 8b may not have the ring shape. In addition, the electrical conduction window 8b may not be a continuous region, but may include a plurality of discrete regions.

25 [0040]

The protective film 8 is arranged below the front surface electrode film 9 and has a first function of limiting a portion of the front surface electrode film 9 through which a current flows into or out from the compound semiconductor layer 20 to the electrical conduction window 8b of the top surface to a portion of the front surface electrode film 9 which comes into contact with the compound semiconductor layer 20, in order to narrow a light emission region and a light extraction range. That is, after the protective film 8 is formed, the front surface electrode film is formed on the entire surface including the protective film 8. Then, the front surface electrode film is patterned. Even though the front surface electrode film is not removed from the portion in which the protective film 8 is formed, no current flows. The electrical conduction window 8b of the protective film 8 is formed at the desired position where the current flows.

Therefore, as long as the electrical conduction window 8b is formed in a portion of the top surface 7b of the mesa structure portion 7 in order to make the protective film 8 have the first function, the shape or position of the electrical conduction window 8b is not limited to that shown in FIG. 1.

[0041]

While the first function is indispensable, the second function of the protective film 8 is not indispensable. The protective film 8 shown in FIG. 1 is arranged on the surface of the contact layer 5 in the light emission hole 9a of the front surface electrode film 9 in plane view and takes on the second function of extracting light through the protective film 8 and protecting the surface of the contact layer 5 which extracts light.

In a second embodiment which will be described below, the protective film is not provided below the light emission hole and light is directly extracted from the light emission hole 9b, without passing through the protective film. The protective film does

not have the second function.

[0042]

A known material forming an insulating layer can be used as the material forming the protective film 8. A silicon oxide film is preferable since it is easy to form
5 a stable insulating film.

In this embodiment, since light is extracted through the protective film 8 (8d), the protective film 8 needs to be transparent.

[0043]

The thickness of the protective film 8 is preferably in the range of 0.3 μm to 1
10 μm and more preferably, in the range of 0.5 μm to 0.8 μm . The reason is that sufficient insulation is not obtained when the thickness is less than 0.3 μm and it takes a lot of time to form the protective film 8 when the thickness is greater than 1 μm .

Here, the thickness of the protective film means the thickness of the protective film in a flat portion, such as the upper surface of the supporting structure portion or the
15 top surface of the mesa structure portion.

[0044]

The electrode film (front surface electrode film) 9 consists of a portion 9a which covers the portion 8a of the protective film 8 covering the inclined side surface 7a, a portion 9c which covers the portion 8c of the protective film 8 covering at least a portion
20 of the flat portion 6, a portion 9ba which covers the portion 8ba of the protective film 8 covering the peripheral region 7ba of the top surface 7b of the mesa structure portion 7, a portion 9bb (hereinafter, appropriately referred to as a “contact portion”) which fills the electrical conduction window 8b of the protective film 8, and a portion 9d which covers the outer circumferential edge of the portion 8d of the protective film 8 covering the

central portion of the top surface 7b of the mesa structure portion 7.

[0045]

The first function of the electrode film (front surface electrode film) 9 is the function of an electrode for current flow and the second function thereof is limiting the emission range of generated light. In the example shown in FIG. 1, the contact portion 9bb takes on the first function and the portion 9d which covers the outer circumferential edge of the portion 8d covering the central portion takes on the second function.

A non-translucent protective film may be used and take on the second function.

[0046]

The electrode film 9 may cover a portion of or the entire protective film 8 on the flat portion 6. It is preferable that the electrode film 9 covers as wide a range as possible in order to appropriately attach the bonding wire. It is preferable that the street diode in order to reduce costs, as shown in FIG. 2.

[0047]

In the electrode film 9, only the contact portion 9bb comes into contact with the contact layer 5 in the top surface 7b of the mesa structure portion 7. Therefore, the current which flows in the light-emitting diode flows only through the contact portion 9bb.

[0048]

A known electrode material which has a good ohmic contact with the contact layer can be used as the material forming the electrode film 9. For example, an n-type electrode can have a layer structure (AuGe/Ni/Au) including an AuGe layer, a Ni layer, and an Au layer which are sequentially formed.

The thickness of the electrode film 9 is preferably in the range of 0.5 μm to 2.0

μm and more preferably in the range of $1.2\ \mu\text{m}$ to $1.8\ \mu\text{m}$. The reason is that it is difficult to obtain a uniform and good ohmic contact, which results in insufficient bonding strength and thickness when the thickness is less than $0.5\ \mu\text{m}$, and production costs increase when the thickness is greater than $2.0\ \mu\text{m}$.

5 The thickness of the electrode film means the thickness of the electrode film in a flat portion, such as the upper surface of the supporting structure portion or the top surface of the mesa structure portion.

[0049]

10 The transparent film 30 is formed between the reflecting layer 2 and the compound semiconductor layer 20.

The material forming the transparent film 30 is not particularly limited as long as it is transparent (translucent) and has a higher conductivity than the through-electrode 31. For example, SiO_2 , SiN , SiON , Al_2O_3 , MgF_2 , TiO_2 , TiN , or ZnO can be used.

15 The thickness of the transparent film 30 is determined by the thickness of the through-electrode. The thickness of the through-electrode 31 is preferably in the range of $0.05\ \mu\text{m}$ to $2\ \mu\text{m}$. Therefore, the thickness of the transparent film 30 is preferably in the range of $0.05\ \mu\text{m}$ to $2\ \mu\text{m}$, which will be described below.

[0050]

20 The through-electrode 31 is provided in the transparent film 30 in the range (R2 (see FIG. 4)) which overlaps the light emission hole 9b in plane view so as to come into contact with the compound semiconductor layer 20 and the reflecting layer 2. When the through-electrode 31 is arranged in this range, a current is concentrated between the through-electrode 31 and the portion (contact portion 9bb) of the electrode film 9 which fills the electrical conduction window. Then, the amount of light emitted from a portion,

which is arranged immediately below the range overlapping the light emission hole 9b, of the active layer is more than the amount of light emitted from a portion, other than the portion which is arranged immediately below the range, of the active layer. As a result, the percentage of light which travels toward the light emission hole increases and light
5 extraction efficiency is improved.

[0051]

It is preferable that the through-electrode 31 be formed in the range (R4 (see FIG. 4)) of a reduced and projected figure of the light emission hole 9b which is reduced and projected onto the transparent film 30 by extending a segment that connects each point
10 on the outer circumference of the electrical conduction window 8b and each point on the outer circumference of a figure obtained by projecting the light emission hole 9b onto the active layer 4 at the shortest distance. When the through-electrode 31 is arranged in this range, the amount of light emitted from a portion of the active layer which is arranged immediately below a range (R5 (see FIG. 4)) narrower than the range 9b that overlaps the
15 light emission hole is more than the amount of light emitted from a portion other than the portion which is arranged immediately below the range. As a result, the percentage of light which travels toward the light emission hole further increases and the light extraction efficiency is further improved.

[0052]

20 The shape of the through-electrode 31 is not particularly limited and the through-electrode 31 may have a plurality of electrodes which are discretely arranged.

[0053]

The metal material forming the through-electrode 31 is not particularly limited as long as it can make an ohmic contact with the bonding (contact) layer 5. For
25 example, AuBe or AuZn can be used.

It is preferable that the thickness of the through-electrode 31 be in the range of 0.05 μm to 2 μm . The reason is that it is difficult to make the through-electrode when the thickness is less than 0.05 μm and production costs increase when the thickness is greater than 2 μm .

5 [0054]

FIG. 4 is an enlarged perspective view illustrating the vicinity of the through-electrode 31 and the electrical conduction window 8b of the light-emitting diode shown in FIG. 1. The planar arrangement of the through-electrode 31 in the cross-sectional view of FIG. 4 will be described with reference to FIG. 4.

10 [0055]

In FIG. 4, R1 indicates the inside of the outer circumference of the electrical conduction window 8b (the electrical conduction window 8b and the range S surrounded by the electrical conduction window 8b (see FIG. 1)). R2 indicates the range (width) of the light emission hole 9b. R3 indicates the inside of the outer circumference of the figure obtained by projecting the light emission hole 9b onto the active layer 4. R3 and R2 have the same size. R4 indicates the range of the reduced and projected figure of the light emission hole 9b which is reduced and projected onto the transparent film 30 by extending the segment (for example, a segment connecting the points P and Q) that connects each point on the outer circumference of the electrical conduction window 8b (a point P is a point on the outer circumference) and each point on the outer circumference of the figure (a point Q is a point on the outer circumference. The point Q varies depending on the thickness of the active layer 9 and the effect of the invention is obtained regardless of the position of the point Q) obtained by projecting the light emission hole 9b onto the active layer 4 at the shortest distance. R5 indicates the range in which the through-electrode 31 is actually formed.

15

20

25

[0056]

In FIG. 4, the through-electrode 31 is formed so as to fill the range R5 in the range R4 in plane view.

When the through-electrode 31 is formed in this range, the current is concentrated on a range which connects the contact portion 9bb (the portion fills the electrical conduction window 8b) of the electrode film 9 and the through-electrode 31. Then, the amount of light emitted from a portion of the active layer 4 which is arranged between the segments T-T and Q-Q is more than the amount of light emitted from the other portions. Therefore, the amount of light emitted from a portion which is arranged immediately below the light emission hole 9b is significantly more than the amount of light emitted from the other portions. As a result, the percentage of light emitted from the light emission hole 9b increases and the light extraction efficiency is improved.

[0057]

As shown in FIG. 1, the light leakage prevention film 16, which prevents light emitted from the active layer from leaking from the side surface of the mesa structure portion 7 to the outside of the element, may be provided.

[0058]

A known reflective material can be used as the material forming the light leakage prevention film 16. For example, when AuGe/Ni/Au is used as the material forming the electrode film 9, AuGe/Ni/Au can be used as the material forming the light leakage prevention film 16.

[0059]

In this embodiment, the protective film 8d (8) is formed below the light emission hole 9b and light is extracted from the light emission hole 9b through the protective film 8d (8) in the top surface of the mesa structure portion 7.

[0060]

It is preferable that the light emission hole 9b has a circular or elliptical shape in plane view. The reason is as follows. It is easy to form a uniform contact region, as compared to a structure in which the light emission hole 9b has an angular shape, such as a rectangular shape, and it is possible to prevent, for example, the concentration of a current on the corner. In addition, this structure is suitable for a coupling to a fiber in the light-receiving side.

[0061]

It is preferable that the diameter of the light emission hole 9b is in the range of 50 μm to 150 μm . The reason is as follows. When the diameter is less than 50 μm , current density increases in the light emission portion and an output is saturated with a small amount of current. When the diameter is greater than 150 μm , it is difficult to diffuse the current to the entire light emission portion. As a result, light emission efficiency with respect to an input current is reduced.

[0062]

For example, metal, Ge, Si, GaP, GaInP, or SiC can be used as the material forming the supporting substrate 1. A Ge substrate and a Si substrate have the advantages that they are inexpensive and have high humidity resistance. GaP, GaInP, and SiC substrate have the advantages that they have a thermal expansion coefficient close to that of the light emission portion and have high humidity resistance and high thermal conductivity. A metal substrate is inexpensive and has high mechanical strength and high radiation performance. A laminated structure of a plurality of metal layers (metal plates) has the advantage that it can adjust the thermal expansion coefficient of the entire metal substrate, which will be described below.

[0063]

When the metal substrate is used as the supporting substrate 1, a plurality of metal layers (metal plates) can be laminated.

When the plurality of metal layers (metal plates) are laminated, it is preferable that two types of metal layers are alternately laminated. In particular, in two types of
5 metal layers (for example, they are referred to as a first metal layer and a second metal layer), it is preferable that the number of metal layers of each type is an odd number.

[0064]

For example, in the metal substrate in which the second metal layer is interposed between the first metal layers, when the second metal layer consists of a material which
10 has a smaller thermal expansion coefficient than the compound semiconductor layer, it is preferable that the first metal layer consists of a material which has a larger thermal expansion coefficient than the compound semiconductor layer, in order to prevent the warping or breaking of the metal substrate. The reason is as follows. Since the thermal expansion coefficient of the entire metal substrate is close to the thermal
15 expansion coefficient of the compound semiconductor layer, it is possible to prevent the warping or breaking of the metal substrate when the compound semiconductor layer and the metal substrate are bonded to each other and to improve the production yield of the light-emitting diode. Similarly, when the second metal layer consists of a material which has a larger thermal expansion coefficient than the compound semiconductor layer,
20 it is preferable that the first metal layer consists of a material which has a smaller thermal expansion coefficient than the compound semiconductor layer. The reason is as follows. Since the thermal expansion coefficient of the entire metal substrate is close to the thermal expansion coefficient of the compound semiconductor layer, it is possible to prevent the warping or breaking of the metal substrate when the compound
25 semiconductor layer and the metal substrate are bonded to each other and to improve the

production yield of the light-emitting diode.

From the above-mentioned viewpoint, one of the two types of metal layers may be the first metal layer or the second metal layer.

As the two types of metal layers, for example, a combination of a metal layer
 5 which is made of any one of silver (thermal expansion coefficient = 18.9 ppm/K), copper
 (thermal expansion coefficient = 16.5 ppm/K), gold (thermal expansion coefficient =
 14.2 ppm/K), aluminum (thermal expansion coefficient = 23.1 ppm/K), nickel (thermal
 expansion coefficient = 13.4 ppm/K), and alloys thereof and a metal layer which is made
 of any one of molybdenum (thermal expansion coefficient = 5.1 ppm/K), tungsten
 10 (thermal expansion coefficient = 4.3 ppm/K), chromium (thermal expansion coefficient =
 4.9 ppm/K), and alloys thereof can be used.

As a preferred example, there is a metal substrate consisting of three layers of
 Cu/Mo/Cu. From the above-mentioned viewpoint, the same effect as described above is
 obtained from the metal substrate consisting of three layers of Mo/Cu/Mo. Since the
 15 metal substrate consisting of three layers of Cu/Mo/Cu has a structure in which the Mo
 layer with high mechanical strength is interposed between the Cu layers which are easy
 to process, the metal substrate is easier to cut than a metal substrate consisting of three
 layers of Mo/Cu/Mo.

[0065]

20 For the thermal expansion coefficient of the metal substrate, for example, the
 thermal expansion coefficient of the metal substrate consisting of three layers of Cu (30
 μm)/Mo (25 μm)/Cu (30 μm) is 6.1 ppm/K and the thermal expansion coefficient of the
 metal substrate including three layers of Mo (25 μm)/Cu (70 μm)/Mo (25 μm) is 5.7
 ppm/K.

25 [0066]

From the viewpoint of heat dissipation, it is preferable that the metal layer forming the metal substrate consists of a material with high thermal conductivity. In this case, it is possible to improve the radiation performance of the metal substrate and to make the light-emitting diode emit light with high brightness. In addition, it is possible to increase the lifespan of the light-emitting diode.

For example, it is preferable to use silver (thermal conductivity = $420\text{W/m}\cdot\text{K}$), copper (thermal conductivity = $398\text{W/m}\cdot\text{K}$), gold (thermal conductivity = $320\text{W/m}\cdot\text{K}$), aluminum (thermal conductivity = $236\text{W/m}\cdot\text{K}$), molybdenum (thermal conductivity = $138\text{W/m}\cdot\text{K}$), tungsten (thermal conductivity = $174\text{W/m}\cdot\text{K}$), and alloys thereof.

It is more preferable that the metal layers consist of a material with a thermal expansion coefficient that is substantially equal to the thermal expansion coefficient of the compound semiconductor layer. In particular, it is preferable that the material of the metal layer has a thermal expansion coefficient that is $\pm 1.5\text{ ppm/K}$ for the thermal expansion coefficient of the compound semiconductor layer. In this case, it is possible to reduce thermal stress on the light-emitting portion when the metal substrate and the compound semiconductor layer are bonded to each other. As a result, it is possible to suppress the breaking of the metal substrate due to heat caused when the metal substrate is connected to the compound semiconductor layer and to improve the production yield of the light-emitting diode.

For the thermal conductivity of the entire metal substrate, for example, the thermal conductivity of the metal substrate consisting of three layers of Cu ($30\text{ }\mu\text{m}$)/Mo ($25\text{ }\mu\text{m}$)/Cu ($30\text{ }\mu\text{m}$) is $250\text{W/m}\cdot\text{K}$ and the thermal conductivity of the metal substrate including three layers of Mo ($25\text{ }\mu\text{m}$)/Cu ($70\text{ }\mu\text{m}$)/Mo ($25\text{ }\mu\text{m}$) is $220\text{W/m}\cdot\text{K}$.

When the compound semiconductor layer is grown on a growth substrate, the metal substrate is bonded, and the growth substrate is removed by an etchant, it is preferable that the upper and lower surfaces of the metal substrate are covered with a metal protective film in order to prevent deterioration of it due to the etchant. In addition, it is preferable that the side surface of the metal substrate be covered with the metal protective film.

It is preferable that the metal protective film is made of a material including at least one of chromium and nickel with high adhesion, platinum which is chemically stable, and gold.

It is most preferable that the metal protective film is a layer made of a combination of nickel with high adhesion and gold with high chemical resistance.

The thickness of the metal protective film is not particularly limited and is in the range of 0.2 μm to 5 μm in terms of the balance between etchant resistance and costs. Preferably, the optimum range of the thickness is from 0.5 μm to 3 μm . When expensive gold is used, it is preferable that the thickness is equal to or less than 2 μm .

[0068]

Known functional layers can be timely added to the structure of the reflecting layer 2 and the compound semiconductor layer 20 (the bonding layer 3, the active layer 4, and the contact layer 5). For example, a structure of a known layer, such as a current diffusion layer for diffusing an element driving current to the entire plane of the light-emitting portion, a current blocking layer for limiting a region through which the element driving current flows, or a current blocking layer, can be used.

[0069]

As shown in FIG. 5, the active layer 4 includes a lower cladding layer 11, a lower guide layer 12, a light-emitting layer 13, an upper guide layer 14, and an upper

cladding layer 15 which are sequentially laminated. That is, in order to emit light with high intensity, it is preferable that the active layer 4 has a so-called double hetero (abbreviated to DH) structure in which the lower cladding layer 11 and the lower guide layer 12, and the upper guide layer 14 and the upper cladding layer 15 are arranged on the upper and lower sides of the light-emitting layer 13 to “confine” carriers causing radiation recombination and light emission to the light-emitting layer 13, respectively.

[0070]

As shown in FIG. 5, the light-emitting layer 13 can have a quantum well structure in order to control the emission wavelength of the light emitted with the light-emitting diode (LED). That is, the light-emitting layer 13 can have a multi-layer structure (laminated structure) of well layers 17 and barrier layers 18 which has the barrier layers 18 at both ends thereof.

[0071]

It is preferable that the thickness of the light-emitting layer 13 be in the range of 0.02 μm to 2 μm . The conductivity type of the light-emitting layer 13 is not particularly limited and can be selected from any one of undoped type, p type, and n type. It is preferable that the light-emitting layer 13 be an undoped type with good crystallinity or have a carrier concentration of less than $3 \times 10^{17} \text{ cm}^{-3}$ in order to improve light emission efficiency.

20 [0072]

A known well layer material can be used as the material forming the well layer 17. For example, AlGaAs, InGaAs, or AlGaInP can be used.

[0073]

The thickness of the well layer 17 is preferably in the range of 3 nm to 30 nm and more preferably in the range of 3 nm to 10 nm.

[0074]

It is preferable that a material which is suitable for the material forming the well layer 17 be selected as the material forming the barrier layer 18. A material with a composition which has a larger band gap than the material forming the well layer 17 is preferably used in order to prevent the absorption of light by the barrier layer 18 and to improve light emission efficiency.

[0075]

For example, when AlGaAs or InGaAs is used as the material forming the well layer 17, it is preferable that AlGaAs or AlGaInP is used as the material forming the barrier layer 18. When AlGaInP is as the material forming the barrier layer 18, the barrier layer 18 has high crystallinity and contributes to a high output since it does not include As, which is likely to cause a defect.

When $(\text{Al}_{X1}\text{Ga}_{1-X1})_{Y1}\text{In}_{1-Y1}\text{P}$ ($0 \leq X1 \leq 1$, $0 < Y1 \leq 1$) is used as the material forming the well layer 17, $(\text{Al}_{X4}\text{Ga}_{1-X4})_{Y1}\text{In}_{1-Y1}\text{P}$ ($0 \leq X4 \leq 1$, $0 < Y1 \leq 1$, $X1 < X4$) with a high Al composition or AlGaAs with a higher band gap energy than the well layer $(\text{Al}_{X1}\text{Ga}_{1-X1})_{Y1}\text{In}_{1-Y1}\text{P}$ ($0 \leq X1 \leq 1$, $0 < Y1 \leq 1$) can be used as the material forming the barrier layer 18.

[0076]

It is preferable that the thickness of the barrier layer 18 is equal to or greater than the thickness of the well layer 17. When the thickness of the barrier layer 18 is sufficiently large in a thickness range in which a tunnel effect is caused, the spreading of carriers between the well layers due to the tunnel effect is suppressed and the effect of confining the carriers is improved. Therefore, the radiative recombination probability of electrons and holes increases and it is possible to improve a light emission output.

25 [0077]

In the multi-layer structure of the well layers 17 and the barrier layers 18, the number of pairs of the well layers 17 and the barrier layers 18 which are alternately laminated is not particularly and it is preferable that the number of pairs are equal to or greater than 2 and equal to or less than 40. That is, it is preferable that the light-emitting layer 13 includes 2 to 40 well layers 17. It is preferable that five or more well layers 17 are provided in terms of the optimal light emission efficiency range of the light-emitting layer 13. When a large number of pairs of the well layers 17 and the barrier layers 18 are provided, the forward voltage (V_F) increases since the well layer 17 and the barrier layer 18 have low carrier concentration. Therefore, the number of pairs of the well layers 17 and the barrier layers 18 is preferably equal to or less than 40 and more preferably equal to less than 20.

[0078]

As shown in FIG. 5, the lower guide layer 12 and the upper guide layer 14 are provided on the lower and upper surfaces of the light-emitting layer 13, respectively. Specifically, the lower guide layer 12 is provided on the lower surface of the light-emitting layer 13 and the upper guide layer 14 is provided on the upper surface of the light-emitting layer 13.

[0079]

A known compound semiconductor material can be used as the material forming the lower guide layer 12 and the upper guide layer 14. It is preferable to select a material which is suitable for the material forming the light-emitting layer 13. For example, AlGaAs or AlGaInP can be used.

[0080]

For example, when AlGaAs or InGaAs is used as the material forming the well layer 17 and AlGaAs or AlGaInP is used as the material forming the barrier layer 18,

AlGaAs or AlGaInP is preferable as the material forming the lower guide layer 12 and the upper guide layer 14. When AlGaInP is used as the material forming the lower guide layer 12 and the upper guide layer 14, the lower guide layer 12 and the upper guide layer 14 have high crystallinity and contribute to a high output since they do not include As, which is likely to cause a defect.

When $(\text{Al}_{X1}\text{Ga}_{1-X1})_{Y1}\text{In}_{1-Y1}\text{P}$ ($0 \leq X1 \leq 1$, $0 < Y1 \leq 1$) is used as the material forming the well layer 17, $(\text{Al}_{X4}\text{Ga}_{1-X4})_{Y1}\text{In}_{1-Y1}\text{P}$ ($0 \leq X4 \leq 1$, $0 < Y1 \leq 1$, $X1 < X4$) with a high Al composition or AlGaAs with a higher band gap energy than the well layer $(\text{Al}_{X1}\text{Ga}_{1-X1})_{Y1}\text{In}_{1-Y1}\text{P}$ ($0 \leq X1 \leq 1$, $0 < Y1 \leq 1$) can be used as the material forming the guide layer 14.

[0081]

The lower guide layer 12 and the upper guide layer 14 are provided in order to reduce the propagation of defects between the lower and upper cladding layers 11 and 15 and the light-emitting layer 13. Therefore, the thickness of the lower guide layer 12 and the upper guide layer 14 is preferably equal to or greater than 10 nm and more preferably in the range of 20 nm to 100 nm.

[0082]

The conductivity type of the lower guide layer 12 and the upper guide layer 14 is not particularly limited and can be selected from any one of undoped type, p type, and n type. It is preferable that the guide layers are undoped type with good crystallinity or have a carrier concentration of less than $3 \times 10^{17} \text{ cm}^{-3}$ in order to improve light emission efficiency.

[0083]

As shown in FIG. 5, the lower cladding layer 11 and the upper cladding layer 15

are provided on the lower surface of the lower guide layer 12 and the upper surface of the upper guide layer 14, respectively.

[0084]

A known compound semiconductor material can be used as the material forming the lower cladding layer 11 and the upper cladding layer 15. It is preferable to select a material which is suitable for the material forming the light-emitting layer 13. For example, AlGaAs or AlGaInP can be used.

[0085]

For example, when AlGaAs or InGaAs is used as the material forming the well layer 17 and AlGaAs or AlGaInP is used as the material forming the barrier layer 18, AlGaAs or AlGaInP is preferable as the material forming the lower cladding layer 11 and the upper cladding layer 15. When AlGaInP is used as the material forming the lower cladding layer 11 and the upper cladding layer 15, the lower cladding layer 11 and the upper cladding layer 15 have high crystallinity and contribute to a high output since they do not include As, which is likely to cause a defect.

When $(\text{Al}_{X1}\text{Ga}_{1-X1})_{Y1}\text{In}_{1-Y1}\text{P}$ ($0 \leq X1 \leq 1$, $0 < Y1 \leq 1$) is used as the material forming the well layer 17, $(\text{Al}_{X4}\text{Ga}_{1-X4})_{Y1}\text{In}_{1-Y1}\text{P}$ ($0 \leq X4 \leq 1$, $0 < Y1 \leq 1$, $X1 < X4$) with a high Al composition or AlGaAs with a higher band gap energy than the well layer $(\text{Al}_{X1}\text{Ga}_{1-X1})_{Y1}\text{In}_{1-Y1}\text{P}$ ($0 \leq X1 \leq 1$, $0 < Y1 \leq 1$) can be used as the material forming the cladding layer 15.

[0086]

The lower cladding layer 11 and the upper cladding layer 15 are configured so as to have different polarities. The carrier concentration and thickness of the lower cladding layer 11 and the upper cladding layer 15 can be set in a known referred range. It is preferable to optimize conditions so that the light emission efficiency of the

light-emitting layer 13 is improved. The lower and upper cladding layers may not be provided.

In addition, it is possible to control the composition of the lower cladding layer 11 and the upper cladding layer 15 to reduce the warping of the compound semiconductor layer 20.

[0087]

The contact layer 5 is provided in order to reduce contact resistance with the electrode. It is preferable that the contact layer 5 consisted of a material with a higher band gap energy than that forming the light-emitting layer 13. The lower limit of the carrier concentration of the contact layer 5 is preferably equal to or greater than $5 \times 10^{17} \text{ cm}^{-3}$ and more preferably equal to or greater than $1 \times 10^{18} \text{ cm}^{-3}$, in order to reduce the contact resistance with the electrode. It is preferable that the upper limit of the carrier concentration is equal to or less than $2 \times 10^{19} \text{ cm}^{-3}$ at which crystallinity is likely to be reduced. It is preferable that the thickness of the contact layer 5 is equal to or greater than $0.05 \text{ }\mu\text{m}$. The upper limit of the thickness of the contact layer 5 is not particularly limited and is preferably equal to or less than $10 \text{ }\mu\text{m}$ in order to set costs for epitaxial growth in a proper range.

[0088]

The light-emitting diode according to the invention can be incorporated into electronic apparatuses, such as lamps, backlights, mobile phones, displays, various types of panels, computers, game machines, and illuminators, or mechanical devices, such as vehicles into which the electronic apparatuses are incorporated.

[0089]

[Light-emitting Diode (Second Embodiment)]

FIG. 6 is an enlarged cross-sectional view illustrating the vicinity of a through-electrode 32 and an electrical conduction window 8b in a modification example of the light-emitting diode to which the invention is applied.

In the first embodiment, the through-electrode 31 is formed in the range (R2 or R3) (particularly, R4) which overlaps the light emission hole 9b in plane view. A second embodiment differs from the first embodiment in that the through-electrode 32 is formed at the position which overlaps the electrical conduction window 8b in plane view.

[0090]

The shape of the through-electrode 32 is not particularly limited and the through-electrode 32 may include a plurality of electrodes which are discretely arranged.

[0091]

The planar arrangement of the through-electrode 32 in the cross-section view of FIG. 6 will be described with reference to FIG. 6.

In FIG. 6, R1 indicates the inside of the outer circumference of the electrical conduction window 8b (the electrical conduction window 8b and a range S surrounded by the electrical conduction window 8b (see FIG. 1)) and R2 indicates the range (width) of a light emission hole 9b, similarly to FIG. 4. R6 indicates the width of the electrical conduction window 8b and also indicates a position (range) which overlaps the electrical conduction window 8b. Dotted lines are drawn down from the outer circumference and inner circumference of the electrical conduction window 8b in order to indicate the range. R7 indicates the range in which the through-electrode 32 is actually formed.

[0092]

As shown in FIG. 6, the through-electrode 32 is formed in a transparent film 2 at a position R6 that overlaps the electrical conduction window 8b in plane view.

When the through-electrode 32 is arranged in this range, a current is

concentrated between the through-electrode 32 and a portion (contact portion 9bb) of the electrode film 9 which fills the electrical conduction window. The portion on which the current is concentrated is close to a portion which is arranged immediately below the light emission hole 9b. Since a large amount of light is emitted from the portion on which the current is concentrated, the percentage of light which travels toward the light emission hole increases and light extraction efficiency is improved.

[0093]

[Light-emitting Diode (Third Embodiment)]

FIG. 7 is a schematic cross-sectional view illustrating a modification example of the light-emitting diode according to the first embodiment of the invention.

In the first embodiment, the protective film is formed below the light emission hole and light is extracted from the light emission hole through the protective film in the top surface of the mesa structure portion. A third embodiment has a structure in which the protective film is not provided below the light emission hole and light is directly extracted from a light emission hole 9b, without passing through the protective film.

That is, in a light-emitting diode 200 according to the third embodiment, a protective film 28 covers at least a portion 28c of a flat portion 6, an inclined side surface 7a of a mesa structure portion 7, and a peripheral region 7ba of a top surface 7b of the mesa structure portion 7. In addition, the protective film 28 includes an electrical conduction window 28b which is provided inside the peripheral region 7ba in plane view and from which the surface of a contact layer 5 is exposed. An electrode film 29 covers at least a portion of the flat portion 6 through the protective film 28, covers the inclined side surface 7a of the mesa structure portion 7 through the protective film 28, and covers the peripheral region 7ba of the top surface 7b of the mesa structure portion 7 through the protective film 28. In addition, the electrode film 29 includes a light emission hole 29b

which is formed by covering only a portion of the surface of the contact layer 5 exposed from the electrical conduction window 28b in the top surface of the mesa structure portion 7 and from which another portion 5a of the surface of the contact layer 5 is exposed.

5 [0094]

As shown in FIG. 7, the protective film 28 according to the second embodiment includes a portion 28a which covers the inclined side surface 7a of the mesa structure portion 7, a portion 28c (including a portion 28cc which is opposite to the portion 28c, with the mesa structure portion 7 interposed therebetween, and covers an opposite flat
10 portion) which covers at least a portion of the flat portion 6, and a portion 28ba which covers the peripheral region 7ba of the top surface 7b of the mesa structure portion 7. In addition, the protective film 28 includes the electrical conduction window 28b which is provided inside the peripheral region 7ba in plane view and from which the surface of the contact layer 5 is exposed. That is, a portion other than the portion of the surface of
15 the contact layer 5 which is disposed below the peripheral region 7ba in the top surface 7b of the mesa structure portion 7 is exposed from the electrical conduction window 28b. An electrode film (front surface electrode film) 9 is on the protective film 8. The protective film 8 is formed in a portion in which no current flows.

[0095]

20 As shown in FIG. 7, the electrode film (front surface electrode film) 29 according to the second embodiment consists of a portion 29a which covers the portion 28a of the protective film 28 covering the inclined side surface 7a, a portion 29c which covers the portion 28c of the protective film 28 covering at least a portion of the flat portion 6, a portion 29ba which covers the portion 28ba of the protective film 28
25 covering the peripheral region 7ba of the top surface 7b of the mesa structure portion 7,

and a portion 29bb which covers the contact layer 5 over a portion 28ba of the protective film 28 in the top surface 7b of the mesa structure portion 7 such that the light emission hole 29b is formed.

In the electrode film (front surface electrode film) 29 according to the second embodiment, the portion 29bb takes on both the first function and the second function.

[0096]

[Method of Manufacturing Light-emitting Diode]

Next, a method of Manufacturing the light-emitting diode according to the invention will be described.

10 <Process of Manufacturing Supporting Substrate>

[1] When Ge Substrate Is Used as Supporting Substrate 1 (See Reference Numerals Shown in FIG. 10A)

A layer structure (a layer including Ti/Au/In) 42 including, for example, a Ti layer, an Au layer, and an In layer which are sequentially laminated is formed on a front surface 41A of a germanium substrate 41, a layer structure (a layer including Ti/Au) 43 including, for example, a Ti layer and an Au layer which are sequentially laminated is formed on a rear surface of the germanium substrate 41. In this way, the supporting substrate 1 is produced.

[0097]

20 [2] When Metal Substrate Is Used as Supporting Substrate 1 (Modification Example)

FIGS. 8(a) to 8(c) are schematic cross-sectional views illustrating a portion of the metal substrate for describing a process of manufacturing the metal substrate.

The metal substrate 1 includes a first metal layer (first metal plate) 51b which has a larger thermal expansion coefficient than the material forming the active layer and a second metal layer (second metal plate) 51a which has a smaller thermal expansion

coefficient than the material forming the active layer and the metal substrate 1 is formed by a hot press.

[0098]

Specifically, first, two first metal layers 51b which are substantially flat plates
 5 and one second metal layer 51a which is a substantially flat plate are prepared. For example, a Cu layer with a thickness of 10 μm is used as the first metal layer 51b and a Mo layer with a thickness of 75 μm is used as the second metal layer 51a.

Then, as shown in FIG. 8(a), the second metal layer 51a is inserted between the two first metal layers 51b so as to overlap each other.

10 [0099]

Then, these metal layers which overlap each other are arranged in a predetermined pressing apparatus and a load is applied to the first metal layer 51b and the second metal layer 51a in the direction of arrows at a high temperature. Then, as shown in FIG. 8(b), the metal substrate 1 including three layers, that is, the Cu layer (10 μm),
 15 which is the first metal layer 51b, the Mo layer (75 μm), which is the second metal layer 51a, and the metal substrate 1, which consists of the three layers Cu (10 μm) / Mo(75 μm) / Cu (10 μm), is formed.

For example, the metal substrate 1 has a thermal expansion coefficient of 5.7 ppm/K and a thermal conductivity of 220 W/m·K.

20 [0100]

Then, as shown in FIG. 8(c), a metal protective film 51c which covers the entire surface, that is, the upper, lower, and side surfaces of the metal substrate 1 is formed. In this case, since the metal substrate has not been diced into each light-emitting diode, the side surface of the metal substrate which is covered with the metal protective film is the

outer circumferential side surface of the metal substrate (plate). Therefore, when the metal protective film 51c covers the side surface of the metal substrate 1 of each light-emitting diode after dicing, a process of covering the side surface with the metal protective film is separately performed.

5 FIG. 8(c) shows a portion of the metal substrate (plate), not the outer circumferential end. Therefore, the metal protective film on the outer circumferential side surface is not shown in FIG. 8(c).

It is not necessary that the metal substrate includes the metal protective film.

[0101]

10 The metal protective film can be formed by a known film formation method. A plating method which can form a film on the entire surface including the side surface is most preferable.

For example, an electroless plating method sequentially plates the metal substrate with nickel and gold to produce the metal substrate 1 with the upper, side, and
15 lower surfaces which are sequentially covered with the nickel film and the gold film (metal protective film).

A plating material is not particularly limited and a known material, such as copper, silver, nickel, chromium, platinum, or gold can be used. A layer made of a combination of nickel with high adhesion and gold with high chemical resistance is
20 optimal.

The plating method can be performed with a known technique and a known chemical. The electroless plating method, which does not require an electrode, is simple and preferable.

[0102]

25 <Process of Forming Compound Semiconductor Layer>

First, as shown in FIG. 9, a plurality of epitaxial layers are grown on one surface 61a of a semiconductor substrate (growth substrate) 61 to form an epitaxial laminate 80 including the active layer 4.

The semiconductor substrate 61 is used to form the epitaxial laminate 80 and is, for example, a Si-doped n-type GaAs single crystal substrate in which one surface 61a is inclined at 15° with respect to the (100) plane. When an AlGaInP layer or an AlGaAs layer is used as the epitaxial laminate 80, a gallium arsenide (GaAs) single crystal substrate can be used as the substrate for forming the epitaxial laminate 80.

[0103]

As a method for forming the active layer 4, for example, the following method can be used: a metal organic chemical vapor deposition (MOCVD) method; a molecular beam epitaxy (MBE) method; or a liquid phase epitaxy (LPE) method.

[0104]

In this embodiment, each layer is epitaxially grown by a reduced-pressure MOCVD method using trimethylaluminum ($((\text{CH}_3)_3\text{Al})$), trimethylgallium ($((\text{CH}_3)_3\text{Ga})$) and trimethylindium ($((\text{CH}_3)_3\text{In})$) as a raw material for a group-III element.

Bis(cyclopentadienyl)magnesium ($((\text{C}_5\text{H}_5)_2\text{Mg})$) is used as a MG doping material. In addition, disilane ((Si_2H_6)) is used as a Si doping material. Phosphine ((PH_3)) or arsine ((AsH_3)) is used as a raw material for a group-V element.

A p-type GaP layer 3 is grown at a temperature of, for example, 750°C and the other epitaxially grown layers are grown at a temperature of, for example, 730°C .

[0105]

Specifically, first, a buffer layer 62a which is made of Si-doped n-type GaAs is formed on the one surface 61a of the growth substrate 61. For example, the buffer layer 62a is made of, for example, Si-doped n-type GaAs and has a carrier concentration of

$2 \times 10^{18} \text{ cm}^{-3}$ and a thickness of $0.2 \text{ } \mu\text{m}$.

[0106]

Then, in this embodiment, an etching stop layer 62b is formed on the buffer layer 62a.

5 The etching stop layer 62b is used to prevent the cladding layer and the light-emitting layer from being etched when the semiconductor substrate is removed by etching, is made of, for example, Si-doped $(\text{Al}_{0.5}\text{Ga}_{0.5})_{0.5}\text{In}_{0.5}\text{P}$, and has a thickness of $0.5 \text{ } \mu\text{m}$.

[0107]

10 Then, the contact layer 5 which is made of, for example, Si-doped n-type $\text{Al}_X\text{Ga}_{1-X}\text{As}$ ($0.1 \leq X \leq 0.3$) is formed on the etching stop layer 62b.

[0108]

Then, a cladding layer 63a which is made of, for example, Si-doped n-type $(\text{Al}_{0.7}\text{Ga}_{0.3})_{0.5}\text{In}_{0.5}\text{P}$ is formed on the contact layer 5.

15 [0109]

Then, a light-emitting layer 64 having a laminated structure of three pairs of well layers and barrier layers which respectively consists of, for example, $\text{Al}_{0.17}\text{Ga}_{0.83}\text{As}$ and $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ is formed on the cladding layer 63a.

[0110]

20 Then, a cladding layer 63b which consists of, for example, Mg-doped p-type $(\text{Al}_{0.7}\text{Ga}_{0.3})_{0.5}\text{In}_{0.5}\text{P}$ is formed on the light-emitting layer 64.

[0111]

Then, a bonding (contact) layer 3 which is, for example, a Mg-doped p-type GaP layer is formed on the cladding layer 63b.

25 Before the epitaxial laminate is bonded to a substrate, such as a metal substrate

which will be described below, it is preferably polished by about 1 μm in order to process the bonding surface (that is, to perform a mirroring process such that surface roughness is equal to or less than, for example, 0.2 nm).

[0112]

5 A guide layer may be provided between the cladding layer and the light-emitting layer.

[0113]

<Process of Forming Transparent Film and Through-electrode>

10 In this process, as shown in FIG. 9, a transparent film 30 and a through-electrode 31 (in the second embodiment, a “through-electrode 32”) which is formed in the transparent film 30 so as to pass through the transparent film 30 are formed on the epitaxial laminate 80.

15 One of the transparent film 30 and the through-electrode 31 may be formed first by a known method. A case in which the transparent film 30 and the through-electrode 31 are formed in this order will be described below.

[0114]

First, the transparent film 30 is formed on the entire bonding (contact) layer 3 by, for example, a CDV method.

20 Then, a hole for a through-electrode is formed in a range (in the second embodiment, “at a position which overlaps an electrical conduction window, which will be formed, in plane view”) of the transparent film 30 which overlaps a light emission hole, which will be formed, in plane view by a photolithography method and an etching method.

25 Specifically, a resist pattern with an opening corresponding to the hole for a through-electrode is formed on the transparent film 30 and the hole for a

through-electrode is formed in the transparent film 30 by etching.

Then, a film which is made of a metal material for forming the through-electrode is formed by the entire surface of the transparent film 30 by, for example, a vapor deposition method to fill the through-electrode in the transparent film 30, thereby forming the through-electrode 31 in the transparent film 30.

Then, the resist pattern is removed.

[0115]

<Process of Forming Reflecting Layer>

Then, as shown in FIG. 9, a reflecting layer 2 which consists of, for example, Au is formed on the transparent film 30.

[0116]

<Process of Bonding Supporting Substrate>

[1] When Ge Substrate Is Used as Supporting Substrate 1 (See Reference Numerals in FIG. 10A)

The In layer on the front surface of the supporting substrate 1, which is produced by forming the layer 42 consisting of a Ti layer, an Au layer, and an In layer on the front surface of the germanium substrate 41 and by forming the layer 43 consisting of a Ti layer and an Au layer on the rear surface, and the reflecting layer 2 which is made of Au in the structure shown in FIG. 10A overlap each other, are heated at, for example, 320°C, are pressed at 500 g/cm². In this way, as shown in FIG. 10A, the supporting substrate 1 is bonded to the structure including the epitaxial laminate.

[0117]

[2] When Metal Substrate Is Used as Supporting Substrate 1

Before the metal substrate is bonded to the reflecting layer 2, a barrier layer (not shown) and/or a bonding layer (not shown) may be sequentially formed on the reflecting

layer 2.

[0118]

The barrier layer can prevent metal contained in the metal substrate from being diffused and reacting with the reflecting layer 2.

5 For example, it is possible to use nickel, titanium, platinum, chromium, tantalum, tungsten, or molybdenum as the barrier layer. The barrier layer may be a combination of two or more types of metal layers, for example, a combination of a platinum layer and a titanium layer which are sequentially provided from the reflecting layer. In this case, it is possible to improve the performance of the barrier.

10 Even if the barrier layer is not provided, the bonding layer can obtain a same function as the barrier layer by adding these materials to the bonding layer.

[0119]

The bonding layer is used to closely bond, for example, a compound semiconductor layer 20 including the active layer 4 to the metal substrate 1.

15 For example, an Au-based eutectic metal material which is chemically stable and has a low melting point can be used as the material forming the bonding layer. Examples of the Au-based eutectic metal material include eutectic alloys, such as AuGe, AuSn, AuSi, and AuIn.

[0120]

20 Then, as shown in FIG. 10B, the semiconductor substrate 61 having the epitaxial laminate 80 or the reflecting layer 2 formed thereon and the metal substrate 1 which is formed by the metal substrate producing process are put into a decompression device and are arranged such that the bonding surface of the reflecting layer (a bonding surface of a bonding layer when the bonding layer is provided (the bonding layer is not shown in FIG.
25 10B)) and a bonding surface 1A of the metal substrate 1 face and overlap each other.

Then, the inside of the decompression device is evacuated to 3×10^{-5} Pa and the semiconductor substrate 61 and the metal substrate 1 which overlap each other are heated at 400°C. In this state, a load of 500 kg is applied to bond the bonding surface of the reflecting layer (the bonding surface of the bonding layer when the bonding layer is provided) and the bonding surface 1A of the metal substrate 1. In this way, a bonding structure 90 is formed.

[0121]

Next, a case in which a Ge substrate is used as the supporting substrate 1 will be described.

[0122]

<Process of Removing Semiconductor Substrate and Buffer Layer>

Then, as shown in FIG. 11, the semiconductor substrate 61 and the buffer layer 62a are selectively removed from the bonding structure 90 by an ammonia-based etchant.

In this case, since the metal substrate according to this embodiment is covered with the metal protective film and has high resistance to an etchant, it is possible to prevent the deterioration of the quality of the metal substrate.

[0123]

<Process of Removing Etching Stop Layer>

Then, as shown in FIG. 11, the etching stop layer 62b is selectively removed by a hydrochloric acid-based etchant.

Since the metal substrate according to this embodiment is covered with the metal protective film and has high resistance to an etchant, it is possible to prevent the deterioration of the quality of the metal substrate.

[0124]

(Process of Forming Back Electrode)

Then, as shown in FIG. 11, a back electrode 40 is formed on the rear surface of the metal substrate 1.

When the metal substrate is used as the supporting substrate 1, the back electrode 40 may not be formed.

5 [0125]

(Process of Forming Mesa Structure Portion)

Then, wet etching is performed on the compound semiconductor layer in a portion other than the mesa structure portion, that is, the contact layer and at least a portion of the active layer, or the contact layer, the active layer, and at least a portion of the bonding (contact) layer in order to form the mesa structure portion (except the protective film and the electrode film). Wet etching is performed on the contact layer 5 and the active layer 4 in order to form the mesa structure portion shown in FIG. 1.

Specifically, first, as shown in FIG. 12, a photoresist is deposited on the contact layer, which is the uppermost layer of the compound semiconductor layer, and a resist pattern 65 which has an opening 65a in a portion other than the mesa structure portion is formed by photolithography.

The shape of the mesa structure portion in plane view is determined by the shape of the opening 65a of the resist pattern 65. The opening 65a which has a shape corresponding to a desired shape in plane view is formed in the resist pattern 65.

20 It is preferable that the size of a portion of the resist pattern in which the mesa structure portion will be formed is about 10 μm greater than each of the upper, lower, left, and right sides of the top surface of the "mesa structure portion".

An etching depth, that is, the layer to be removed by etching in the compound semiconductor layer is determined by the type of etchant and an etching time.

25 After wet etching is performed, the resist is removed.

[0126]

Then, wet etching is performed on the compound semiconductor layer in the portion other than the mesa structure portion.

An etchant used for the wet etching is not limited. An ammonia-based etchant
5 (for example, a mixture of ammonia, hydrogen peroxide, and water) is suitable as an As-based compound semiconductor material such as AlGaAs. An iodine-based etchant (for example, potassium iodide/ammonia) is suitable as a P-based compound semiconductor material such as AlGaInP. A mixture of a phosphoric acid and a hydrogen peroxide solution is suitable as an AlGaAs-based material. A mixture of
10 bromine and methanol is suitable as a P-based material.

In a structure in which the compound semiconductor layer is made of only an As-based material, a phosphoric acid mixture may be used. In a structure in which As and a P-based material is mixed, an ammonia mixture may be used for an As-based structure portion and an iodine mixture may be used for a P-based structure portion.

15 [0127]

In the above-mentioned compound semiconductor layer, that is, in the compound semiconductor layer including the contact layer 5 which is the uppermost layer and is made of AlGaAs, the cladding layer 63a which is made of AlGaInP, the light-emitting layer 64 which is made of AlGaAs, the cladding layer 63b which is made
20 of AlGaInP, and the GaP layer 3, it is preferable that an etchant, which is used for As-based contact layer 5 and light-emitting layer 64, and the other etchant, which is used for other P-based layers, have high etching rate in each layer.

For example, it is preferable that an iodine-based etchant be used to etch the P-based layer and an ammonia-based etchant be used to etch the As-based contact layer 5
25 and light-emitting layer 64.

For example, an etchant having iodine (I), potassium iodide (KI), pure water (H_2O), or ammonia water (NH_4OH) mixed therewith can be used as the iodine-based etchant.

In addition, for example, a mixture of ammonia, hydrogen peroxide, and water
5 ($\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$) can be used as the ammonia-based etchant.

[0128]

A case in which the portion other than the mesa structure portion is removed by the preferred etchant will be described. First, the contact layer 5 which is arranged in the portion other than the mesa structure portion and consists of AlGaAs is removed by
10 etching with the ammonia-based etchant.

During the etching, since the cladding layer 63a, which consists of AlGaInP and is the next layer, has functions as an etching stop layer, it is not necessary to strictly manage the etching time. For example, when the thickness of the contact layer 5 is about $0.05\text{ }\mu\text{m}$, the etching may be performed for about 10 seconds.

15 [0129]

Then, the cladding layer 63a which is arranged in the portion other than the mesa structure portion and consists of AlGaInP is removed by etching using the iodine-based etchant.

When an etchant containing 500 cc of iodine (I), 100 g of potassium iodide (KI),
20 2000 cc of pure water (H_2O), and 90 cc of ammonium hydroxide (NH_4OH) mixed with each other at this rate was used, the etching speed was $0.72\text{ }\mu\text{m}/\text{min}$.

During the etching, since the light-emitting layer 64 which consists of AlGaAs and is the next layer, has functions as an etching stop layer, it is not necessary to strictly manage the etching time. For example, when the thickness of the cladding layer 63a is
25 about $4\text{ }\mu\text{m}$, the etching may be performed for about 6 minutes.

[0130]

Then, the light-emitting layer 64, which is arranged in the portion other than the mesa structure portion and consists of AlGaAs, is removed by etching with the ammonia-based etchant.

5 During the etching, since the cladding layer 63b which consists of AlGaInP and is the next layer, has functions as an etching stop layer, it is not necessary to strictly manage the etching time. For example, when the thickness of the light-emitting layer 64 is about 0.25 μm , the etching may be performed for about 40 seconds.

[0131]

10 Then, the cladding layer 63b, which is arranged in the portion other than the mesa structure portion and consists of AlGaInP, is removed by etching with the iodine-based etchant.

The GaP layer 3 is arranged below the cladding layer 63b. Since the exposure of the reflecting layer 2 which is made of metal and is arranged below the GaP layer 3 is not preferable in terms of electric characteristics, the GaP layer 3 also needs to function
15 as an etching stop layer.

For example, when the GaP layer is formed with a thickness of 3.5 μm and is polished by 1 μm , the thickness of the GaP layer is 2.5 μm . When the thickness of the cladding layer 63b is 0.5 μm and the iodine-based etchant is used, the etching time needs
20 to be equal to or less than 4 minutes.

[0132]

When a mixture of phosphoric acid, hydrogen peroxide, and water (for example, $\text{H}_2\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 1$ to 3:4 to 6:8 to 10) is used, the etching can be performed for a wet etching time of 30 seconds to 120 seconds.

[0133]

FIG. 13 shows the relationship among the depth, the width, and the etching time when wet etching is performed on a compound semiconductor layer according to

Example 1, which will be described below, using an etchant which is a mixture of

5 $\text{H}_2\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 2:5:9$ (100:250:450), contains 56% of H_2O , and is at a temperature of 30°C to 34°C . The conditions and results are numerically shown in Table 1.

[0134]

[Table 1]

TIME (sec)	DEPTH (μm)	WIDTH (μm)
5	0.45	0.25
10	0.91	0.55
30	2.7	1.6
45	4.2	2.6
60	5.45	3.8
90	8.5	7.2

10 [0135]

As can be seen from FIG. 13 and Table 1, the etching depth (corresponding to “h” in FIG. 1) is substantially proportional to the etching time (sec) and the rate of increase in the etching width increases as the etching time increases. That is, as shown in FIG. 13, as the depth increases (as it goes down in FIG. 13), the rate of increase in the

15 horizontal cross-sectional area (or the width or diameter) of the mesa structure portion increases. The etching shape is different from an etching shape by dry etching.

Therefore, it is possible to determine whether the mesa structure portion is formed by dry etching or wet etching on the basis of the shape of the inclined side surface of the mesa structure portion.

20 [0136]

(Process of Forming Protective Film)

Then, the material forming the protective film 8 is deposited on the entire surface. Specifically, for example, a SiO₂ film is formed on the entire surface by a sputtering method.

[0137]

5 (Process of Removing Protective Film Corresponding to Street and Contact Layer)

Then, a photoresist is deposited on the entire surface and a resist pattern in which a portion corresponding to the electrical conduction window 8b and a portion corresponding to the street are opened is formed on the contact layer by photolithography.

10 Then, for example, in the material forming the protective film 8, a portion corresponding to the electrical conduction window 8b in the top surface of the mesa structure portion and a portion corresponding to the street are removed by wet etching with a buffered hydrofluoric acid to form the protective film 8.

FIG. 14 is a plane view illustrating the vicinity of the electrical conduction
15 window 8b of the protective film 8.

Then, the resist is removed.

[0138]

(Process of Forming Front Surface Electrode Film)

Then, the front surface electrode film 9 is formed. That is, the front surface
20 electrode film 9 including the light emission hole 9b is formed on the protective film 8 and on a portion of the contact layer 5 which is exposed from the electrical conduction window 8b of the protective film 8.

Specifically, a photoresist is deposited on the entire surface and a resist pattern in which portions that include a portion corresponding to the light emission hole 9b and a
25 cutting portion (street) between a plurality of light-emitting diodes on a wafer substrate

and a portion which is not required to form the electrode film are opened is formed by photolithography. Then, an electrode film material is vapor-deposited. When the electrode film material is not sufficiently vapor-deposited on the inclined side surface of the mesa structure portion only by the vapor deposition, it is further vapor-deposited on the inclined side surface of the mesa structure portion by a planetary deposition apparatus in which deposition metal easily goes round.

Then, the resist is removed.

[0139]

The shape of the light emission hole 9b is determined by the shape of the opening in the resist pattern (not shown). A resist pattern in which the shape of the opening corresponds to the desired shape of the light emission hole 9b is formed.

[0140]

(Dividing Process)

Then, the wafer substrate is cut into light-emitting diodes.

Specifically, for example, the wafer substrate is cut into light-emitting diodes along the street portions by a dicing saw or a laser.

[0141]

(Process of Forming Metal Protective Film on Side Surface of Metal Substrate)

When a metal substrate is used as the supporting substrate, the metal protective film may be formed on the cut side surface of the metal substrate of each divided light-emitting diode under the same conditions as those for forming the metal protective film on the upper surface and the lower surface.

[Example]

[0142]

(Example)

Hereinafter, the light-emitting diode according to the invention will be further described in detail using an example of the first embodiment. However, the invention is not limited only to this example. In this example, a light-emitting diode lamp having a light-emitting diode chip mounted on a substrate was manufactured for characteristic
5 evaluation.

In this example, with reference to FIGS. 1 and 4, the outside diameter R1 of an electrical conduction window 8b was 166 μm , the inside diameter thereof was 154 μm , the diameter R2 of a light emission hole was 150 μm , and the outside diameter R5 of a through-electrode 31 was 100 μm .

10 [0143]

First, a layer 42 consisting of a Ti layer with a thickness of 0.1 μm , an Au layer with a thickness of 0.5 μm , and an In layer with a thickness of 0.3 μm was formed on the surface of a germanium substrate 41. A layer 43 consisting of a Ti layer with a thickness of 0.1 μm and an Au layer with a thickness of 0.5 μm was formed on the rear
15 surface of the germanium substrate 41.

[0144]

Then, compound semiconductor layers were sequentially laminated on a GaAs substrate which consists of a Si-doped n-type GaAs single crystal to produce an epitaxial wafer with an emission wavelength of 730 nm.

20 The GaAs substrate had a surface which was inclined at an angle of 15° with respect to the (100) plane in the (0-1-1) direction as a growth surface and had a carrier concentration of $2 \times 10^{18} \text{ cm}^{-3}$. In addition, the thickness of the GaAs substrate was about 0.5 μm . The compound semiconductor layers include an n-type buffer layer 62a which consists of Si-doped GaAs, an etching stop layer 62b which consists of Si-doped

(Al_{0.5}Ga_{0.5})_{0.5}In_{0.5}P, a contact layer 5 which consists of Si-doped n-type Al_{0.3}GaAs, an n-type upper cladding layer 63a which consists of Si-doped (Al_{0.7}Ga_{0.3})_{0.5}In_{0.5}P, an upper guide layer which consists of Al_{0.4}Ga_{0.6}As, a well layer/barrier layer 64 which consists of Al_{0.17}Ga_{0.83}As/Al_{0.3}Ga_{0.7}As, a lower guide layer which consists of Al_{0.4}Ga_{0.6}As, a p-type lower cladding layer 63b which consists of Mg-doped (Al_{0.7}Ga_{0.3})_{0.5}In_{0.5}P, a thin intermediate layer which consists of (Al_{0.5}Ga_{0.5})_{0.5}In_{0.5}P, and a Mg-doped p-type GaP layer 3.

[0145]

In this example, the compound semiconductor layers were epitaxially grown on the GaAs substrate with a diameter of 50 mm and a thickness of 250 μm by a reduced-pressure metal organic chemical vapor deposition method (MOCVD apparatus) to form an epitaxial wafer. When the epitaxial growth layer was grown, trimethylaluminum ((CH₃)₃Al), trimethylgallium ((CH₃)₃Ga), and trimethylindium ((CH₃)₃In) were used as a raw material for a group-III element. In addition, bis(cyclopentadienyl)magnesium (bis-(C₅H₅)₂Mg) was used as a MG doping material. In addition, disilane (Si₂H₆) was used as a Si doping material. Phosphine (PH₃) or arsine (AsH₃) was used as a raw material for a group-III element.

For the growth temperature of each layer, the p-type GaP layer was grown at 750°C. The other layers were grown at 700°C.

[0146]

The buffer layer which consisted of GaAs had a carrier concentration of about $2 \times 10^{18} \text{ cm}^{-3}$ and a thickness of about 0.5 μm . The etching stop layer had a carrier concentration of $2 \times 10^{18} \text{ cm}^{-3}$ and a thickness of about 0.5 μm . The contact layer had a carrier concentration of about $2 \times 10^{18} \text{ cm}^{-3}$ and a thickness of about 0.05 μm . The upper

cladding layer had a carrier concentration of about $1 \times 10^{18} \text{ cm}^{-3}$ and a thickness of about 3.0 μm . The well layer was undoped, consisted of $\text{Al}_{0.17}\text{Ga}_{0.83}\text{As}$, and had a thickness of about 7 nm. The barrier layer was undoped, was made of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$, and had a thickness of about 19 nm. Three pairs of the well layers and the barrier layers were alternately laminated. The lower guide layer was undoped and had a thickness of about 50 nm. The lower cladding layer had a carrier concentration of about $8 \times 10^{17} \text{ cm}^{-3}$ and a thickness of about 0.5 μm . The intermediate layer had a carrier concentration of about $8 \times 10^{17} \text{ cm}^{-3}$ and a thickness of about 0.05 μm . The GaP layer had a carrier concentration of about $3 \times 10^{18} \text{ cm}^{-3}$ and a thickness of about 3.5 μm .

10 [0147]

Then, the GaP layer 3 was polished to a depth of about 1 μm from the surface by mirror-like polishing. The surface roughness of the GaP layer was 0.18 nm by the mirror-like polishing.

[0148]

15 Then, the through-electrode 31 which consisted of AuBe and had a thickness of 500 nm and an outside diameter R5 (see FIG. 4) of 100 μm and a transparent film 30 which consisted of SiO_2 and had a thickness of 500 nm were formed on the GaP layer 3.

[0149]

20 Then, a reflecting layer 2 which consisted of Au and had a thickness of 0.7 μm was formed on the transparent film 30 and the through-electrode 31. In addition, a Ti layer with a thickness of 0.5 μm was formed as the barrier layer on the reflecting layer and an AuGe layer with a thickness of 1.0 μm was formed as the bonding layer on the barrier layer.

[0150]

Then, the structure having the compound semiconductor layers and the reflecting layer formed on the GaAs substrate and the metal substrate were arranged so as to face each other, were carried into the decompression device, and were heated at 400°C. In this state, a load of 500 kg was applied to bond the structure and the metal substrate, thereby forming a bonding structure.

[0151]

Then, the GaAs substrate, which is a growth substrate for the compound semiconductor layers, and the buffer layer were selectively removed from the bonding structure by an ammonia-based etchant. In addition, the etching stop layer was selectively removed by a hydrochloric acid-based etchant.

[0152]

(Process of Forming Rear Surface Electrode)

Then, an Au film with a thickness of 1.2 μm and an AuBe film with a thickness of 0.15 μm were sequentially formed on the rear surface of the metal substrate 1 by a vacuum vapor deposition method to form a back electrode 40.

[0153]

Then, in order to form a mesa structure portion, a resist pattern was formed and wet etching was performed with a mixture of ammonia, hydrogen peroxide, and water ($\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$) for 10 seconds to remove the contact layer 5 in a portion other than the mesa structure portion.

Then, wet etching was performed with an iodine-based etchant which contained 500 cc of iodine (I), 100 g of potassium iodide (KI), 2000 cc of pure water (H_2O), and 90 cc of ammonium hydroxide water (NH_4OH) at this ratio for 45 seconds to remove the upper cladding layer 63a in the portion other than the mesa structure portion.

Then, wet etching was performed with the mixture of ammonia, hydrogen

peroxide, and water ($\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$) for 40 seconds to remove the upper guide layer, the light-emitting layer 64, and the lower guide layer in the portion other than the mesa structure portion.

Then, wet etching was performed with the iodine-based etchant for 50 seconds
5 to remove the lower cladding layer 63b in the portion other than the mesa structure portion.

In this way, the mesa structure portion was formed.

[0154]

Then, in order to form a protective film, the protective film which consisted of
10 SiO_2 was formed with a thickness of about $0.5\ \mu\text{m}$.

Then, a resist pattern was formed and an opening (see FIG. 11) which had a concentric shape (an outside diameter d_{out} : $166\ \mu\text{m}$; and an inside diameter d_{in} : $154\ \mu\text{m}$) in plane view and an opening for the street portion were formed using a buffered hydrofluoric acid.

15 [0155]

Then, in order to form a front surface electrode (film), a resist pattern was formed, an AuGe film with a thickness of $0.5\ \mu\text{m}$, a Ni alloy film with a thickness of $0.5\ \mu\text{m}$, a Pt film with a thickness of $0.2\ \mu\text{m}$, and an Au film with a thickness of $1\ \mu\text{m}$ were formed by a vacuum vapor deposition method, and the front surface electrode (n-type
20 ohmic electrode) which included a light emission hole 9b with a circular shape (diameter : $150\ \mu\text{m}$) in plane view and had a long side of $350\ \mu\text{m}$ and a short side of $250\ \mu\text{m}$ was formed by a liftoff technique.

Then, a heat treatment was performed at 450°C for 10 minutes to change the materials into an alloy, thereby forming a low-resistance n-type ohmic electrode.

[0156]

Then, in order to form a light leakage prevention film 16 on the side surface of the mesa structure portion, a resist pattern was formed, a Ti film with a thickness of 0.5 μm and an Au film with a thickness of 0.17 μm were sequentially formed by vapor deposition, and the light leakage prevention film 16 was formed by the liftoff technique.

[0157]

Then, wet etching and laser cutting were sequentially performed to divide the wafer into light-emitting diodes. In this way, the light-emitting diode according to the example was manufactured.

10 [0158]

100 light-emitting diode lamps each having the manufactured light-emitting diode chip according to the example mounted on a mount substrate were assembled. The light-emitting diode lamp was produced by supporting (mounting) a mount with a die bonder, connecting a p-type ohmic electrode and a p electrode terminal with a gold line using wire bonding, and performing sealing with a general epoxy resin.

[0159]

In the light-emitting diode (light-emitting diode lamp), when a current flowed between the n-type electrode and the p-type electrode, infrared light with a peak wavelength 730 of nm was emitted. When a current of 20 milliamperes (mA) flowed in the forward direction, a forward voltage (V_F) was 1.8V. When the forward current was 20 mA, an emission output was 4.3 mW. A response speed (rise time: T_r) was 12 nsec.

[0160]

The 100 manufactured light-emitting diode lamps had the same characteristics and there was no defect due to leakage (short-circuit), which causes when the protective film was a discontinuous film, or an electrical conduction failure, which causes when the

electrode metal film is a discontinuous film.

[0161]

(Comparative Example)

A light-emitting diode according to a comparative example was formed by a liquid phase epitaxial method according to the related art. The light-emitting diode included a light emission portion with a double hetero structure in which an $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ light-emitting layer was formed on a GaAs substrate.

[0162]

Specifically, the light-emitting diode according to the comparative example was manufactured by the liquid phase epitaxial method such that an n-type upper cladding layer that consisted of $\text{Al}_{0.7}\text{Ga}_{0.3}\text{As}$ and had a thickness of 20 μm , an undoped light-emitting layer that consisted of $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ and had a thickness of 2 μm , a p-type lower cladding layer that consisted of $\text{Al}_{0.7}\text{Ga}_{0.3}\text{As}$ and had a thickness of 20 μm , and a p-type thick layer that consisted of $\text{Al}_{0.6}\text{Ga}_{0.4}\text{As}$, which was transparent with respect to an emission wavelength, and had a thickness of 120 μm were formed on an n-type GaAs single crystal substrate with the (100) plane. After the epitaxial growth, the GaAs substrate was removed. Then, an n-type ohmic electrode with a diameter of 100 μm was formed on the surface of the n-type AlGaAs substrate. Then, p-type ohmic electrodes with a diameter 20 of μm were formed on the rear surface of the p-type AlGaAs layer at intervals of 80 μm . Then, the substrate was cut by a dicing saw at intervals of 350 μm and a broken layer was removed by etching. In this way, the light-emitting diode chip according to the comparative example was manufactured.

[0163]

When a current flowed between the n-type electrode and the p-type electrode,

infrared light with a peak wavelength 730 of nm was emitted. When a current of 20 milliamperes (mA) flowed in the forward direction, a forward voltage (V_F) was about 1.9 volts (V). When the forward current was 20 mA, an emission output was 5 mW. A response speed (T_r) was 15.6 nsec, which was later than that in the example according to the invention.

Reference Signs List

[0164]

- 1: SUPPORTING SUBSTRATE
- 2: REFLECTING LAYER
- 10 3: BONDING (CONTACT) LAYER
- 4: ACTIVE LAYER
- 5: CONTACT LAYER
- 6: FLAT PORTION
- 7: MESA STRUCTURE PORTION
- 15 7a: INCLINED SIDE SURFACE
- 7b: TOP SURFACE
- 7ba: PERIPHERAL REGION
- 8, 28: PROTECTIVE FILM
- 8b, 28b: ELECTRICAL CONDUCTION WINDOW
- 20 9, 29: ELECTRODE FILM
- 9b, 29b: LIGHT EMISSION HOLE
- 11: LOWER CLADDING LAYER
- 12: LOWER GUIDE LAYER
- 13: LIGHT-EMITTING LAYER
- 25 14: UPPER GUIDE LAYER

- 15: UPPER CLADDING LAYER
- 16: LIGHT LEAKAGE PREVENTION FILM
- 20: COMPOUND SEMICONDUCTOR LAYER
- 30: TRANSPARENT FILM
- 5 31, 32: THROUGH-ELECTRODE
- 40: BACK ELECTRODE
- 51C: METAL PROTECTIVE FILM
- 61: SEMICONDUCTOR SUBSTRATE (GROWTH SUBSTRATE)
- 63a: UPPER CLADDING LAYER
- 10 63b: LOWER CLADDING LAYER
- 64: LIGHT-EMITTING LAYER
- 65: RESIST PATTERN
- 100, 200: LIGHT-EMITTING DIODE

What is claimed is

1. A light-emitting diode that outputs light from a light emission hole to the
5 outside, comprising:
 - a reflecting layer that consists of metal;
 - a transparent film; and
 - a compound semiconductor layer that sequentially includes an active layer and a
10 contact layer; on a supporting substrate in this order,
 - wherein a flat portion and a mesa structure portion including an inclined side
surface and a top surface are provided in an upper part of the light-emitting diode,
 - wherein
 - at least a part of the flat portion and at least a part of the mesa structure portion
15 are sequentially covered with a protective film and an electrode film,
 - the mesastructure portion includes at least a portion of the active layer,
 - the inclined side surface is formed by wet etching,
 - a cross-sectional area of the mesa structure portion in a horizontal direction is
continuously reduced toward the top surface,
 - 20 the protective film covers at least a part of the flat portion, the inclined side
surface of the mesa structure portion, and a peripheral region of the top surface of the
mesa structure portion and includes an electrical conduction window which is provided
inside the peripheral region in plane view and is arranged around the light emission hole
and from which a portion of a surface of the compound semiconductor layer is exposed,
 - 25 the electrode film is a continuous film that comes into direct contact with the

surface of the compound semiconductor layer which is exposed from the electrical conduction window, covers at least a portion of the protective film formed on the flat portion, and has the light emission hole on the top surface of the mesa structure portion,

the transparent film is formed between the reflecting layer and the compound semiconductor layer, and

a through-electrode is provided in a range of the transparent film which overlaps the light emission hole in plane view so as to come into contact with the compound semiconductor layer and the reflecting layer.

2. A light-emitting diode that outputs light from a light emission hole to the outside, comprising:

a reflecting layer that consists of metal;

a transparent film; and

a compound semiconductor layer that sequentially includes an active layer and a contact layer; on a supporting substrate in this order,

wherein a flat portion and a mesa structure portion including an inclined side surface and a top surface are provided in an upper part of the light-emitting diode,

wherein at least a part of the flat portion and at least a part of the mesa structure portion are sequentially covered with a protective film and an electrode film,

the mesa structure portion includes at least a portion of the active layer,

the inclined side surface is formed by wet etching,

a cross-sectional area of the mesa structure portion in a horizontal direction is continuously reduced toward the top surface,

the protective film covers at least a part of the flat portion, the inclined side

surface of the mesa structure portion, and a peripheral region of the top surface of the mesa structure portion and includes an electrical conduction window which is provided inside the peripheral region in plane view and is arranged around the light emission hole and from which a portion of a surface of the compound semiconductor layer is exposed,

5 the electrode film is a continuous film that comes into direct contact with the surface of the compound semiconductor layer which is exposed from the electrical conduction window, covers at least a portion of the protective film formed on the flat portion, and has the light emission hole on the top surface of the mesa structure portion,

 the transparent film is formed between the reflecting layer and the compound
10 semiconductor layer, and

 a through-electrode is provided in the transparent film at a position that overlaps the electrical conduction window in plane view so as to come into contact with the compound semiconductor layer and the reflecting layer.

15 3. The light-emitting diode according to Claim 1,

 wherein the through-electrode is formed in a range of a reduced and projected figure of the light emission hole which is reduced and projected onto the transparent film by extending a segment that connects each point on the outer circumference of the electrical conduction window and each point on the outer circumference of a figure
20 obtained by projecting the light emission hole onto the active layer at the shortest distance.

 4. The light-emitting diode according to any one of Claims 1 to 3,

 wherein the through-electrode consists of AuBe or AuZn.

5. The light-emitting diode according to any one of Claims 1 to 3,
wherein the transparent film consists of any one of SiO₂, SiN, SiON, Al₂O₃,
MgF₂, TiO₂, TiN, and ZnO.

5 6. The light-emitting diode according to any one of Claims 1 to 3,
wherein the contact layer comes into contact with the electrode film.

7. The light-emitting diode according to any one of Claims 1 to 3,
wherein the mesa structure portion has a rectangular shape in plane view.

10

8. The light-emitting diode according to Claim 7,
wherein each inclined side surface of the mesa structure portion is formed so as
to be offset from an orientation flat of the substrate.

15

9. The light-emitting diode according to any one of Claims 1 to 3,
wherein the mesa structure portion has a height of 3 μm to 7 μm, and
the width of the inclined side surface in plane view is in the range of 0.5 μm to 7
μm.

20

10. The light-emitting diode according to any one of Claims 1 to 3,
wherein the light emission hole has a circular shape or an elliptical shape in
plane view.

25

11. The light-emitting diode according to Claim 10,
wherein the light emission hole has a diameter of 50 μm to 150 μm.

12. The light-emitting diode according to any one of Claims 1 to 3,
wherein a bonding wire is provided on the flat portion of the electrode film.

5 13. The light-emitting diode according to any one of Claims 1 to 3,
wherein a light-emitting layer that is included in the active layer has a multiple
quantum well structure.

14. The light-emitting diode according to any one of Claims 1 to 3,
10 wherein a light-emitting layer that is included in the active layer consists of any
one of $(\text{Al}_{X1}\text{Ga}_{1-X1})_{Y1}\text{In}_{1-Y1}\text{P}$ ($0 \leq X1 \leq 1$, $0 < Y1 \leq 1$), $(\text{Al}_{X2}\text{Ga}_{1-X2})\text{As}$ ($0 \leq X2 \leq 1$), and
 $(\text{In}_{X3}\text{Ga}_{1-X3})\text{As}$ ($0 \leq X3 \leq 1$).

15. A method for producing a light-emitting diode that includes a reflecting
15 layer made of metal, a transparent film, and a compound semiconductor layer
sequentially including an active layer and a contact layer, which are sequentially
provided on a supporting substrate, in this order, and that emits light from a light
emission hole to the outside, the method comprising:

20 a step of forming the compound semiconductor layer that sequentially includes
the contact layer and the active layer on a growth substrate;

 a step of forming the transparent film and forming a through-electrode in a range
of the transparent film which overlaps the light emission hole to be formed in plane view
so as to come into contact with the compound semiconductor layer and the reflecting
layer, on the compound semiconductor layer;

25 a step of forming the reflecting layer made of metal on the transparent film and

the through-electrode;

a step of bonding the supporting substrate to the reflecting layer;

a step of removing the growth substrate;

a step of performing wet etching for the compound semiconductor layer to form

5 a mesa structure portion which is formed such that a cross-sectional area thereof in a horizontal direction is continuously reduced toward a top surface and a flat portion which is arranged around the mesa structure portion;

a step of forming a protective film that covers, at least, a part of the flat portion, the inclined side surface of the mesa structure portion, and a peripheral region of the top
10 surface of the mesa structure portion, and that includes an electrical conduction window which is provided inside the peripheral region and is arranged around the light emission hole in plane view and from which a portion of a surface of the compound semiconductor layer is exposed; and

a step of forming an electrode film which is a continuous film that comes into
15 direct contact with the surface of the compound semiconductor layer exposed from the electrical conduction window, that covers at least a portion of the protective film formed on the flat portion, and that has the light emission hole on the top surface of the mesa structure portion.

20 16. A method for producing a light-emitting diode that includes a reflecting layer made of metal, a transparent film, and a compound semiconductor layer sequentially including an active layer and a contact layer, which are sequentially provided on a supporting substrate, in this order, and that emits light from a light emission hole to the outside, the method comprising:

25 a step of forming the compound semiconductor layer that sequentially includes

the contact layer and the active layer on a growth substrate;

a step of forming the transparent film and forming a through-electrode in the transparent film at a position that overlaps an electrical conduction window to be formed in plane view so as to come into contact with the compound semiconductor layer and the
5 reflecting layer, on the compound semiconductor layer;

a step of forming the reflecting layer made of metal on the transparent film and the through-electrode;

a step of bonding the supporting substrate to the reflecting layer;

a step of removing the growth substrate;

10 a step of performing wet etching for the compound semiconductor layer to form a mesa structure portion which is formed such that a cross-sectional area thereof in a horizontal direction is continuously reduced toward a top surface and a flat portion which is arranged around the mesa structure portion;

a step of forming a protective film that covers, at least, a part of the flat portion,
15 the inclined side surface of the mesa structure portion, and a peripheral region of the top surface of the mesa structure portion, and that includes the electrical conduction window which is provided inside the peripheral region and is arranged around the light emission hole in plane view and from which a portion of a surface of the compound semiconductor layer is exposed; and

20 a step of forming an electrode film which is a continuous film that comes into direct contact with the surface of the compound semiconductor layer exposed from the electrical conduction window, that covers at least a portion of the protective film formed on the flat portion, and that has the light emission hole on the top surface of the mesa structure portion.

17. The method for producing a light-emitting diode according to Claim 15 or 16,

wherein the wet etching is performed with at least one of a mixture of phosphoric acid, hydrogen peroxide, and water, a mixture of ammonia, hydrogen
5 peroxide, and water, a mixture of bromine and methanol, and a mixture of potassium iodide and ammonia.