

SELECTIVE DEPOSITION PROCESSES ON SEMICONDUCTOR SUBSTRATES

TECHNICAL FIELD

5 [0001] Embodiments of the present disclosure pertain to methods of selective deposition facilitated by a flowable polymer. More particularly, embodiments of the disclosure are directed to methods of selectively depositing polysilicon after use of a flowable polymer to protect a substrate surface within a feature.

BACKGROUND

10 [0002] Gap fill processes are integral to several semiconductor manufacturing processes. A gap fill process can be used to fill a gap (or feature) with an insulating or conducting material. For example, shallow trench isolation, inter-metal dielectric layers, passivation layers, dummy gate, are all typically implemented by gap fill processes.

15 [0003] As device geometries continue to shrink (e.g., critical dimensions < 20 nm, < 10 nm, and beyond) and thermal budgets are reduced, defect-free filling of spaces becomes increasingly difficult due to the limitations of conventional deposition processes.

20 [0004] Polysilicon may be used in a variety of semiconductor applications, such as a thin film transistor, due to its unique electronic character. However, selective deposition of high quality silicon (Si) remains a challenge. Known physical vapor deposition (PVD) processes can provide high quality (Si) but are not selective. Additionally, there are no known processes for selectively depositing silicon (Si) on metal or metal silicide without causing damage to the underlying metal or metal
25 silicide.

[0005] Accordingly, there is a need for methods to protect the metal or metal silicide within a feature in order to enable bottom-up fill by selective polysilicon deposition processes.

SUMMARY

- [0006] One or more embodiments of the disclosure are directed to a method of selectively depositing polysilicon. The method comprises: depositing a first silicon (Si) layer by physical vapor deposition (PVD) on a semiconductor substrate surface with at least one feature formed thereon, the at least one feature having at least one opening at a top surface with an opening width, at least one sidewall, and a bottom, the at least one feature extending a feature depth from the top surface to the bottom, the first silicon (Si) layer forming on the top surface, along the at least one sidewall, and the bottom; forming a flowable polymer film on the first silicon (Si) layer within the at least one feature, the flowable polymer film forming on the first silicon (Si) layer on the bottom and having a polymer depth less than or equal to the feature depth; selectively removing at least a portion of the first silicon (Si) layer from the top surface and the at least one sidewall; and removing the flowable polymer film to expose the first silicon (Si) layer on the bottom of the at least one feature.
- [0007] Additional embodiments of the disclosure are directed to a method of selectively depositing polysilicon. The method comprises: depositing a first silicon (Si) layer by physical vapor deposition (PVD) on a semiconductor substrate surface with at least one feature formed thereon, the at least one feature having at least one opening at a top surface with an opening width, at least one sidewall, and a bottom, the at least one feature extending a feature depth from the top surface to the bottom, the first silicon (Si) layer forming on the top surface, along the at least one sidewall, and the bottom; forming a flowable polymer film on the first silicon (Si) layer within the at least one feature, the flowable polymer film forming on the first silicon (Si) layer on the bottom and having a polymer depth less than or equal to the feature depth; selectively removing at least a portion of the first silicon (Si) layer from the top surface and the at least one sidewall without substantially affecting any material beneath the flowable polymer film; removing the flowable polymer film to expose the first silicon (Si) layer on the bottom; and oxidizing the remaining portion of the first silicon (Si) layer to form a first silicon oxide (SiO_x) layer on the bottom.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] So that the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended
5 drawings illustrate only typical embodiments of this disclosure and are therefore not to be considered limiting of its scope, for the disclosure may admit to other equally effective embodiments.

[0009] The embodiments as described herein are illustrated by way of example and not limitation in the figures of the accompanying drawings in which like references
10 indicate similar elements.

[0010] FIG. 1 illustrates a process flow diagram of a method according to one or more embodiments;

[0011] FIG. 2 illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;

15 [0012] FIG. 3 illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;

[0013] FIG. 4 illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;

20 [0014] FIG. 5 illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;

[0015] FIG. 6 illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;

[0016] FIG. 7 illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;

25 [0017] FIG. 8A illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;

[0018] FIG. 8B illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments;

30 [0019] FIG. 8C illustrates a cross-sectional view of a semiconductor substrate according to one or more embodiments; and

[0020] FIG. 9 is a schematic top-view diagram of an example multi-chamber processing system according to one or more embodiments.

DETAILED DESCRIPTION

[0021] Before describing several exemplary embodiments of the disclosure, it is to be understood that the disclosure is not limited to the details of construction or process steps set forth in the following description. The disclosure is capable of other
5 embodiments and of being practiced or being carried out in various ways.

[0022] The term "about" as used herein means approximately or nearly and in the context of a numerical value or range set forth means a variation of $\pm 15\%$ or less, of the numerical value. For example, a value differing by $\pm 14\%$, $\pm 10\%$, $\pm 5\%$, $\pm 2\%$, $\pm 1\%$, $\pm 0.5\%$, or $\pm 0.1\%$ would satisfy the definition of about.

10 [0023] As used in this specification and the appended claims, the term "substrate" or "wafer" refers to a surface, or portion of a surface, upon which a process acts. It will also be understood by those skilled in the art that reference to a substrate can refer to only a portion of the substrate unless the context clearly indicates otherwise. Additionally, reference to depositing on a substrate can mean both a bare substrate
15 and a substrate with one or more films or features deposited or formed thereon.

[0024] A "substrate" as used herein, refers to any substrate or material surface formed on a substrate upon which film processing is performed during a fabrication process. For example, a substrate surface on which processing can be performed include materials such as silicon, silicon oxide, strained silicon, silicon on insulator
20 (SOI), carbon doped silicon oxides, amorphous silicon, doped silicon, germanium, gallium arsenide, and any other materials such as metals, metal nitrides, metal alloys, and other conductive materials, depending on the application. Substrates include, without limitation, semiconductor wafers. Substrates may be exposed to a pretreatment process to polish, etch, reduce, oxidize, hydroxylate, anneal and/or bake
25 the substrate surface. In addition to film processing directly on the surface of the substrate itself, in the present disclosure, any of the film processing steps disclosed may also be performed on an under-layer formed on the substrate as disclosed in more detail below, and the term "substrate surface" is intended to include such under-layer as the context indicates. Thus, for example, where a film/layer or partial
30 film/layer has been deposited onto a substrate surface, the exposed surface of the newly deposited film/layer becomes the substrate surface.

[0025] As used herein, the term "substrate surface" refers to any substrate surface upon which a layer may be formed. The substrate surface may have one or more features formed therein, one or more layers formed thereon, and combinations thereof. The shape of the feature can be any suitable shape including, but not limited to, peaks, trenches, holes and vias (circular or polygonal). As used in this regard, the term "feature" refers to any intentional surface irregularity. Suitable examples of features include but are not limited to trenches, which have a top, two sidewalls and a bottom extending into the substrate, vias which have one or more sidewall extending into the substrate to a bottom and slot vias.

10 [0026] As used in this specification and the appended claims, the term "selectively" refers to a process which acts on a first surface with a greater effect than another second surface. Such a process would be described as acting "selectively" on the first surface over the second surface. The term "over" used in this regard does not imply a physical orientation of one surface on top of another surface, rather a relationship of the thermodynamic or kinetic properties of the chemical reaction with one surface relative to the other surface.

[0027] The term "on" indicates that there is direct contact between elements. The term "directly on" indicates that there is direct contact between elements with no intervening elements.

20 [0028] As used in this specification and the appended claims, the terms "precursor," "reactant," "reactive gas" and the like are used interchangeably to refer to any gaseous species that can react with the substrate surface.

[0029] Embodiments of the disclosure advantageously provide methods for selectively depositing polysilicon after use of a flowable polymer to protect a substrate surface within a feature. One or more embodiments advantageously provide for the removal of a metallic material from the field and sidewalls of a feature without removal of a flowable polymer from the bottom surface of the substrate. The remaining flowable polymer has a smooth surface. Further embodiments advantageously provide methods for selectively depositing a metallic gap fill in a bottom-up fashion.

30 [0030] The embodiments of the disclosure are described by way of the Figures, which illustrate processes and substrates in accordance with one or more embodiments of the disclosure. The processes, schemes, and resulting substrates

shown are merely illustrative of the disclosed processes, and the skilled artisan will recognize that the disclosed processes are not limited to the illustrated applications.

[0031] In the following description, numerous specific details are set forth in order to provide a thorough understanding of embodiments. It will be apparent to one skilled in the art that embodiments may be practiced without these specific details. In other instances, well-known aspects are not described in detail in order to not unnecessarily obscure embodiments. Furthermore, it is to be understood that the various embodiments shown in the accompanying drawings are illustrative representations and are not necessarily drawn to scale.

10 [0032] Referring to the Figures, the disclosure relates to a method 100 of selective deposition of a gap fill material. FIG. 1 depicts a process flow diagram of a selective deposition method 100 in accordance with one or more embodiments of the present disclosure. FIGS. 2-8C depict a device 200 having a substrate surface with at least one feature formed therein during processing according to one or more embodiments of the present disclosure. FIG. 9 is a schematic top-view diagram of an example multi-chamber processing system for performing the methods according to one or more
15 embodiments.

[0033] FIG. 2 illustrates a semiconductor device 200 with a substrate surface 205. As identified above, the substrate surface refers to the exposed surface of the substrate upon which a process may be performed. The substrate surface 205 has at
20 least one feature 210 formed therein. While only three features are shown in the Figures, one skilled in the art will recognize that a plurality of features will each be affected by the disclosed methods in a similar manner.

[0034] The at least one feature 210 has an opening 212 with an opening width 202. The opening 212 is formed in a top surface 215 of the device 200. The feature 210
25 also has one or more sidewall 214 and extends a feature depth D from the top surface 215 to a bottom 216. While straight, vertical sidewalls are shown in the Figures, the disclosed methods may also be performed on slanted, irregular, or reentrant sidewalls.

30 [0035] In one or more embodiments, the device 200 illustrated in FIG. 2 is comprised of a material 220 on the feature 210. Those skilled in the art will recognize that the top surface 215, sidewall 214, and bottom 216 may each be comprised of one

- or more similar or different materials. For example, the lower portion of sidewall 214 may be formed from a first material while the upper portion of the same sidewall 214 may be comprised of a second material. Similarly, a thin layer may be deposited on the top surface 215 without forming an appreciable portion of the sidewall 214. In one or more embodiments, the bottom 216 may be comprised of a different material than the sidewall 214. In one or more embodiments, the material on the bottom 216 comprises silicon (Si). In one or more embodiments, the sidewall 214 comprises a dielectric material. The dielectric material may be any suitable dielectric material known to the skilled artisan.
- 10 [0036] In one or more embodiments, the opening width 202 of the opening 212 is less than or equal to about 50 nm, less than or equal to about 30 nm, less than or equal to about 20 nm, less than or equal to about 10 nm, or less than or equal to about 7 nm. In one or more embodiments, the opening width 202 is in a range of about 8 nm to about 20 nm.
- 15 [0037] In one or more embodiments, the feature depth D of the feature 210 is greater than or equal to about 5 nm, greater than or equal to about 10 nm, greater than or equal to about 20 nm, greater than or equal to about 50 nm, greater than or equal to about 60 nm, greater than or equal to about 75 nm, greater than or equal to about 100 nm, greater than or equal to about 200 nm, greater than or equal to about 20
300 nm, greater than or equal to about 400 nm, or greater than or equal to about 450 nm. In one or more embodiments, the feature depth D is in a range of about 5 nm to about 500 nm. In one or more embodiments, the feature depth D is in a range of about 10 nm to about 300 nm. In one or more embodiments, the feature depth D is in a range of about 60 nm to about 100 nm.
- 25 [0038] As used herein, the term "feature" means any intentional surface irregularity. Suitable examples of features include but are not limited to trenches or vias which have a top, two sidewalls and a bottom, peaks which have a top and two sidewalls. Features can have any suitable aspect ratio (ratio of the depth of the feature to the width of the feature). In one or more embodiments, the aspect ratio of the at least
30 one feature 210 is greater than or equal to about 5:1, 10:1, 15:1, 20:1, 25:1, 30:1, 35:1, or 40:1.

[0039] For simplicity, reference will be made to parts of the feature 210 illustrated in FIG. 2 while referring to FIGS. 3-8C. For example, the device 200 shown in FIG. 3 will be referred to as having a bottom 216. For clarity of the illustrations provided, the reference numerals of the parts of feature 210 are not shown in FIGS. 3-8C.

5 [0040] Referring to FIG. 1 and FIGS. 2-8C, in one or more embodiments, the method 100 begins with optional operation 105 to pre-treat the substrate. The pre-treatment at operation 105 can be any suitable pre-treatment known to the skilled artisan. Suitable pre-treatments include, but are not limited to, pre-heating, cleaning, soaking, native oxide removal, or deposition of a contact layer (e.g., titanium silicide
10 (TiSi)), or capping layers (e.g., TiSiN). In one or more embodiments, a layer such as titanium silicide or titanium silicon nitride (TiSiN), or other metal silicide is deposited at operation 105 to form a silicide contact.

[0041] The skilled artisan will recognize that the disclosed processes are not limited to the silicide contact and liner/gap fill applications. Generally, front-end of line (FEOL)
15 refers to the first portion of integrated circuit fabrication, including transistor fabrication, middle of line (MOL) connects the transistor and interconnect parts of a chip using a series of contact structures, and back-end of line (BEOL) refers to a series of process steps after transistor fabrication through completion of a wafer. One or more embodiments of the disclosure are directed to methods of forming devices
20 that are useful for one or more FEOL, MOL, and/or BEOL processes known to the skilled artisan.

[0042] An exemplary device 200 is shown in FIG. 3 after optional operation 105. The device 200 comprises a bottom formed from the at least one feature 210 and sidewalls and a top surface formed from layer 220. In one or more embodiments, the
25 at least one feature 210 comprises a conductive material and layer 220 comprises a dielectric. Those skilled in the art will recognize that the disclosed processes may be performed on different materials and/or that the illustrated layers may be arranged in different ways.

[0043] The method 100 continues with cycle 110. The cycle 110 forms a first silicon
30 (Si) layer 240 at the bottom 216 of at least one feature 210 of the device 200. The cycle 110 includes a series of operations which are each performed in sequence and may be repeated. Some of the operations are optional within each cycle. A given

optional operation may be performed during each cycle, periodically (every other, every fifth, or every hundredth cycle), as needed based on predetermined parameters, or even not at all.

5 [0044] As shown in FIG. 3, the cycle 110 begins with operation 112. At operation 112, a first silicon (Si) layer 240 is deposited on the substrate surface 205 of the device 200. The first silicon (Si) layer 240 has a bottom thickness on the bottom 216 and a top thickness on the top surface 215 and/or a sidewall thickness on the sidewall 214. In some embodiments, the first silicon (Si) layer 240 forms on the bottom of the at least one feature 210.

10 [0045] The first silicon (Si) layer 240 may be deposited by any suitable method. In one or more embodiments, the first silicon (Si) layer 240 may be deposited by physical vapor deposition (PVD). In these embodiments, as shown in FIG. 3, the sidewall thickness is less than the top thickness and the bottom thickness. In one or more embodiments, the top thickness is greater than the bottom thickness.

15 [0046] Those skilled in the art will recognize that the disclosed methods may begin with a first silicon (Si) layer 240 already formed on the substrate surface 205 of the device 200, and the device 200 is then provided. As used in this specification and the appended claims, the term "provided" means that the substrate is made available for processing (e.g., positioned in a processing chamber).

20 [0047] The cycle 110 continues with operation 114. As shown in FIG. 4, at operation 114, a flowable polymer film 250 is formed on the first silicon (Si) layer 240 within the feature 210 of the device 200. The polymer film 250 has a polymer thickness less than or equal to the feature depth D. Stated differently, as a flowable film (described below), the polymer film is contained entirely within the feature 210 and
25 is not present on the top surface 215 of the device 200. Accordingly, in this regard, the polymer may be described as having a "thickness" or may interchangeably be described as having a "depth." Stated differently, the polymer "thickness" is measured in a Z-direction within the feature 210 of the device 200, such that the thickness/depth is less than or equal to feature depth D. In one or more embodiments, the polymer film 250
30 has a thickness in a range of about 1 nm to about 50 nm, or in a range of about 1 nm to 10 nm, or in a range of about 2 nm to about 5 nm. In some embodiments, the thickness of the polymer film 250 is in a range of from 1% to 99%, or in a range of

from 1% to 80%, or in a range of from 2% to 20% of the depth D of the at least one feature 210.

[0048] In the disclosed methods, processing parameters and reactants may be selected to limit conformality of deposited materials, which may allow the deposited material to better fill features on the substrate. A flowable material is one which, under the proper conditions, will flow by gravity to the low point of a substrate surface and/or by capillary action to narrow CD spaces of trenches or other features.

[0049] In one or more embodiments, forming the polymer film comprises exposing the surface to one or more monomers.

[0050] In some embodiments, the one or more monomers comprise, consist essentially of, or consist of a single monomer selected from the group consisting of a methyl group, a methacrylate group, a styrene group, a benzyl alcohol group, a benzyl chloride group, an aldehyde group, and an amine group. In some embodiments, the one or more monomers consist of a single monomer selected from the group consisting of a methyl group, a methacrylate group, a styrene group, a benzyl alcohol group, a benzyl chloride group, an aldehyde group, and an amine group.

[0051] In one or more embodiments, the monomers comprise, consist essentially of, or consist of a single, bi-functional monomer, with each functional group in the bi-functional monomer being different. In this way, one functional group of a monomer molecule will react with the other functional group of a different monomer molecule. Those skilled in the art may recognize this as an "A" polymer.

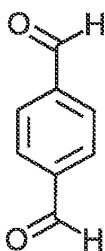
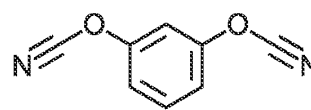
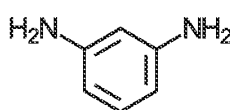
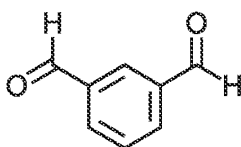
[0052] In one or more embodiments, the one or more monomers comprise, consist essentially of, or consist of one or more of amines with bi-functional groups, aldehydes with bi-functional groups, ketones with bi-functional groups, and alcohols with bi-functional groups.

[0053] In one or more embodiments, the amines have a formula of $\text{H}_2\text{N}-(\text{CH}_x)_n-\text{NH}_2$, where n is an integer in a range of from 1 to 20 and x is 1 or 2. In one or more embodiments, the aldehydes have a formula of $\text{OHC}-(\text{CH}_x)_m-\text{CHO}$, where m is an integer in a range of from 2 to 20 and x is 1 or 2. In one or more embodiments, the ketones have a formula of $\text{ROC}-(\text{CH}_x)_q-\text{COR}$, where q is an integer in a range of from 2 to 20, x is 1 or 2, and R is an alkyl group. In one or more embodiments, each R in the formula $\text{ROC}-(\text{CH}_x)_q-\text{COR}$ is the same alkyl group. In one or more embodiments,

each R in the formula $\text{ROC}-(\text{CH}_x)_q-\text{COR}$ is a different alkyl group. In one or more embodiments, the alcohols have a formula of $\text{HOC}-(\text{CH}_x)_r-\text{COH}$, where r is an integer in a range of from 2 to 20 and x is 1 or 2.

[0054] In one or more embodiments, the amines, the aldehydes, the ketones, and the alcohols comprise carbon atoms. In one or more embodiments, the monomers described herein may be linear, branched, cyclic, saturated, or unsaturated. The monomers described herein do not contain groups which are reactive in the chemical polymerization process described herein.

[0055] In specific embodiments, the monomers may be selected from one or more of:



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[0056] In one or more embodiments, the monomers comprise, consist essentially of, or consist of two monomers, such as two bi-functional monomers, each functional group being the same. In this way the functional groups of one monomer react with the functional groups of a second monomer. Those skilled in the art may recognize this as an "AB" polymer.

[0057] In one or more embodiments, the one or more monomers comprise, consist essentially of, or consist of three monomers, wherein two of the monomers independently comprise one or more of an amine with a single functional group, an

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aldehyde with a single functional group, a ketone with a single functional group, or an alcohol with a single functional group, and at least one of the monomers is independently selected from the group consisting of amines with bi-functional groups, aldehydes with bi-functional groups, ketones with bi-functional groups, and alcohols with bi-functional groups. Those skilled in the art may recognize this as an "ABC" polymer.

[0058] In one or more embodiments, the flexible monomers used for producing the selective protection polymer film 250 are capable of forming oligomers in a higher percentage during polymerization compared with stiff monomers. Thus, in one or more embodiments, the polymerization process is through monomer, oligomer, and polymer stages. The polymer formation depends on its local concentration of monomers. In one or more embodiments, A and B monomers are used, which can only bond between A and B, not between A's or B's. Therefore, during the purge and pumping stage, the A concentration is greatly reduced, especially on the field/wall areas 214, 215. In this case, when B monomers come in, it only forms oligomers on the field/wall areas 214, 215 with very low concentration of A monomer. Due to pumping and purge efficiency difference between field/wall 214, 215 and bottom 216 of the feature 210, the A monomer concentration in the bottom 216 of the feature 210 is higher compared with the concentration on the field/wall 214, 215. Since A monomer concentration is higher at the bottom 216 of the feature 210, it forms higher molecular number oligomer or polymer with incoming B monomers. These oligomers and polymers will continually grow with process cycles at bottom 216 of the feature 210. In one or more embodiments, a lower molecular weight B monomer is used, when it forms B-A-B oligomer on field/wall 214, 215 with low concentration of A, it is still volatile compared with higher oligomers formed at bottom 216 of the feature 210, B-A-B-A-B, etc., which decreases the amount of polymer residue on field/wall 214, 215 as much as possible.

[0059] A benzene ring has an electrical advantage to activate the aldehyde functional group during bonding with amine. When two aldehyde groups are in the 1,4 positions of a benzene ring, the monomer is a stiff or rigid monomer. When the monomer reacts with 1,4-diaminobenzene, it forms a stiff polymer with a rough surface in the feature.

[0060] Accordingly, in one or more embodiments, if two aldehyde groups are in the 1,3 positions of benzene, which is a flexible monomer, a flexible polymer film 250 with is formed. The flexible polymer film 250 has a lower glass transition temperature compared with a film formed from a stiff polymer. Thus, in one or more embodiments, a polymer film 250 is advantageously formed having a smooth polymer surface, flexibility, and a lower glass transition temperature (T_g), especially when the T_g is below the process temperature.

[0061] In one or more embodiments, when a flexible monomer is used, the opportunity to form oligomers, such as ABAB or ABABAB, is increased. Flexible monomers also make possible a smooth surface in the feature 210 with easy packing and packing density. Flexible monomers also reduce polymer residue on field/wall 214, 215 area due to the oligomers' volatility and flowability into the feature. By this improvement, the residue of polymer on field 215 and on the sidewall 214 is eliminated, enhancing process efficiency. In one or more embodiments, the semiconductor device quality is improved when there is substantially no residue or no residue on the field 215 and wall 214 areas.

[0062] Without intending to be bound by theory, it is thought that the polymer that is formed and deposited as the polymer film 250 has the flexibility to fill the bottom 216 of the feature 210. In one or more embodiments, the polymer has liquidity during deposition and further processing.

[0063] As stated previously, the polymer film 250 is flowable. In order to control the "flowability" of the resulting polymer film 250, it has been found that it is necessary to control the size of the resulting oligomers.

[0064] Accordingly, in one or more embodiments, the formation of the polymer film 250 is performed on a substrate maintained at a temperature in a range of 0 °C to 400 °C. In some embodiments, the substrate is maintained at a temperature in a range of 30 °C to 400 °C.

[0065] Further, other process parameters may be controlled during the formation of the polymer film 250. Examples of parameters which may be controlled include, but are not limited to processing chamber pressure, monomer selections, the use of an inert diluent or carrier gas, partial pressures of monomers, pulse sequence of monomers, and pause periods to permit flow of the polymer material.

[0066] After forming the flowable polymer film 250 at operation 114, the cycle 110 continues with operation 116. As shown in FIG. 5, at operation 116, at least a portion of the first silicon (Si) layer 240 is selectively removed. The first silicon (Si) layer 240 is removed from the top surface 215 without substantially affecting any material
5 beneath the polymer film 250. As used in this regard, a process which does not “substantially affect” material layers does not cause any decrease in volume, thickness, or composition. One skilled in the art will recognize that the polymer film 250 is acting as an etch stop layer during the removal of a portion of the first silicon (Si) layer 240.

10 [0067] In one or more embodiments, operation 116 also removes a portion of the first silicon (Si) layer 240 from the sidewall 214. In one or more embodiments, any portion of the first silicon (Si) layer 240 which is present on sidewall 214 below the upper surface of the polymer film 250 may remain intact without being removed.

[0068] In one or more embodiments, the selective removal of the portion of the first
15 silicon (Si) layer at operation 116 is performed on a substrate maintained at a temperature in a range of 100 °C to 400 °C.

[0069] In one or more embodiments, the selective removal of the first silicon (Si) layer 240 is performed by exposing the substrate surface 205 to a fluorine-based plasma or a chlorine-based plasma. Any suitable fluorine-based plasma or chlorine-
20 based plasma known to the skilled artisan that selectively removes the first silicon (Si) layer 240 may be used.

[0070] In one or more embodiments, the selective removal of the first silicon (Si) layer 240 at operation 116 is performed by exposing the substrate surface 205 of device 200 to NF_3 radicals. In one or more embodiments, the substrate is maintained
25 at a temperature in a range of 80 °C to 150 °C.

[0071] In one or more embodiments, the selective removal of the first silicon (Si) layer 240 at operation 116 is performed by exposing the substrate surface 205 of device 200 to a chlorine-containing gas or an alkylchloride gas. In some
30 embodiments, the alkylchloride gas includes, but is not limited to, methylchloride, 2-chloropropane, or 1,2-dichloroethane. In one or more embodiments, the substrate is maintained at a temperature in a range of 80 °C to 150 °C.

[0072] The cycle 110 continues with operation 118. As shown in FIG. 6, at operation 118, the polymer film 250 is removed to expose the remaining portion of the first silicon (Si) layer 240, e.g., the portion of the first silicon (Si) layer on the bottom 216 beneath the polymer film 250. In one or more embodiments, the removal
5 of the polymer film 250 is complete and leaves substantially no residue or no residue.

[0073] In one or more embodiments, the polymer film 250 is removed by exposing the substrate surface 205 of the device 200 to a hydrogen (H₂) plasma treatment. In one or more embodiments, the polymer film 250 is removed by exposure to a thermal O₂ environment at an elevated temperature.

10 [0074] In one or more embodiments, the removal of the polymer film 250 is performed by exposing the substrate surface 205 of device 200 to one or more of a thermal process or a hydrogen (H₂) plasma treatment. In one or more embodiments, after removing the first silicon (Si) layer 240 from the top surface 215 and sidewall 214, the polymer film 250 can be removed thermally by heating it to 350 °C to 500 °C
15 under vacuum. In other embodiments, after removing the first silicon (Si) layer 240 from the top surface 215 and sidewall 214, the polymer film 250 may also be removed by hydrogen (H₂) plasma at temperature in a range of from 100 °C to 300 °C for a time period in a range of from 2 seconds to 30 seconds.

[0075] In one or more embodiments, the removal of the polymer film 250 at
20 operation 118 comprises a first step including exposing the substrate surface to hydrogen (H₂) plasma and oxygen (O₂) plasma and a second step including exposing the substrate surface to hydrogen (H₂) plasma only.

[0076] The first step may be performed at a chamber pressure in a range of from about 1 Torr to about 10 Torr, for example, about 5 Torr, at a flow rate of the hydrogen
25 (H₂) plasma in a range of from about 1000 sccm to about 10000 sccm, for example, 6000 sccm and a flow rate of the oxygen (O₂) in a range of from about 100 sccm to about 1000 sccm, for example, 300 sccm.

[0077] The second step may be performed at a chamber pressure in a range of from about 10 Torr to about 50 Torr, for example, about 20 Torr, at a flow rate of the
30 hydrogen (H₂) plasma in a range of from about 10 sccm to about 10000 sccm.

[0078] The polymer removal process of operation 118 may be performed in a processing chamber, such as a Volta® CVD/ALD chamber available from Applied Materials of Santa Clara, Calif.

[0079] After removing the polymer film 250, at operation 118 shown in FIG. 6, the cycle 110 optionally continues with operation 119. At operation 119, the remaining portion of the first silicon (Si) layer 240 is oxidized to form a first silicon oxide (SiO_x) layer on the bottom 216. In one or more embodiments, oxidizing the remaining portion of the first silicon (Si) layer 240 at operation 119 includes a thermal oxidation process and/or a plasma oxidation process. In one or more embodiments, the thermal oxidation process includes oxidizing the remaining portion of the first silicon (Si) layer 240 in a range of from about 500 °C to about 900 °C in a process chamber or a furnace. In one or more embodiments, the plasma oxidation process includes exposing the remaining portion of the first silicon (Si) layer 240 to an oxygen-containing plasma in a range of from about 200 °C to about 500 °C. The oxygen-containing plasma may include any suitable oxygen-containing plasma known to the skilled artisan.

[0080] In embodiments where the cycle 110, after removing the polymer film 250 at operation 118 shown in FIG. 6, oxidizes the remaining portion of the first silicon (Si) layer 240 to form a first silicon oxide (SiO_x) layer 242 on the bottom 216 (operation 119), the cycle 110 then continues to operation 130 as discussed in further detail below.

[0081] In one or more embodiments, at the end of cycle 110, the surface of the first silicon (Si) layer 240 does not contain any contaminants or residues of the polymer layer 250. Specifically, in one or more embodiments, there are no carbon or oxygen residues on the surface of the first silicon (Si) layer 240. In one or more embodiments, when the method 100 includes repeated cycles 110 (see below), there are no contaminants or residues between amounts of the first silicon (Si) layer 240 deposited in subsequent cycles. In one or more embodiments, when the method 100 includes the deposition of a second silicon (Si) layer 260 (see below), there are no contaminants or residues between the first silicon (Si) layer 240 and the second silicon (Si) layer 260.

[0082] In one or more embodiments, the monomers are selected so as not to contain any oxygen atoms which may oxidize the surface of the first silicon (Si) layer 240 during removal of the polymer layer 250.

[0083] The method 100 continues to decision point 120. At point 120, the substrate is evaluated to determine whether or not the first silicon (Si) layer 240 has reached a predetermined thickness or a predetermined number of cycles 110 have been performed. If the conditions are met, the method 100 continues to operation 130. If the conditions are not met, the method 100 returns to the beginning of cycle 110 with operation 112. In those embodiments in which the cycle 110 is repeated to form additional material, those skilled in the art will appreciate that operation 112 is often performed to deposit the requisite additional metal material (e.g., silicon (Si)). In one or more embodiments, the predetermined thickness is in a range of about 2 nm to about 10 nm.

[0084] In one or more unillustrated embodiments, the first silicon (Si) layer 240 may be optionally etched. In one or more embodiments, the first silicon (Si) layer 240 is etched to remove the portions of the first silicon (Si) layer 240 which extend up the sidewall 214. When etched, the first silicon (Si) layer 240 is also thinned on the bottom 216 of the feature 210. Accordingly, one skilled in the art will recognize that the first silicon (Si) layer 240 may be deposited to a greater bottom thickness than desired in a final product to provide for sacrificial material which will be removed when etching the metal material from the sidewall 214.

[0085] The method 100 includes optional operation 130. As shown in FIG. 7, in some embodiments, the optional operation 130 occurs after removing the polymer film 250, at operation 118 shown in FIG. 6.

[0086] In FIG. 7, at operation 130, a second silicon (Si) layer 260 is selectively deposited on the first silicon (Si) layer 240. The second silicon (Si) layer 260 may be deposited by any suitable deposition process known to the skilled artisan such that the second silicon (Si) layer 260 forms selectively to the surface of the first silicon (Si) layer 240 over other substrate surface materials (e.g., layer 220). In one or more embodiments, selectively depositing the second silicon (Si) layer 260 comprises chemical vapor deposition (CVD). The selective deposition process provides a gapfill material comprising the second silicon (Si) layer 260 which is formed in a bottom-up

fashion without lateral deposition from the sidewall 214. In one or more embodiments, the second silicon (Si) layer 260 is deposited without forming any voids or seams within the second silicon (Si) layer 260.

[0087] As shown in FIG. 8B, in some embodiments, the optional operation 130 occurs after removing the polymer film 250, at operation 118 shown in FIG. 6, and after the cycle 110 oxidizes the remaining portion of the first silicon (Si) layer 240 to form a first silicon oxide (SiO_x) layer 242 on the bottom 216 (operation 119), the cycle 110 then continues to operation 130. In one or more unillustrated embodiments, a second silicon (Si) layer 260 is selectively deposited on the first silicon oxide (SiO_x) layer 242. While not shown, the skilled artisan will appreciate that the second silicon (Si) layer 260 would be selectively deposited on the first silicon oxide (SiO_x) layer 242 at operation 130, after oxidizing the remaining portion of the first silicon (Si) layer 240 to form the first silicon oxide (SiO_x) layer 242 on the bottom 216 at operation 119, shown in FIG. 8A. In specific embodiments, the deposition process is selective to the surface of the first silicon oxide (SiO_x) layer 242 over other substrate surface materials (e.g., layer 220). The selective deposition process provides a gapfill material comprising the second silicon (Si) layer 260 which is formed in a bottom-up fashion without lateral deposition from the sidewall 214. In one or more embodiments, the second silicon (Si) layer 260 is deposited without forming any voids or seams within the second silicon (Si) layer 260.

[0088] In FIG. 7, at operation 130, a second silicon (Si) layer 260 is selectively deposited on the first silicon (Si) layer 240. The deposition process is selective to the surface of the first silicon (Si) layer 240 over other substrate surface materials (e.g., layer 220). The selective deposition process provides a gapfill material comprising the second silicon (Si) layer 260 which is formed in a bottom-up fashion without lateral deposition from the sidewall 214. In one or more embodiments, the second silicon (Si) layer 260 is deposited without forming any voids or seams within the second silicon (Si) layer 260.

[0089] FIG. 8B illustrates operation 130 of the cycle 110. In FIG. 8B, at operation 130, a second silicon (Si) layer 260 is selectively deposited on the first silicon oxide (SiO_x) layer 242. The second silicon (Si) layer 260 may be deposited by any suitable deposition process known to the skilled artisan such that the second silicon (Si) layer

260 forms selectively to the surface of the first silicon oxide (SiO_x) layer 242 over other substrate surface materials (e.g., layer 220). In one or more embodiments, selectively depositing the second silicon (Si) layer 260 comprises chemical vapor deposition (CVD). The selective deposition process provides a gapfill material comprising the
5 second silicon (Si) layer 260 which is formed in a bottom-up fashion without lateral deposition from the sidewall 214. In one or more embodiments, the second silicon (Si) layer 260 is deposited without forming any voids or seams within the second silicon (Si) layer 260.

[0090] FIG. 8C illustrates operation 119 after selectively depositing the second
10 silicon (Si) layer 260 on the first silicon oxide (SiO_x) layer 242 at operation 130 in FIG. 8B. In one or more embodiments, the selectively second silicon (Si) layer 260 layer is oxidized, at operation 119, to form a second silicon oxide (SiO_x) layer 262 on the first silicon oxide (SiO_x) layer 242. In one or more embodiments, the second silicon oxide (SiO_x) layer is selectively deposited on the first silicon oxide (SiO_x) layer by
15 performing an etching process, and the second silicon oxide (SiO_x) layer forms as a result of the etching process. The etching process may be any suitable etching process known to the skilled artisan.

[0091] The method 100 may end after operation 130 (selectively depositing the second silicon (Si) layer 260) or operation 119 after selectively depositing the second
20 silicon (Si) layer 260 on the first silicon oxide (SiO_x) layer 242 at operation 130 in FIG. 8B, or it may continue with optional post processing at optional operation 140. The optional post-processing operation 140 can be, for example, a process to modify film properties (e.g., annealing or plasma treatment), a further film deposition process (e.g., additional ALD or CVD processes) to grow additional films, or a further etch
25 process to form a desired predetermined device architecture. In one or more embodiments, the optional post-processing operation 140 can be a process that modifies a property of the deposited film. In one or more embodiments, the optional post-processing operation 140 comprises annealing the device 200. In one or more embodiments, annealing is performed at a temperature greater than or equal to about
30 300 °C, greater than or equal to about 400 °C, greater than or equal to about 500 °C, greater than or equal to about 600 °C, greater than or equal to about 700 °C, greater than or equal to about 800 °C, greater than or equal to about 900 °C or greater than or

equal to about 1000 °C. The annealing environment of one or more embodiments comprises one or more of an inert gas (e.g., molecular nitrogen (N₂), argon (Ar)) or a reducing gas (e.g., molecular hydrogen (H₂) or ammonia (NH₃)) or an oxidant, such as, but not limited to, oxygen (O₂), ozone (O₃), or peroxides. Annealing can be performed for any suitable length of time. In one or more embodiments, the substrate is annealed for a predetermined time in the range of about 15 seconds to about 90 minutes, or in the range of about 1 minute to about 60 minutes.

[0092] Additional embodiments of the disclosure are directed to methods of selectively depositing a dielectric material, such as a high-k dielectric material including but not limited to hafnium oxide (HfO_x) or zirconium oxide (ZrO_x). It has been advantageously found that use of a flowable polymer to protect a substrate surface within a feature can be used to selectively deposit a metal material, such as silicon and polysilicon, as well as dielectric materials, such as hafnium oxide (HfO_x) or zirconium oxide (ZrO_x).

[0093] In one or more embodiments, hafnium oxide (HfO_x) may be deposited by the method 100 including cycle 110. In some embodiments, hafnium oxide (HfO_x) is directly deposited on the substrate surface 205 of the device 200 by atomic layer deposition (ALD) or chemical vapor deposition (CVD). After the hafnium oxide (HfO_x) is deposited, the method of selectively depositing the dielectric material includes forming a flowable polymer film on the hafnium oxide (HfO_x) within the at least one feature to protect the hafnium oxide (HfO_x) on the bottom and remove the hafnium oxide (HfO_x) on the field 215 and wall 214. Accordingly, in one or more embodiments, the method 100 of selectively depositing the dielectric material includes: optionally, pre-treating the substrate (operation 105), cycle 110, including depositing a first dielectric layer (e.g., hafnium oxide (HfO_x) or zirconium oxide (ZrO_x)) (operation 112), forming a flowable polymer film (operation 114), selectively removing a portion of the first dielectric layer (operation 116), removing the polymer film (operation 118), decision point (operation 120), optionally, selectively depositing a second dielectric layer (e.g., hafnium oxide (HfO_x) or zirconium oxide (ZrO_x)) on the remaining portion of the first dielectric layer, and optionally, post-processing (operation 140).

[0094] FIG. 9 illustrates a schematic top-view diagram of an example of a multi-chamber processing system 400 according to embodiments of the present disclosure.

The processing system 400 generally includes a factory interface 402, load lock chambers 404, 406, transfer chambers 408, 410 with respective transfer robots 412, 414, holding chambers 416, 418, and processing chambers 420, 422, 424, 426, 428, 430. As detailed herein, wafers in the processing system 400 can be processed in and transferred between the various chambers without exposing the wafers to an ambient environment exterior to the processing system 400 (e.g., an atmospheric ambient environment such as may be present in a fab). For example, the wafers can be processed in and transferred between the various chambers in a low pressure (e.g., less than or equal to about 300 Torr) or vacuum environment without breaking the low pressure or vacuum environment between various processes performed on the wafers in the processing system 400. Accordingly, the processing system 400 may provide for an integrated solution for some processing of wafers.

[0095] Examples of a processing system that may be suitably modified in accordance with the teachings provided herein include the Endura®, Producer® or Centura® integrated processing systems or other suitable processing systems commercially available from Applied Materials, Inc., located in Santa Clara, California. It is contemplated that other processing systems (including those from other manufacturers) may be adapted to benefit from aspects described herein.

[0096] In the illustrated example of FIG. 9, the factory interface 402 includes a docking station 440 and factory interface robots 442 to facilitate transfer of wafers. The docking station 440 is configured to accept one or more front opening unified pods (FOUPs) 444. In some examples, each factory interface robot 442 generally comprises a blade 448 disposed on one end of the respective factory interface robot 442 configured to transfer the wafers from the factory interface 402 to the load lock chambers 404, 406.

[0097] The load lock chambers 404, 406 have respective ports 450, 452 coupled to the factory interface 402 and respective ports 454, 456 coupled to the transfer chamber 408. The transfer chamber 408 further has respective ports 458, 460 coupled to the holding chambers 416, 418 and respective ports 462, 464 coupled to processing chambers 420, 422. Similarly, the transfer chamber 410 has respective ports 466, 468 coupled to the holding chambers 416, 418 and respective ports 470, 472, 474, 476 coupled to processing chambers 424, 426, 428, 430. The ports 454,

456, 458, 460, 462, 464, 466, 468, 470, 472, 474, 476 can be, for example, slit valve openings with slit valves for passing wafers therethrough by the transfer robots 412, 414 and for providing a seal between respective chambers to prevent a gas from passing between the respective chambers. Generally, any port is open for transferring
5 a wafer therethrough. Otherwise, the port is closed.

[0098] The load lock chambers 404, 406, transfer chambers 408, 410, holding chambers 416, 418, and processing chambers 420, 422, 424, 426, 428, 430 may be fluidly coupled to a gas and pressure control system (not specifically illustrated). The gas and pressure control system can include one or more gas pumps (e.g., turbo
10 pumps, cryo-pumps, roughing pumps), gas sources, various valves, and conduits fluidly coupled to the various chambers. In operation, a factory interface robot 442 transfers a wafer from a FOUP 444 through a port 450 or 452 to a load lock chamber 404 or 406. The gas and pressure control system then pumps down the load lock chamber 404 or 406. The gas and pressure control system further maintains the
15 transfer chambers 408, 410 and holding chambers 416, 418 with an interior low pressure or vacuum environment (which may include an inert gas). Hence, the pumping down of the load lock chamber 404 or 406 facilitates passing the wafer between, for example, the atmospheric environment of the factory interface 402 and the low pressure or vacuum environment of the transfer chamber 408.

20 [0099] With the wafer in the load lock chamber 404 or 406 that has been pumped down, the transfer robot 412 transfers the wafer from the load lock chamber 404 or 406 into the transfer chamber 408 through the port 454 or 456. The transfer robot 412 is then capable of transferring the wafer to and/or between any of the processing chambers 420, 422 through the respective ports 462, 464 for processing and the
25 holding chambers 416, 418 through the respective ports 458, 460 for holding to await further transfer. Similarly, the transfer robot 414 is capable of accessing the wafer in the holding chamber 416 or 418 through the port 466 or 468 and is capable of transferring the wafer to and/or between any of the processing chambers 424, 426, 428, 430 through the respective ports 470, 472, 474, 476 for processing and the
30 holding chambers 416, 418 through the respective ports 466, 468 for holding to await further transfer. The transfer and holding of the wafer within and among the various

chambers can be in the low pressure or vacuum environment provided by the gas and pressure control system.

[00100] The processing chambers 420, 422, 424, 426, 428, 430 can be any appropriate chamber for processing a wafer. In some embodiments, the processing chamber 420 can be capable of performing an annealing process, the processing chamber 422 can be capable of performing a cleaning process, and the processing chambers 424, 426, 428, 430 can be capable of performing epitaxial growth processes. In some examples, the processing chamber 422 can be capable of performing a cleaning process, the processing chamber 420 can be capable of performing an etch process, and the processing chambers 424, 426, 428, 430 can be capable of performing respective epitaxial growth processes. The processing chamber 422 may be a SiCoNi™ Preclean chamber available from Applied Materials of Santa Clara, Calif. The processing chamber 420 may be a Selectra™ Etch chamber available from Applied Materials of Santa Clara, Calif. The processing chamber 422 may be a Volta® CVD/ALD chamber available from Applied Materials of Santa Clara, Calif.

[00101] A system controller 490 is coupled to the processing system 400 for controlling the processing system 400 or components thereof. For example, the system controller 490 may control the operation of the processing system 400 using a direct control of the chambers 404, 406, 408, 416, 418, 410, 420, 422, 424, 426, 428, 430 of the processing system 400 or by controlling controllers associated with the chambers 404, 406, 408, 416, 418, 410, 420, 422, 424, 426, 428, 430. In operation, the system controller 490 enables data collection and feedback from the respective chambers to coordinate performance of the processing system 400.

[00102] The system controller 490 generally includes a central processing unit (CPU) 492, memory 494, and support circuits 496. The CPU 492 may be one of any form of a general-purpose processor that can be used in an industrial setting. The memory 494, or non-transitory computer-readable medium, is accessible by the CPU 492 and may be one or more of memory such as random-access memory (RAM), read only memory (ROM), floppy disk, hard disk, or any other form of digital storage, local or remote. The support circuits 496 are coupled to the CPU 492 and may comprise cache, clock circuits, input/output subsystems, power supplies, and the like. The

various methods disclosed herein may generally be implemented under the control of the CPU 492 by the CPU 492 executing computer instruction code stored in the memory 494 (or in memory of a particular process chamber) as, for example, a software routine. When the computer instruction code is executed by the CPU 492, the CPU 492 controls the chambers to perform processes in accordance with the various methods.

[00103] Other processing systems can be in other configurations. For example, more or fewer processing chambers may be coupled to a transfer apparatus. In the illustrated example, the transfer apparatus includes the transfer chambers 408, 410 and the holding chambers 416, 418. In other examples, more or fewer transfer chambers (*e.g.*, one transfer chamber) and/or more or fewer holding chambers (*e.g.*, no holding chambers) may be implemented as a transfer apparatus in a processing system.

[00104] Processes may generally be stored in the memory of the system controller 1190 as a software routine that, when executed by the processor, causes the process chamber to perform processes of the present disclosure. The software routine may also be stored and/or executed by a second processor (not shown) that is remotely located from the hardware being controlled by the processor. Some or all of the methods of the present disclosure may also be performed in hardware. As such, the process may be implemented in software and executed using a computer system, in hardware as, *e.g.*, an application specific integrated circuit or other type of hardware implementation, or as a combination of software and hardware. The software routine, when executed by the processor, transforms the general-purpose computer into a specific purpose computer (controller) that controls the chamber operation such that the processes are performed.

[00105] Embodiments of the disclosure are directed to a non-transitory computer readable medium. In one or more embodiments, the non-transitory computer readable medium includes instructions that, when executed by a controller of a processing chamber, causes a processing chamber to perform the operations of any of the methods (*e.g.*, method 100) described herein.

[00106] Spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or

feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as "below," or "beneath" other elements or features would then be oriented "above" the other elements or features. Thus, the exemplary term "below" may encompass both an orientation of above and below. The device may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein interpreted accordingly.

10 [00107] The use of the terms "a" and "an" and "the" and similar referents in the context of describing the materials and methods discussed herein (especially in the context of the following claims) are to be construed to cover both the singular and the plural, unless otherwise indicated herein or clearly contradicted by context. Recitation of ranges of values herein are merely intended to serve as a shorthand method of referring individually to each separate value falling within the range, unless otherwise indicated herein, and each separate value is incorporated into the specification as if it were individually recited herein. All methods described herein can be performed in any suitable order unless otherwise indicated herein or otherwise clearly contradicted by context. The use of any and all examples, or exemplary language (e.g., "such as")
15 provided herein, is intended merely to better illuminate the materials and methods and does not pose a limitation on the scope unless otherwise claimed. No language in the specification should be construed as indicating any non-claimed element as essential to the practice of the disclosed materials and methods.

[00108] Reference throughout this specification to "one embodiment," "certain embodiments," "one or more embodiments" or "an embodiment" means that a particular feature, structure, material, or characteristic described in connection with the embodiment is included in at least one embodiment of the disclosure. Thus, the appearances of the phrases such as "in one or more embodiments," "in certain embodiments," "in one embodiment" or "in an embodiment" in various places
25 throughout this specification are not necessarily referring to the same embodiment of the disclosure. In one or more embodiments, the particular features, structures, materials, or characteristics are combined in any suitable manner.

[00109] Although the disclosure herein has been described with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present disclosure. It will be apparent to those skilled in the art that various modifications and variations can be made to the method and apparatus of the present disclosure without departing from the spirit and scope of the disclosure. Thus, it is intended that the present disclosure include modifications and variations that are within the scope of the appended claims and their equivalents.

What is claimed is:

1. A method of selectively depositing polysilicon, the method comprising:
depositing a first silicon (Si) layer by physical vapor deposition (PVD) on
5 a semiconductor substrate surface with at least one feature formed thereon, the
at least one feature having at least one opening at a top surface with an
opening width, at least one sidewall, and a bottom, the at least one feature
extending a feature depth from the top surface to the bottom, the first silicon
(Si) layer forming on the top surface, along the at least one sidewall, and the
10 bottom;
forming a flowable polymer film on the first silicon (Si) layer within the at
least one feature, the flowable polymer film forming on the first silicon (Si) layer
on the bottom and having a polymer depth less than or equal to the feature
depth;
15 selectively removing at least a portion of the first silicon (Si) layer from
the top surface and the at least one sidewall; and
removing the flowable polymer film to expose the first silicon (Si) layer
on the bottom of the at least one feature.
- 20 2. The method of claim 1, comprising forming the flowable polymer film at a
temperature in a range of from 30 °C to 400 °C.
3. The method of claim 1, wherein forming the flowable polymer film comprises
exposing the semiconductor substrate surface to one or more monomers.
- 25 4. The method of claim 3, wherein the one or more monomers includes a single
monomer selected from the group consisting of a methyl group, a methacrylate
group, a styrene group, a benzyl alcohol group, a benzyl chloride group, and an
aldehyde group.
- 30 5. The method of claim 3, wherein the one or more monomers includes two
monomers, each monomer independently selected from the group consisting of

amines with bi-functional groups, aldehydes with bi-functional groups, ketones with bi-functional groups, and alcohols with bi-functional groups.

- 5 6. The method of claim 5, wherein the one or more monomers includes three monomers, wherein two of the monomers independently comprise one or more of an amine with a single functional group, an aldehyde with a single functional group, a ketone with a single functional group, or an alcohol with a single functional group, and at least one of the monomers is independently selected from the group consisting of amines with bi-functional groups, aldehydes with
10 bi-functional groups, ketones with bi-functional groups, and alcohols with bi-functional groups.
- 15 7. The method of claim 1, comprising selectively removing the portion of the first silicon (Si) layer at a temperature in a range of from 100 °C to 400 °C.
8. The method of claim 7, wherein selectively removing the portion of the first silicon (Si) layer includes exposing the semiconductor substrate surface to a fluorine-based plasma or a chlorine-based plasma.
- 20 9. The method of claim 1, wherein the flowable polymer film is removed by exposing the semiconductor substrate surface to one or more of a thermal process or a hydrogen (H₂) plasma treatment.
- 25 10. The method of claim 9, wherein the flowable polymer film is removed without substantially affecting any material beneath the flowable polymer film.
- 30 11. The method of claim 1, comprising repeating the operations of: forming a flowable polymer film on the first silicon (Si) layer, selectively removing at least a portion of the first silicon (Si) layer from the top surface and the at least one sidewall, and removing the flowable polymer film.

12. The method of claim 1, wherein the feature depth is in a range of about 10 nm to about 300 nm.
13. The method of claim 1, wherein the polymer depth is in a range of about 1 nm to about 50 nm.
14. A method of selectively depositing polysilicon, the method comprising:
depositing a first silicon (Si) layer by physical vapor deposition (PVD) on a semiconductor substrate surface with at least one feature formed thereon, the at least one feature having at least one opening at a top surface with an opening width, at least one sidewall, and a bottom, the at least one feature extending a feature depth from the top surface to the bottom, the first silicon (Si) layer forming on the top surface, along the at least one sidewall, and the bottom;
forming a flowable polymer film on the first silicon (Si) layer within the at least one feature, the flowable polymer film forming on the first silicon (Si) layer on the bottom and having a polymer depth less than or equal to the feature depth;
selectively removing at least a portion of the first silicon (Si) layer from the top surface and the at least one sidewall without substantially affecting any material beneath the flowable polymer film;
removing the flowable polymer film to expose the first silicon (Si) layer on the bottom; and
oxidizing the remaining portion of the first silicon (Si) layer to form a first silicon oxide (SiO_x) layer on the bottom.
15. The method of claim 14, wherein forming the flowable polymer film comprises exposing the semiconductor substrate surface to one or more monomers.
16. The method of claim 14, wherein the flowable polymer film is removed by exposing the semiconductor substrate surface to one or more of a thermal process or a hydrogen (H₂) plasma treatment.

17. The method of claim 16, wherein the flowable polymer film is removed without substantially affecting any material beneath the flowable polymer film.
- 5 18. The method of claim 14, comprising repeating the operations of: forming the flowable polymer film on the first silicon (Si) layer, selectively removing at least a portion of the first silicon (Si) layer from the top surface and the at least one sidewall, removing the flowable polymer film, and oxidizing the remaining portion of first silicon (Si) layer.
- 10 19. The method of claim 14, further comprising selectively depositing a second silicon (Si) layer on the first silicon oxide (SiOx) layer to fill the feature depth after removing the flowable polymer film.
- 15 20. The method of claim 19, further comprising oxidizing the second silicon (Si) layer to form a second silicon oxide (SiOx) layer.