FILM FORMING METHOD

TECHNICAL FIELD

The present invention relates to a film forming method.

BACKGROUND ART

A switch element for a pixel of a large display uses a low temperature polysilicon (hereinafter simply referred to as low temperature p-Si), which has high electron mobility, in an active layer of a thin film transistor (TFT) to increase the response speed. To form a gate insulation film, which is stacked on low temperature p-Si, PECVD (Plasma Enhanced Chemical Vapor Deposition) is known in the prior art as a process using an organic silane compound, for example, tetraethoxysilane (TEOS) as a raw material (e.g., patent document 1).

The PECVD process uses a vacuum chamber, which is connected to a gas supply system and an exhaust system, and supplies a gas mixture containing organic silane compound and oxidation gas into the vacuum chamber from the gas supply system. In the vacuum chamber, a substrate is arranged on one electrode and high frequency power is supplied to another electrode to generate plasma between the electrodes and thereby form an insulative film on the substrate. The organic silane compound is activated in plasma. Thus, an insulative film may be evenly formed on the large substrate surface even when the temperature of the substrate is relatively low.

As the resolution becomes higher for a large display,

various electrical characteristics become necessary for the gate insulative film, such as low leakage current, high breakdown resistance to pressure, low fixed charge density, and low interface state density. Patent document 2 includes a high frequency power supply and a pulse power supply, in which the high frequency power applied to an electrode is repeatedly stopped for by a predetermined period. In the plasma generated between the electrodes, the lifespan of a radical is several milliseconds to several tens of milliseconds, and the lifespan of an ion is several microseconds to several tens of microseconds. Thus, ions disappear in the OFF period of the high frequency power, and the insulative film grows under a high radical concentration. Patent document 2 alternately arranges the period in which ions apply impact to the insulative film and the period in which the insulative film grows without receiving impact from the ions. This reduces damage on the insulative film caused by plasma and improves the electrical characteristics of the insulative film.

Patent Document 1: Japanese Laid-Open Patent Publication No. 8-279505

Patent Document 2: Japanese Laid-Open Patent Publication No. 2001-110798

DISCLOSURE OF THE INVENTION

Generally, a laser annealing process that irradiates amorphous silicon (hereinafter simply referred to as a-Si) with an excimer laser is used as a technique for forming low temperature p-Si. In the laser annealing process, the crystal growth of a low temperature p-Si is promoted in the planar direction of a substrate to fabricate a large-

diameter p-Si. For example, in the laser annealing process, the intensity of the laser is spatially modulated in the planar direction of the substrate or laser scanning is performed in the planar direction of the substrate. Thus, the crystals of the p-Si are grown from a location at which the intensity is low to a location at which the intensity is high, that is, along the planar direction of the substrate.

When performing the laser annealing process on a-Si, the density of the low temperature p-Si is lower than the density of the a-Si. This increases the volume of the film that has undergone the annealing. Thus, when growing the p-Si using the laser annealing process, valleys and ridges are formed in the surface of the p-Si in accordance with the time difference of crystallization between different positions. The valleys and ridges in the surface of the p-Si cause the problems that will now be described in subsequent steps, in particular, in the formation step of the gate insulative film.

When ridges are formed in the surface of the low temperature p-Si, the thickness of the gate insulative film must be entirely increased to ensure that there is sufficient distance between the peaks of the ridges and the lower surface of the gate electrode. This greatly obstructs thickness reduction of the gate insulative film. As a result, with a TFT using the low temperature p-Si, it is difficult to sufficiently improve the electrical characteristics of the TFT even with designs for increasing the current drive capability of the TFT, such as for improving the quality of the low temperature p-Si or shortening the gate length.

The present invention provides a film formation method allowing for the gate insulative film to be thinner by suppressing the deterioration in the electrical characteristics of the gate insulative film and increasing the surface coating rate of the gate insulative film.

MEANS FOR SOLVING THE PROBLEM

A first aspect of the present invention is a film formation method for forming a silicon insulative film on a substrate arranged in a vacuum chamber. The method includes supplying the vacuum chamber with a gas mixture containing an organic silane compound and an oxidation gas, generating a pulsed high frequency power to intermittently supply a high frequency power, and forming the silicon insulative film on the substrate by plasmatizing the gas mixture with the pulsed high frequency power. Said generating a pulsed high frequency power includes generating the pulsed high frequency power with the largest duty ratio that satisfies a target value of a surface coating rate of the silicon insulative film.

A second aspect of the present invention is a film formation method for forming a silicon insulative film on a substrate arranged in a vacuum chamber. The method includes supplying the vacuum chamber with a gas mixture containing an organic silane compound and an oxidation gas, generating a pulsed high frequency power to intermittently supply a high frequency power, and forming the silicon insulative film on the substrate by plasmatizing the gas mixture with the pulsed high frequency power. Said generating a pulsed high frequency power includes generating the pulsed high frequency power with a duty ratio that maintains a flat band

voltage of the silicon insulative film within a predetermined voltage range and satisfies a target value of a surface coating rate of the silicon insulative film.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic cross-sectional view showing a film formation device;

Fig. 2 is a cross-sectional view showing a dummy pattern; and

Figs. 3A and 3B are diagrams respectively showing the dependency of the duty ratio on the flat band voltage and the dependency of the duty ratio on the surface coating rate.

DESCRIPTION OF REFERENCE CHARACTERS

T1: ON period, T2: OFF period, 10: film formation device, 11: vacuum chamber, 14: power supply unit, 15: high frequency power supply, 16: pulse power supply.

BEST MODE FOR CARRYING OUT THE INVENTION

A film formation method according to one embodiment of the present invention will now be discussed with reference to the drawings. Fig. 1 is a schematic cross-sectional view showing a film formation device 10 used in the film formation method of the present invention. The broken lines in Fig. 1 show the electrical connection between the members.

As shown in Fig. 1, the film formation device 10 includes a vacuum chamber 11 coupled to an exhaust system 12

and depressurized to a predetermined pressure when the exhaust system 12 is driven. The vacuum chamber 11 has an upper wall that holds a plate-shaped upper electrode 13, which is electrically insulated from the vacuum chamber 11. The upper wall is connected via the upper electrode 13 to a power supply unit 14.

The power supply unit 14 includes a high frequency power supply 15 and a switching power supply 16. The power supply unit 14 modulates high frequency power, which has a predetermined frequency (e.g., 27.12 MHz) and which is generated by the high frequency power supply 15, to a pulse wave with the switching power supply 16 and supplies power during a predetermined ON period. When the power supply unit 14 is driven, the upper electrode 13 receives the pulsed high frequency power from the power supply unit 14 and generates plasma in the vacuum chamber 11.

A gas supply chamber 13a extends throughout the interior of the upper electrode 13, and the gas supply chamber 13a is connected to a gas supply system 17. The gas supply system 17 is connected to a gas cylinder 17a, which is filled with organic silane compound, and a gas cylinder 17b, which is filled with oxidation gas, to selectively draw the gas filled in each of the gas cylinders 17a and 17b into the gas supply chamber 13a. The gas supply chamber 13a is connected to a plurality of supply holes 13b, which are in communication with the interior of the vacuum chamber 11, and supplies the gas from the gas supply system 17 into the vacuum chamber 11 when the gas supply system 17 is driven.

Examples of an organic saline compound include tetraethoxysilane (TEOS) and trimethylsilane, and an

inactive gas, such as argon, helium, or nitrogen, may be added to these gases. Examples of an oxidation gas include oxygen and nitric oxide, and an inactive gas such as argon, helium, and nitrogen, may be added to these gases. Further, the gas supply system 17 may add hydrogen in addition to the organic silane compound and the oxidation gas.

A substrate stage 18 for holding a substrate S is arranged in the vacuum chamber 11. The substrate stage 18 holds the substrate S in a state in which the upper electrode 13 and the surface of the substrate S face toward each other. The substrate stage 18 includes a heater 18a for heating the substrate S to raise the temperature of the substrate S to a predetermined temperature. The substrate stage 18 is electrically grounded, and plasma is generated between the substrate stage 18 and the upper electrode 13 when high frequency power is applied to the upper electrode 13. The substrate S, which is held on the substrate stage 18, receives film formation seeds generated in the plasmic area, and grows a silicon insulative film, such as a silicon oxide film, on its surface.

A low temperature p-Si film, which undergoes a laser annealing process, is formed on the surface of the substrate S. A plurality of ridges having a height of about several tens of nanometers is formed on the surface of the low temperature p-Si film as low temperature p-Si crystallizes.

The film formation device 10 includes a controller 20 for executing the film formation process. The controller 20 is connected to the gas supply system 17 and generates a control signal corresponding to the gas supply system 17. The gas supply system 17, which is driven in response to the

control signal from the controller 20, adjusts the flow rate of the oxidation gas relative to the flow rate of the organic silane compound to a range of ten times to one hundred times when supplying organic silane compound and oxidation gas to the vacuum chamber 11. The film formation device 10 oxidizes most of the carbon elements contained in the organic silane compound in the plasmic area and discharges the carbon elements from the plasmic area.

The controller 20 is connected to the exhaust system 12 and generates a control signal corresponding to the exhaust system 12. The exhaust system 12, which is driven in response to the control signal from the controller 20, adjusts the pressure in the vacuum chamber 11 to 80 Pa to 300 Pa when the gas supply system 17 supplies the gas mixture. As a result, the film formation device 10 reduces collisions between radical components, suppresses excessive agglomeration of radical components, and densifies the film quality of the silicon insulative film.

The controller 20 is connected to the heater 18a and generates a control signal corresponding to the heater 18a. The heater 18a, which is driven in response to the control signal from the controller 20, adjusts the temperature of the substrate S to a range of 250°C to 430°C when the substrate S is arranged on the substrate stage 18. This allows for the film formation device 10 to decrease the defect concentration in the film and improve the film characteristics of the silicon insulative film.

The controller 20 is connected to the power supply unit 14 and generates a control signal corresponding to the power supply unit 14. The power supply unit 14, which is driven in

response to the control signal from the controller 20, and applies to the upper electrode 13 pulsed high frequency power having a power density of 0.1 W/cm^2 to 1.0 W/cm^2. In this case, the power supply unit 14 generates the pulsed high frequency power having a frequency of 5 kHz to 50 kHz at a predetermined duty ratio.

In the present embodiment, the duty ratio of the pulsed high frequency power output from the power supply unit 14 during actual film formation is referred to as a target duty ratio. The duty ratio in the present embodiment is a value determined from the ON period T1 of the high frequency power and the OFF period T2 of the high frequency power through $T1/(T1+T2)\times100$.

The controller 20 drives the power supply unit 14 and applies the high frequency power, which is obtained from the target duty ratio, to the upper electrode 13 to form the desired silicon insulative film on the surface of the low temperature p-Si film. In the present embodiment, the surface coating rate of the silicon insulative film, that is, the surface coating rate of when the silicon insulative film substantially evenly coats each ridge in the surface of the low temperature p-Si film and the silicon insulative film functions as a gate insulative film that is in accordance with the desired design rule is referred to as a target coating rate.

The silicon insulative film serving as the gate insulative film must have an even film thickness throughout the entire surface of the low temperature p-Si film to reduce variations in the threshold voltage and the leakage current. Further, the silicon insulative film serving as the

gate insulative film must have a lower concentration of impure elements such as carbon, hydrogen, and oxygen that are contained in the film to suppress variations in the threshold voltage.

The target duty ratio of the present embodiment is set with the largest duty ratio with which the surface coating rate of the silicon insulative film meets the target coating rate.

Various types of ions and various types of radicals are generated in the plasmic area of the vacuum chamber 11 when the film formation device 10 forms the silicon insulative film. The lifespan of the radicals is several milliseconds to several tens of milliseconds, whereas the lifespan of the ions is several microseconds to several tens of microseconds. Thus, during the OFF period T2 of the high frequency power, the ions disappear or drastically decrease and the radicals become dominant in the film formation. As a result, in the OFF period of the high frequency power, the radicals grow film formation seeds having high fluidity, for example, oligomers of the organic silicon compounds grow into the silicon insulative film, and the silicon insulative film grows on the ridges in the substrate surface with a high surface coating rate. In the ON period T1 of the high frequency power, the film formation seeds grow with a high plasma density into the silicon insulative film, and an electrically satisfactory silicon insulative film having only a small amount of impurities grows on the ridges of the substrate surface.

When decreasing the duty ratio of the high frequency power, the OFF period T2 becomes long. This increases the

surface coating rate of the silicon insulative film. However, the content of impure elements such as carbon and hydrogen contained in the organic silicon compound tends to easily increase. When the duty ratio of the high frequency power is simply decreased to increase the surface coating rate of the silicon insulative film, the flat band voltage of the silicon insulative film shifts drastically.

In the range in which the surface coating rate of the silicon insulative film meets the target coating rate for the film formation device 10, the target duty ratio is the value that most shortens the OFF period T2 of the high frequency power. In other words, the target duty ratio for the film formation device 10, which is taken from the film formation conditions of the silicon insulative film satisfying the target coating rate, causes the ON period T1 of the high frequency power to be the longest. Thus, the film formation device 10 can maximize the amount of power supplied to the reaction system while sufficiently coating each ridge in the surface of the low temperature p-Si film with the silicon insulative film. As a result, the film formation device 10 increases the surface coating rate while suppressing deterioration of the electrical characteristics of the silicon insulative film.

A method for forming the silicon insulative film with the film formation device 10 will now be described. First, the controller 20 drives the exhaust system 12 to depressurize the interior of the vacuum chamber 11 to a predetermined pressure. Then, the controller 20 loads the substrate S into the vacuum chamber 11 from outside the film formation device 10 and arranges the substrate S on the substrate stage 18.

After arranging the substrate S on the substrate stage 18, the controller 20 drives the heater 18a to raise the temperature of the substrate S to a predetermined temperature. When the temperature of the substrate S rises to the predetermined temperature, the controller 20 drives the gas supply system 17 to supply the gas mixture containing the organic silane compound and the oxidation gas from the gas supply chamber 13a into the interior of the vacuum chamber 11 and adjusts the interior of the vacuum chamber 11 to a predetermined pressure (80 Pa to 300 Pa).

After the gas mixture is supplied to the interior of the vacuum chamber 11, the controller 20 drives the power supply unit 14 to apply the pulsed high frequency power to the upper electrode 13. Preferably, the controller 20 drives the high frequency power supply 15 to generate a high frequency power of for example, 27.12 MHz, and drives the switching power supply 16 to pulse the high frequency power from the high frequency power supply 15 so as to satisfy the target duty ratio at the frequency of, for example, 5 kHz to 50 kHz. The controller 20 then applies the pulsed high frequency power of the target duty ratio from the power supply unit 14 to the upper electrode 13.

When the pulsed high frequency power is applied to the upper electrode 13, the upper electrode 13 functions as a cathode and the substrate stage 18 functions as an anode. Further, plasma is generated between the upper electrode 13 and the substrate S using the gas mixture containing the organic silane compound and the oxidation gas.

In the OFF period T2 of the high frequency power, the

film formation seeds having high fluidity grow into the silicon insulative film, and the silicon insulative film grows with a high surface coating rate on the ridges in the surface of the substrate S. In the ON period T1 of the high frequency power, the film formation reaction under high plasma density advances, and an electrically satisfactory silicon insulative film with a small amount of impurities grows on the ridges in the surface of the substrate S.

In this case, in the film formation method of the present embodiment, a plurality of substrates S having ridges in their surfaces are prepared, and film formation process having different duty ratios are preliminarily performed on each of the plurality of substrates S. The surface coating rate of the silicon insulative film is measured for each of the plurality of substrates S, and the range of the duty ratio that satisfies the target coating rate is obtained. The largest duty ratio within the duty ratio range that satisfies the target coating rate is set as the target duty ratio during actual film formation.

Thus, the ON period T1 of the high frequency power may be set to be the longest in the film formation conditions that forms the silicon insulative film and satisfies the target coating rate. As a result, the maximum amount of power may be supplied to the reaction system while obtaining the target coating rate for sufficiently coating each ridge in the surface of the low temperature p-Si film with the silicon insulative film. This increases the surface coating rate while suppressing deterioration of the electrical characteristics of the silicon insulative film.

[Examples]

A method for setting the target duty ratio will now be discussed using examples. First, a MOS structure diode was formed using a silicon oxide film, which was obtained from the film formation conditions shown below, as the gate insulative film. The CV curve of the diode was measured to obtain the flat band voltage for the example. The silicon oxide film obtained from the film formation conditions was formed on a dummy pattern P. The thickness of the silicon oxide film formed on the side wall of the dummy pattern P was defined as a side film thickness Ts and the thickness of the silicon oxide film F formed on the upper surface wall of the dummy pattern P was defined as the upper film thickness Tt to obtain the surface coating rate ((side film thickness Ts/upper film thickness Tt) ×100%) of each silicon oxide film. Referring to Fig. 2, a line pattern of which width W × height H was 0.4 μm × 0.6 μm and extending in one direction (direction perpendicular to the plane of drawing of Fig. 2) was used as the dummy pattern P.

The flat band voltage and the surface coating rate in the example are shown in Figs. 3A, 3B, and Table 1. The circles in table 1 indicates that the flat band voltage (e.g., absolute value) is smaller than or equal to the target voltage, or that the surface coating rate meets the target coating rate. The crosses in table 1 indicate that the flat band voltage is greater than the target voltage, or that the surface coating rate does not meet the target coating rate.

frequency of high-frequency power: 27.12 MHz
ON period T1 + OFF period T2: 100 microseconds
duty ratio: 30%, 50%, 70%, 100%
power density: 0.5 W/cm^2

film formation pressure: 190 Pa

film formation temperature: 340°C

TEOS flow rate/O_2 flow rate: 1/50

[Table 1]

	Duty Ratio (%)			
	30	50	70	100
Flat Band Voltage (V)	×	○	○	○
Surface Coating Rate (%)	○	○	×	×

In Fig. 3A, the flat band voltage is about -18 V and large when the duty ratio is 30%, and the flat band voltage is about -2V and small when the duty ratio is 50%, 70%, and 100%. In other words, with the film formation conditions of the example, it is apparent that a satisfactory silicon oxide film with lesser impurities and defects is obtained as the duty ratio increases (as the ON period T1 becomes longer).

In Fig. 3B, the surface coating rate is low or smaller than or equal to 60% when the duty ratio is 70%, 100%, and the surface coating rate exceeds 70% when the duty ratio is 30%, 50%. In one example, the range of duty ratios that satisfies the target coating rate is 30% to 50% when the target coating rate is 70%, in which case, the maximum value in the relevant range is 50%.

If the target duty ratio is set to 50%, that is, if the ON period T1 and the OFF period are each set to 50 microseconds, a silicon oxide film satisfying the target coating property and having a flat band voltage close to 0 V is obtained.

The film formation method of the embodiment has the advantages described below.

(1) The range of the duty ratio in which the surface coating rate of the silicon insulative film meets the target coating rate is obtained in advance, and the largest value in the range is set as the target duty ratio of the pulse wave.

Accordingly, in the range in which the surface coating rate meets the target value, the OFF period T2 of the high frequency power is set to the shortest time, and the ON period T1 of the high frequency power is set to the longest time. As a result, the ON period T1 of the high frequency power maximizes the amount of power to the reaction system, while the OFF period T2 of the high frequency power realizes a surface coating rate that meets the target coating rate. This suppresses deterioration in the electrical characteristics (increases the flat band shift) in the silicon insulative film and increases the surface coating rate. Further, the gate insulative film is thinned, and the electrical characteristics of the TFT are improved.

(2) Preferably, the frequency of the high frequency power is 27.12 MHz, and the ON period T1 and OFF period T2 are each 50 microseconds. Preferably, the pressure of the vacuum chamber 11 when forming the film is preferably 80 Pa to 300 Pa, and the power density at the upper electrode 13 is 0.1 W/cm^2 to 1.0 W/cm^2.

This ensures standardization of the dependency of the duty ratio on the surface coating rate and the dependency of

the duty ratio on the flat band voltage. In other words, a decrease in the duty ratio of the high frequency power small ensures an increase in the surface coating rate of the silicon insulative film. An increase in the duty ratio of the high frequency power ensures that the flat band voltage of the silicon insulative film is closer to 0 V. This suppresses deterioration of the electrical characteristics of the silicon insulative film and ensures that the surface coating rate is increased.

The duty ratio of the pulsed high frequency power is not limited to the largest duty ratio that satisfies the target coating rate of the silicon insulative film. In one example, when the range of duty ratio that satisfies the target coating rate of the silicon insulative film is 30% to 50%, and the range of duty ratio that maintains the flat band voltage of the silicon insulative film within a predetermined voltage range (e.g., -2 V to 0 V) is 40% to 50%, the duty ratio of the pulsed high frequency power may be set within a range of 40% to 50%.

CLAIMS:

1. A film formation method for forming a silicon insulative film on a substrate arranged in a vacuum chamber, the method comprising:

supplying the vacuum chamber with a gas mixture containing an organic silane compound and an oxidation gas;

generating a pulsed high frequency power to intermittently supply a high frequency power; and

forming the silicon insulative film on the substrate by plasmatizing the gas mixture with the pulsed high frequency power;

wherein said generating a pulsed high frequency power includes generating the pulsed high frequency power with a duty ratio that maintains an absolute value of a flat band voltage of the silicon insulative film below 2V and satisfies a target value of a surface coating rate of the silicon insulative film.

2. The film formation method according to claim 1, further comprising:

preliminarily performing a film formation process of the silicon insulative film on a plurality of substrates prior to actual formation of the silicon insulative film;

wherein said preliminarily performing a film formation process of the silicon insulative film includes forming the silicon insulative film on each of the plurality of substrates with pulsed high frequency power having different duty ratios, and determining a range of a duty ratio that satisfies the target value of the surface coating rate from the surface coating rate of the silicon insulative film

formed on each substrate.

3. The film formation method according to claim 1, wherein the high frequency power has a frequency of 27.12 MHz; and

an ON period and an OFF period are each 50 microseconds in a single cycle of the pulsed high frequency power.

4. The film formation method according to claim 3, wherein pressure of the vacuum chamber when forming the silicon insulative film is 80 Pa to 300 Pa; and

the power density of the pulsed high frequency power is 0.1 W/cm^2 to 1.0 W/cm^2.