CLAIMS

1. A method for manufacturing a silicon optical interposer, comprising:

providing a wafer, wherein a silicon optoelectronic device is formed on the wafer by etching for a waveguide, epitaxy, ion implantation, and fabricating a thermode, and the silicon optoelectronic device comprises a passive silicon optoelectronic device and an active silicon optoelectronic device;

depositing a first dielectric layer on a top of the silicon optoelectronic device, and forming a first contact via downward from a top of the first dielectric layer through chemical mechanical polishing, for the active silicon optoelectronic device and/or a thermo-optic device in the passive silicon optoelectronic device;

depositing a second dielectric layer, and forming through silicon vias downward from a top of the second dielectric layer;

depositing a third dielectric layer, and forming, on a top of the third dielectric layer, an electrode corresponding to the thermo-optic device and/or the active silicon optoelectronic device, wherein each electrode corresponds to the first contact via and the through via, and a second contact via and a third contact via are formed downward from a bottom of each electrode, the second contact via is connected to the first contact via, and the third contact via is connected to the through silicon via;

performing chemical mechanical polishing on a top of the structure that has been formed, depositing a fourth dielectric layer, forming a bonding pad opening running through the fourth dielectric layer, and forming a first under micro-bump metal or a first micro-bump, wherein the bonding pad opening is located above the electrode;

grinding the wafer from a back surface to expose the through silicon vias;

depositing a passivation layer on the back surface of the wafer; and

etching the passivation layer to form a passivation layer opening for the through silicon via; and forming a redistribution layer, and a second under micro-bump metal or a second micro-bump in the passivation layer opening, or forming a second under micro-bump metal or a second micro-bump in the passivation layer opening.

2. The method according to claim 1, wherein forming the first contact via downward from the top of the first dielectric layer, forming the through silicon vias downward from the top of the second dielectric layer, or forming the electrode, the second contact via, and the third contact via, comprises:

etching downward from the top of a target ~~the first~~ dielectric layer, to form a ~~first~~ target hole;

depositing an ~~first~~ isolation layer on a sidewall and a bottom of the ~~first~~ target hole;

coating the ~~first~~ target hole electrochemically with a ~~first~~ metal, or depositing a ~~first~~ metal in the target ~~first~~ hole; and

removing the ~~first~~ metal and the ~~first~~ isolation layer that are on a surface of the ~~first~~ target dielectric layer, through chemical mechanical polishing or etching;

wherein in case of forming the first contact via downward from the top of the first dielectric layer, the target dielectric layer is the first dielectric layer, the target hole is a first hole, the metal is a first metal;

wherein in case of forming the through silicon vias downward from the top of the second dielectric layer, the target dielectric layer is the second dielectric layer, the target hole is a second hole, the metal is a second metal;

wherein in case of forming the electrode, the second contact via, and the third contact via,

the target dielectric layer is the third dielectric layer, the target hole is a third hole and a fourth hole, the metal is a third metal; and

etching downward from the top of the target dielectric layer to form the target hole comprises: etching from the top of the third dielectric layer to form electrode grooves, and etching, downward from a bottom of each electrode groove, to form the third hole and the fourth hole.

3. The method according to claim 2, wherein

the ~~first~~ metal is copper;

the ~~first~~ target hole is filled with the copper through electrochemical coating, and the copper is annealed and subject to chemical mechanical polishing; and

a ~~first~~ stop layer is deposited after forming the first contact via and before depositing the second dielectric layer, after forming the through silicon via and before depositing the third dielectric layer, or after forming the electrode groove, the third hole, and the fourth hole and before depositing the fourth dielectric layer.

~~4. The method according to claim 3, wherein forming the through silicon vias downward from the top of the second dielectric layer comprises:~~

~~etching downward from the top of the second dielectric layer, to form a second hole;~~

~~depositing a second isolation layer on a sidewall and a bottom of the second hole;~~

~~coating the second hole electrochemically with a second metal;~~

~~removing the second metal and the second isolation layer that are on the surface of the second dielectric layer, through chemical mechanical polishing.~~

~~5. The method according to claim 4, wherein:~~

~~the second metal is copper;~~

~~the second hole is filled with the copper through electrochemical coating, and the copper annealed and subject to chemical mechanical polishing; and~~

~~a second stop layer is deposited after forming the through silicon via and before depositing the third dielectric layer.~~

~~6. The method according to claim 5, wherein forming the electrode, the second contact via, and the third contact via comprises:~~

~~etching from the top of the third dielectric layer to form electrode grooves, and etching, downward from a bottom of each electrode groove, to form a third hole and a fourth hole;~~

~~depositing a third isolation layer on sidewalls and bottoms, of the electrode grooves, the third hole, and the fourth hole;~~

~~coating the electrode grooves, the third hole, and the fourth hole electrochemically with a third metal, or depositing a third metal in the electrode grooves, the third hole and the fourth hole; and~~

~~removing the third metal and the third isolation layer that are on a surface of the third dielectric layer, through chemical mechanical polishing or etching.~~

~~7. The method according to claim 6, wherein:~~

~~the third metal is copper;~~

~~the electrode grooves, the third hole, and the fourth hole are filled with the copper through electrochemical coating, and the copper is annealed and subject to chemical mechanical polishing; and~~

~~a third stop layer is deposited after forming the electrode groove, the third hole, and the fourth hole, and before depositing the fourth dielectric layer.~~

~~8. The method according to claim 6, wherein each of the first isolation layer, the second isolation layer, and the third isolation layer is made of Ta, TaN, or a combination of Ta and TaN.~~

~~9. The method according to claim 1, wherein each of the first dielectric layer, the second dielectric layer, the third dielectric layer, and the fourth dielectric layer is a dielectric layer of silicon dioxide.~~

~~10. The method according to claim 7, wherein each of the first stop layer, the second stop layer, and the third stop layer is made of silicon nitride.~~

~~11~~4. The method according to claim 1, wherein each of the first dielectric layer, the

second dielectric layer, the third dielectric layer, and the fourth dielectric layer is formed through plasma enhanced chemical vapor deposition.

~~12~~5. The method according to claim ~~6~~2, wherein each of the first hole, the third hole, the fourth hole, and the electrode grooves is formed through dry etching.

~~13~~6. The method according to claim ~~4~~2, wherein the second hole is formed through DRIE etching.

~~14. The method for manufacturing a silicon optical interposer according to claim 1, wherein:~~

~~a perpendicular distance between each through silicon via and a side, of the thermo-optic device and/or the active silicon optoelectronic device, adjacent to said through silicon via is not less than 1.5 times a diameter of each through silicon via; and~~

~~a perpendicular distance between central axes of every two adjacent through silicon vias is not less than 3 times the diameter of each through silicon via.~~

~~15. The method for manufacturing a silicon optical interposer according to claim 1, wherein~~

~~the first under micro-bump metal is made of Cu/Ni/Au, and the first micro-bump is made of Cu/Ni/SnAg; and~~

~~the second under micro-bump metal is made of Cu/Ni/Au, and the second micro-bump is made of Cu/Ni/SnAg.~~

~~16~~7. A method for manufacturing a three-dimensional structure, comprising:

providing a silicon optical interposer manufactured by the method according to any one of claims 1 to ~~15~~6; and

bonding the silicon optical interposer to an electronic chip or an optoelectronic chip via the first under micro-bump metal or the first micro-bump;

wherein the method further comprises:

bonding the silicon optical interposer to a silicon interposer via the redistribution layer and the second under micro-bump metal or the second micro-bump, or via the second under micro-bump metal or the second micro-bump; and connecting the silicon optical interposer to a package substrate via a third under micro-bump metal or a third micro-bump arranged on a back surface of the silicon optical interposer; or

connecting the silicon optical interposer to a package substrate directly via the redistribution layer and the second under micro-bump metal or second micro-bump of the silicon optical interposer, or via the second under micro-bump metal or the second micro-bump silicon optical interposer of the silicon optical interposer.

~~17. The method according to claim 16, wherein the third under micro-bump metal is made of Cu/Ni/Au, and the third micro-bump is made of Cu/Ni/SnAg.~~

~~18~~8. A method for integrating a surface-electrode ion trap and a silicon optoelectronic device, comprising:

providing a wafer;

forming a grating ~~, wherein a silicon grating~~ and a silicon structure on the wafer, wherein the silicon structure is ~~are~~ formed at a top of the wafer through photolithography and etching, and the silicon structure is subject to ion implantation and annealing;

depositing a first dielectric layer, etching the first dielectric layer above the silicon structure to form an epitaxy opening, growing silicon or germanium through epitaxy on a top of the silicon structure via the epitaxy opening, and performing ion implantation and annealing on the silicon or the germanium, to form a silicon single-photon avalanche detector or a silicon-based germanium single-photon avalanche detector;

depositing a second dielectric layer, and forming a first contact via downward from a top of the second dielectric layer through etching and performing chemical mechanical polishing, for the silicon single-photon avalanche detector or the silicon-based germanium single-photon avalanche detector of a surface-incident type;

depositing a third dielectric layer, and forming through silicon vias downward from a top

of the third dielectric layer;

depositing a fourth dielectric layer, and forming an electrode on a top of the fourth dielectric layer, wherein the electrode comprises a first electrode corresponds to the silicon single-photon avalanche detector or the silicon-based germanium single-photon avalanche detector and a second electrode for the surface-electrode ion trap, each first electrode corresponds to the first contact via and the through silicon via, each second electrode corresponds to the through silicon via, a second contact via is formed downward from a bottom of each first electrode, the second contact via is connected to the first contact via, a third contact via is formed downward from the bottom of each first electrode and a bottom of each second electrode, and the third contact via is connected to the through silicon via;

grinding the wafer from a back surface to expose the through silicon vias;

depositing a passivation layer on the back surface of the wafer; and

etching the passivation layer to form a passivation layer opening for the through silicon via; and forming a redistribution layer, and a first under micro-bump metal or a first micro-bump in the passivation layer opening, or forming a first under micro-bump metal or a first micro-bump in the passivation layer opening;

wherein forming the grating comprises forming a silicon grating at the top of the wafer through photolithography and etching; or

wherein:

forming the grating comprises: depositing a fifth dielectric layer and a silicon nitride layer sequentially, and forming a silicon nitride grating at a top of the silicon nitride layer through photolithography and etching; and

the fifth dielectric layer above the silicon structure is further etched to form the epitaxy openning.

~~19~~9. The method according to claim ~~18~~8, wherein forming the first contact via downward from the top of the second dielectric layer, forming the through silicon vias downward from the top of the third dielectric layer, or forming the electrode, the second contact via, and the third contact via, comprises:

etching downward from the top of a target ~~the second~~ dielectric layer, to form a target ~~first~~ hole;

depositing an ~~first~~ isolation layer on a sidewall and a bottom of the ~~first~~ target hole;

coating the ~~first~~ target hole electrochemically with a ~~first~~ metal, or depositing a ~~first~~ metal in the target ~~first~~ hole;

removing the ~~first~~ metal and the ~~first~~ isolation layer that are on a surface of the target ~~second~~ dielectric layer, through chemical mechanical polishing or etching;

wherein in case of forming the first contact via downward from the top of the first dielectric layer, the target dielectric layer is the second dielectric layer, the target hole is a first hole, the metal is a first metal;

wherein in case of forming the through silicon vias downward from the top of the second dielectric layer, the target dielectric layer is the third dielectric layer, the target hole is a second hole, the metal is a second metal;

wherein in case of forming the electrode, the second contact via, and the third contact via,

the target dielectric layer is the fourth dielectric layer, the target hole is a third hole and a fourth hole, the metal is a third metal; and

etching downward from the top of the target dielectric layer to form the target hole comprises: etching from the top of the fourth dielectric layer to form electrode grooves, and etching, downward from a bottom of each electrode groove, to form the third hole and the fourth hole.

~~20~~10. The method according to claim ~~19~~9, wherein:

the ~~first~~ metal is copper;

the target ~~first~~ hole is filled with the copper through electrochemical coating, and the copper is annealed and subject to chemical mechanical polishing;

a ~~first~~ stop layer is deposited after forming the first contact via and before depositing the third dielectric layer, or after forming the through silicon via and before depositing the fourth

dielectric layer.

~~21. The method according to claim 20, wherein forming the through silicon vias downward from the top of the third dielectric layer comprises:~~

~~etching downward from the top of the third dielectric layer, to form a second hole;~~

~~depositing a second isolation layer on a sidewall and a bottom of the second hole;~~

~~coating the second hole electrochemically with a second metal;~~

~~removing the second metal and the second isolation layer that are on the surface of the third dielectric layer, through chemical mechanical polishing.~~

~~22. The method according to claim 21, wherein:~~

~~the second metal is copper;~~

~~the second hole is filled with the copper through electrochemical coating, and the copper annealed and subject to chemical mechanical polishing; and~~

~~a second stop layer is deposited after forming the through silicon via and before depositing the fourth dielectric layer.~~

~~23. The method according to claim 22, wherein forming the electrode, the second contact via, and the third contact via comprises:~~

~~etching from the top of the fourth dielectric layer to form electrode grooves, and etching, downward from a bottom of each electrode groove, to form a third hole and a fourth hole;~~

~~depositing a third isolation layer on sidewalls and bottoms, of the electrode grooves, the third hole, and the fourth hole;~~

~~coating the electrode grooves, the third hole, and the fourth hole electrochemically with a third metal, or depositing a third metal in the electrode grooves, the third hole and the fourth hole; and~~

~~removing the third metal and the third isolation layer that are on a surface of the fourth~~

~~dielectric layer, through chemical mechanical polishing or etching.~~

~~24. The method according to claim 23, wherein each of the first isolation layer, the second isolation layer, and the third isolation layer is made of Ta, TaN, or a combination of Ta and TaN.~~

~~25. The method according to claim 18, wherein each of the first dielectric layer, the second dielectric layer, the third dielectric layer, and the fourth dielectric layer is a dielectric layer of silicon dioxide.~~

~~26. The method according to claim 22, wherein each of the first stop layer and the second stop layer is made of silicon nitride.~~

~~27~~11. The method according to claim ~~18~~8, wherein each of the first dielectric layer, the second dielectric layer, the third dielectric layer, and the fourth dielectric layer is formed through plasma enhanced chemical vapor deposition.

~~28~~12. The method according to claim ~~23~~9, wherein each of the first hole, the third hole, the fourth hole, and the electrode grooves is formed through dry etching.

~~29~~13. The method to claim ~~21~~9, wherein the second hole is formed through DRIE etching.

~~30. The method according to claim 18, wherein:~~

~~a perpendicular distance between each through silicon via and a side, of the silicon single-photon avalanche detector or the silicon-based germanium single-photon avalanche detector, adjacent to said through silicon via is not less than 1.5 times a diameter of each through silicon via;~~

a perpendicular distance between central axes of every two adjacent through silicon vias is not less than 3 times the diameter of each through silicon via.

31. A method for integrating a surface-electrode ion trap and a silicon optoelectronic device, comprising:

providing a wafer, wherein a silicon structure, or a silicon grating and a silicon structure, are formed at a top of the wafer through photolithography and etching, and the silicon structure is subject to ion implantation and annealing;

depositing a first dielectric layer and a silicon nitride layer sequentially, and forming a silicon nitride grating at a top of the silicon nitride layer through photolithography and etching ;

depositing a second dielectric layer, etching the first dielectric layer and the second dielectric layer above the silicon structure to form an epitaxy opening, growing silicon or germanium through epitaxy on a top of the silicon structure via the epitaxy opening, and performing ion implantation and annealing on the silicon or the germanium, to form a silicon single-photon avalanche detector or a silicon-based germanium single-photon avalanche detector;

depositing a third dielectric layer, and forming a first contact via downward from a top of the third dielectric layer through etching and performing chemical mechanical polishing, for the silicon single-photon avalanche detector or the silicon-based germanium single-photon avalanche detector of a surface-incident type;

depositing a fourth dielectric layer, and forming through silicon vias downward from a top of the fourth dielectric layer;

depositing a fifth dielectric layer, and forming an electrode on a top of the fifth dielectric layer, wherein the electrode comprises a first electrode corresponds to the silicon single-photon avalanche detector or the silicon-based germanium single-photon avalanche detector and a second electrode for the surface-electrode ion trap, each first electrode corresponds to the first contact via and the through silicon via, each second electrode corresponds to the through silicon via, a second contact via is formed downward from a bottom of each first electrode, the second contact via is connected to the first contact via, a

third contact via is formed downward from the bottom of each first electrode and a bottom of each second electrode, and the third contact via is connected to the through silicon via;

grinding the wafer from a back surface to expose the through silicon vias;

depositing a passivation layer on the back surface of the wafer; and

etching the passivation layer to form a passivation layer opening for the through silicon via; and forming a redistribution layer, and a first under micro-bump metal or a first micro-bump in the passivation layer opening, or forming a first under micro-bump metal or a first micro-bump in the passivation layer opening.

32. The method according to claim 31, wherein forming the first contact via downward from the top of the third dielectric layer comprises:

etching downward from the top of the third dielectric layer, to form a first hole;

depositing a first isolation layer on a sidewall and a bottom of the first hole;

coating the first hole electrochemically with a first metal, or depositing a first metal in the first hole;

removing the first metal and the first isolation layer that are on a surface of the third dielectric layer, through chemical mechanical polishing or etching.

33. The method according to claim 32, wherein:

the first metal is copper;

the first hole is filled with the copper through electrochemical coating, and the copper is annealed and subject to chemical mechanical polishing;

a first stop layer is deposited after forming the first contact via and before depositing the fourth dielectric layer.

34. The method according to claim 33, wherein forming the through silicon vias downward from the top of the fourth dielectric layer comprises:

etching downward from the top of the fourth dielectric layer, to form a second hole;

depositing a second isolation layer on a sidewall and a bottom of the second hole;

coating the second hole electrochemically with a second metal;

removing the second metal and the second isolation layer that are on the surface of the fourth dielectric layer, through chemical mechanical polishing.

35. The method according to claim 34, wherein:

the second metal is copper;

the second hole is filled with the copper through electrochemical coating, and the copper annealed and subject to chemical mechanical polishing; and

a second stop layer is deposited after forming the through silicon via and before depositing the fourth dielectric layer.

36. The method according to claim 35, wherein forming the electrode, the second contact via, and the third contact via comprises:

etching from the top of the fifth dielectric layer to form electrode grooves, and etching, downward from a bottom of each electrode groove, to form a third hole and a fourth hole;

depositing a third isolation layer on sidewalls and bottoms, of the electrode grooves, the third hole, and the fourth hole;

coating the electrode grooves, the third hole, and the fourth hole electrochemically with a third metal, or depositing a third metal in the electrode grooves, the third hole and the fourth hole; and

removing the third metal and the third isolation layer that are on a surface of the fifth dielectric layer, through chemical mechanical polishing or etching.

37. The method according to claim 36, wherein each of the first isolation layer, the second isolation layer, and the third isolation layer is made of Ta, TaN, or a combination of Ta and TaN.

~~38. The method according to claim 31, wherein each of the first dielectric layer, the second dielectric layer, the third dielectric layer, and the fourth dielectric layer is a dielectric layer of silicon dioxide.~~

~~39. The method according to claim 35, wherein each of the first stop layer and the second stop layer is made of silicon nitride.~~

~~40. The method according to claim 31, wherein each of the first dielectric layer, the second dielectric layer, the third dielectric layer, the fourth dielectric layer, and the fifth dielectric layer is formed through plasma enhanced chemical vapor deposition.~~

~~41. The method according to claim 36, wherein each of the first hole, the third hole, the fourth hole, and the electrode grooves is formed through dry etching.~~

~~42. The method according to claim 34, wherein the second hole is formed through DRIE etching.~~

~~43. The method according to claim 31, wherein:~~

~~a perpendicular distance between the through silicon via and a side of the silicon single-photon avalanche detector or the silicon-based germanium single-photon avalanche detector adjacent to the through silicon via is not less than 1.5 times a diameter of each through silicon via; and~~

~~a perpendicular distance between central axes of every two adjacent through silicon vias is not less than 3 times the diameter of each through silicon via.~~

~~44~~14. A method for manufacturing a three-dimensional structure, comprising:

bonding an integrated structure manufactured by the method according to any one of

claims 8 to 13~~18-30 or 31-43~~ to a silicon interposer via the redistribution layer and the first under micro-bump metal or the first micro-bump, or via the first under micro-bump metal or the first micro-bump; and connecting the silicon optical interposer to a package substrate, via a second under micro-bump metal or a second micro-bump arranged on a back surface of the silicon optical interposer, or via a lead; or

connecting the integrated structure to a package substrate directly via the redistribution layer and the first under micro-bump metal or first micro-bump of the integrated structure.

~~45. The method according to claim 44, wherein the second under micro-bump metal is made of Cu/Ni/Au, and the second micro-bump is made of Cu/Ni/SnAg.~~

~~46~~15. An integrated structure of a surface-electrode ion trap and a silicon optoelectronic device, comprising:

a wafer, wherein a ~~silicon~~ grating and a silicon structure are located on the wafer, the silicon structure is ~~are~~ formed at a top of the wafer through photolithography and etching, and the silicon structure is subject to ion implantation and annealing;

a first dielectric layer formed on the above-formed structure, wherein the first dielectric layer above the silicon structure is etched to form epitaxy openings, silicon or germanium is grown through epitaxy on a top of the silicon structure via the epitaxy opening, and ion implantation and annealing is performed to form silicon single-photon avalanche detectors or the silicon-based germanium single-photon avalanche detectors;

a second dielectric layer formed on the above-formed structure, wherein first contact vias are formed downward from a top of the second dielectric layer for the silicon single-photon avalanche detectors or the silicon-based germanium single-photon avalanche detectors of a surface-incident type;

a third dielectric layer formed on the above-formed structure, wherein through silicon vias are formed downward from a top of the third dielectric layer;

a fourth dielectric layer formed on the above-formed structure, wherein electrodes are formed on a top of the fourth dielectric layer, the electrode comprises a first electrode

corresponds to the silicon single-photon avalanche detector or the silicon-based germanium single-photon avalanche detector and a second electrode for the surface-electrode ion trap, each first electrode corresponds to the first contact via and the through silicon via, each second electrode corresponds to the through silicon via, a second contact via is formed downward from a bottom of each first electrode, the second contact via is connected to the first contact via, a third contact via is formed downward from the bottom of each first electrode and a bottom of each second electrode, and the third contact via is connected to the through silicon via; and

a first passivation layer deposited on a back surface of the wafer, wherein the back surface is grinded to expose the through silicon vias, and passivation layer openings for the through silicon vias are formed by etching the passivation layer, and a first under micro-bump metal or a first micro-bump is formed in each passivation layer opening, or a first under micro-bump metal or a first micro-bump is formed on a redistribution layer in each passivation layer opening;

wherein the grating comprises at least one of a silicon grating or a silicon nitride grating;

wherein the silicon grating is formed at the top of the wafer through photolithography and etching; and

wherein the silicon nitride grating is formed at a top of a silicon nitride layer through photolithography and etching, the integrated structure further comprises a fifth dielectric layer and the silicon nitride layer that are sequentially located between the wafer and the first dielectric layer, and the fifth dielectric layer is further etched to form the epitaxy openings.

~~47~~16. The integrated structure according to claim ~~46~~15, wherein ~~each~~ the first contact vias, the through silicon vias, or a combination of the electrodes, the second contact vias and the third contact vias comprises:

a ~~first~~ target hole, arranged in ~~the second~~ a target dielectric layer;

an ~~first~~ isolation layer, deposited on a bottom and a sidewall of the ~~first~~ target hole; and

a ~~first~~ metal structure, with which the ~~first~~ target hole with the ~~first~~ isolation layer is electrochemically coated, or which is deposited in the ~~first~~ target hole with the ~~first~~ isolation layer;

wherein in case of the first contact vias, the target dielectric layer is the second dielectric layer, the target hole is a first hole, the metal structure is a first metal structure;

wherein in case of the through silicon vias, the target dielectric layer is the third dielectric layer, the target hole is a second hole, the metal structure is a second metal structure;

wherein in case of the combination of the electrodes, the second contact vias and the third contact vias,

the target dielectric layer is the fourth dielectric layer, the target hole is a third hole and a fourth hole, the metal structure is a third metal structure; and

the top of the fourth dielectric layer is etched to form electrode grooves, and a bottom of each electrode groove is etched to form the third hole and the fourth hole.

~~48~~17. The integrated structure according to claim ~~47~~16, wherein:

the ~~first~~ metal structure is a copper structure;

the ~~first~~ target hole is filled with copper through electrochemical coating, and the copper is annealed and subject to chemical mechanical polishing, to form the copper structure; and

a ~~first~~ stop layer is deposited after forming the first contact via and before depositing the third dielectric layer, or after forming the through silicon vias and before depositing the fourth dielectric layer.

~~49. The integrated structure according to claim 48, wherein each through silicon via comprises:~~

~~a second hole, arranged in the third dielectric layer;~~

~~a second isolation layer, deposited on a sidewall and a bottom of the second hole; and~~

~~a second metal structure, with which the second hole with the second isolation layer is electrochemically coated.~~

~~50. The integrated structure according to claim 49, wherein:~~

~~the second metal structure is a copper structure;~~

~~the second hole is filled with copper through electrochemical coating, and the copper is annealed and subject to chemical mechanical polishing, to form the copper structure; and~~

~~a second stop layer is deposited after forming the through silicon vias and before depositing the fourth dielectric layer.~~

~~51. The integrated structure according to claim 50, wherein:~~

~~electrode grooves are formed by etching from the top of the fourth dielectric layer;~~

~~a third hole and a fourth hole are formed by etching downward from a bottom of each electrode groove;~~

~~a third isolation layer is deposited on sidewalls and bottoms of the electrode grooves, the third hole, and the fourth hole; and~~

~~the electrode grooves, the third hole, and the fourth hole with the third isolation layer are electrochemically coated with a third metal, or a third metal is deposited in the electrode grooves, the third hole and the fourth hole with the third isolation layer, to form a third metal structure.~~

~~52. The integrated structure according to claim 51, wherein:~~

~~the third metal structure is a copper structure;~~

~~the electrode grooves, the third hole, and the fourth hole are filled with copper through electrochemical coating; and~~

~~the copper is annealed and subject to chemical mechanical polishing, to form the copper structure.~~

~~53~~18. The integrated structure according to claim ~~52~~17, wherein a second passivation layer is deposited in the electrode grooves, the third hole, and the fourth hole, after the third isolation layer and the third metal structure are sequentially formed.

~~54~~19. The integrated structure according to claim ~~53~~16, wherein each of the first isolation layer, the second isolation layer, and the third isolation layer is made of Ta, TaN, or a combination of Ta and TaN.

~~55~~20. The integrated structure according to claim ~~46~~15, wherein each of the first dielectric layer, the second dielectric layer, the third dielectric layer, and the fourth dielectric layer is a dielectric layer of silicon dioxide.

~~56~~21. The integrated structure according to claim ~~49~~17, wherein ~~each of~~ the ~~first~~ stop layer ~~and the second stop layer~~ is made of silicon nitride.

~~57~~22. The integrated structure according to claim ~~46~~15, wherein:

a perpendicular distance between each through silicon via and a side, of the silicon single-photon avalanche detector or the silicon-based germanium single-photon avalanche detector, adjacent to said through silicon via is not less than 1.5 times a diameter of each through silicon via;

a perpendicular distance between central axes of every two adjacent through silicon vias is not less than 3 times the diameter of each through silicon via.

23. The integrated structure according to claim 15, wherein the first under micro-bump metal is made of Cu/Ni/Au, and the first micro-bump is made of Cu/Ni/SnAg.

~~58. An integrated structure of a surface-electrode ion trap and a silicon optoelectronic device, comprising:~~

~~a wafer, wherein a silicon structure is formed at a top of the wafer through photolithography and etching, and the silicon structure is subject to ion implantation and annealing, or wherein a silicon grating and a silicon structure are formed at a top of the wafer through photolithography and etching, and the silicon structure is subject to ion implantation~~

and annealing;

a first dielectric layer and a silicon nitride layer, sequentially formed on the above-formed structure, wherein silicon nitride gratings are formed at a top of the silicon nitride layer through photolithograph and etching;

a second dielectric layer formed on the above-formed structure, wherein the first dielectric layer and the second dielectric layer above the silicon structure is etched to form epitaxy openings, silicon or germanium is grown through epitaxy on a top of the silicon structure via the epitaxy opening, and ion implantation and annealing is performed to form silicon single-photon avalanche detectors or the silicon-based germanium single-photon avalanche detectors;

a third dielectric layer formed on the above-formed structure, wherein first contact vias are formed downward from a top of the third dielectric layer for the silicon single-photon avalanche detectors or the silicon-based germanium single-photon avalanche detectors of a surface-incident type;

a fourth dielectric layer formed on the above-formed structure, wherein through silicon vias are formed downward from a top of the fourth dielectric layer;

a fifth dielectric layer formed on the above-formed structure, wherein electrodes are formed on a top of the fifth dielectric layer, the electrode comprises a first electrode corresponds to the silicon single-photon avalanche detector or the silicon-based germanium single-photon avalanche detector and a second electrode for the surface-electrode ion trap, each first electrode corresponds to the first contact via and the through silicon via, each second electrode corresponds to the through silicon via, a second contact via is formed downward from a bottom of each first electrode, the second contact via is connected to the first contact via, a third contact via is formed downward from the bottom of each first electrode and a bottom of each second electrode, and the third contact via is connected to the through silicon via; and

a first passivation layer deposited on a back surface of the wafer, wherein the back surface is grinded to expose the through silicon vias, and passivation layer openings for the through silicon vias are formed by etching the passivation layer, and a first under micro-bump metal or a first micro-bump is formed in each passivation layer opening, or a first under

micro-bump metal or a first micro-bump is formed on a redistribution layer in each passivation layer opening.

59. The integrated structure according to claim 58, wherein each first contact via comprises:

a first hole, arranged in the third dielectric layer;

a first isolation layer, deposited on a bottom and a sidewall of the first hole; and

a first metal structure, with which the first hole with the first isolation layer is electrochemically coated, or which is deposited in the first hole with the first isolation layer.

60. The integrated structure according to claim 59, wherein:

the first metal structure is a copper structure;

the first hole is filled with copper through electrochemical coating, and the copper is annealed and subject to chemical mechanical polishing, to form the copper structure; and

a first stop layer is deposited after forming the first contact via and before depositing the fourth dielectric layer.

61. The integrated structure according to claim 60, wherein each through silicon via comprises:

a second hole, arranged in the fourth dielectric layer;

a second isolation layer, deposited on a sidewall and a bottom of the second hole; and

a second metal structure, with which the second hole with the second isolation layer is electrochemically coated.

62. The integrated structure according to claim 61, wherein:

the second metal structure is a copper structure;

the second hole is filled with copper through electrochemical coating, and the copper is

annealed and subject to chemical mechanical polishing, to form the copper structure; and

a second stop layer is deposited after forming the through silicon vias and before depositing the fifth dielectric layer.

63. The integrated structure according to claim 62, wherein:

electrode grooves are formed by etching from the top of the fifth dielectric layer;

a third hole and a fourth hole are formed by etching downward from a bottom of each electrode groove;

a third isolation layer is deposited on sidewalls and bottoms of the electrode grooves, the third hole, and the fourth hole; and

the electrode grooves, the third hole, and the fourth hole with the third isolation layer are electrochemically coated with a third metal, or a third metal is deposited in the electrode grooves, the third hole and the fourth hole with the third isolation layer, to form a third metal structure.

64. The integrated structure according to claim 63, wherein:

the third metal structure is a copper structure;

the electrode grooves, the third hole, and the fourth hole are filled with copper through electrochemical coating; and

the copper is annealed and subject to chemical mechanical polishing, to form the copper structure.

65. The integrated structure according to claim 64, wherein a second passivation layer is deposited in the electrode grooves, the third hole, and the fourth hole, after the third isolation layer and the third metal structure are sequentially formed.

66. The integrated structure according to claim 65, wherein each of the first isolation layer, the second isolation layer, and the third isolation layer is made of Ta, TaN, or a

~~combination of Ta and TaN.~~

~~67. The integrated structure according to claim 58, wherein each of the first dielectric layer, the second dielectric layer, the third dielectric layer, the fourth dielectric layer, and the fifth dielectric layer is a dielectric layer of silicon dioxide.~~

~~68. The integrated structure according to claim 62, wherein each of the first stop layer and the second stop layer is made of silicon nitride.~~

~~69. The integrated structure according to claim 58, wherein:~~

~~a perpendicular distance between each through silicon via and a side, of the silicon single-photon avalanche detector or the silicon-based germanium single-photon avalanche detector, adjacent to said through silicon via is not less than 1.5 times a diameter of each through silicon via;~~

~~a perpendicular distance between central axes of every two adjacent through silicon vias is not less than 3 times the diameter of each through silicon via.~~

~~70~~24. A three-dimensional structure, comprising:

the integrated structure according to any one of claims 15 to 23~~ 46-57 or 58-69~~;

and the three-dimensional structure further comprises:

a silicon interposer and a package substrate, wherein the silicon interposer is bonded to the first under micro-bump metal or the first micro-bump of the integrated structure, and the package substrate is bonded to the silicon interposer via the second under micro-bump metal or a second micro bump arranged on the back surface of the silicon interposer, or bonded to the silicon interposer via a lead; or

a package substrate, directly connected to the first under micro-bump metal or the first micro-bump of the integrated structure.

~~71~~25. The three-dimensional structure according to claim ~~70~~24, wherein the second

under micro-bump metal is made of Cu/Ni/Au, and the second micro-bump is made of Cu/Ni/SnAg.