

The invention commences from a switched-mode power supply unit as described in the preamble of Claim 1.

In a switched-mode power supply unit of this kind it is known (DE-OS 37 05 392) to connect a network comprising a capacitor, a resistor and a diode to the primary winding and/or the secondary winding of the transformer. This network, which is also known as a "snubber", serves to limit the flank steepness and the voltage peaks across the windings of the transformer.

It has been proved that a substantial power loss occurs across the resistor of this network, which power loss is in the order of 5 - 10% of the total power transmitted by the power supply unit and leads to a reduction in the efficiency of, and undesired heating of the adjacent components. This power loss is particularly marked in the case of a transition to higher operating frequencies of the switched-mode power supply unit of, for example, 32 kHz and 64 kHz.

A switched-mode power supply unit is also known (EP-A2 0 336 725; FR 2 608 857) wherein, for the regulation of the output voltage, a switch is arranged in parallel to the diode which generates the operating d.c. voltage from the pulse voltage across the secondary winding, said switch being controlled in such manner that when the charging current flowing via the diode into the charging capacitor has died out, a current opposed to the charging current flows from the charging capacitor into the secondary winding.

It is also known (EP-A2 0 279 335), in a switched-mode power supply unit, to connect a network comprising the series connection of a capacitor and the parallel connection of a resistor and a diode to the primary winding or secondary winding of the transformer. This network serves to reduce voltage peaks across the switching transistor when the current is switched off. The resistor in this network inevitably results in a considerable power loss.

The aim of the invention is, in a switched-mode power supply unit of the type described in the introduction, to reduce the power loss occurring across the resistor of the aforementioned network.

This aim is fulfilled by the invention described in Claim 1. Advantageous further developments of the invention are described in the sub-claims.

The invention will be explained in the form of an exemplary embodiment making reference to the drawing wherein:

Figure 1 is a simplified circuit diagram of a known switched-mode power supply unit;

Figure 2 illustrates curves in explanation of the mode of operation according to Figure 1 and

Figure 3 illustrates a switched-mode power supply unit in accordance with the invention.

Figure 1 shows a switched-mode power supply unit with the primary winding 1 of the transformer Tr and with the switching transistor T1 which are connected to an operating voltage. The secondary winding 2 is connected via the diode D1 to the charging capacitor C1 which supplies a stabilized operating voltage +U1 across the terminal 3. The switching transistor T1 is controlled by the processor 4 with a switching voltage 5, the frequency of which is in the order of 30 - 60 kHz. The switching voltage 5 is pulse-width-modulated in such manner that the operating voltage U1 is stabilized by a controlled switch-on time of the switching transistor T1.

The field effect transistor T2, which is controlled by the processor 4 with a switching voltage 6, is arranged in parallel to the diode D1. To limit the flank steepness and the voltage peaks across the transformer Tr, only the capacitor C2 is arranged in parallel to the transistor T1.

The mode of operation will be explained making reference to Figure 2. At the time t1 the transistor T1 is brought into the non-conductive state by the switching

voltage 5 so that the current i_1 falls to zero. As a result, in the secondary winding 2 a voltage is induced which causes a charging current i_D to flow via the diode D1 into the charging capacitor C1. This charging current falls in an approximately linear fashion and attains the value zero at the time t_2 . At the time t_2 the transistor T2 is driven conductive and generates a current i_{T2} which, in opposition to i_D , flows from the charging capacitor C1 into the secondary winding 2. As a result, a part of the energy stored in the charging capacitor C1 at the time t_2 is returned to the transformer Tr. T2 is brought into the non-conductive state at the time t_3 . As a result of this measure the voltage U_{ce} across the transistor T1 is modified in such manner that in accordance with Figure 2 this voltage has fallen to zero when the transistor T1 is re-ignited at the time t_4 .

In Figure 3 the aforementioned network comprising the capacitor C2, the diode D2 and the resistor R2 is arranged in parallel to the transistor T1. The power loss occurring across the resistor R2 is reduced by the field effect transistor T3 connected in parallel to R2. The field effect transistor T3 is driven conductive by the pulse 7 from the processor 4 during the respective pulse flanks across the transformer Tr between the times $t_3 - t_4$ and thus short-circuits the resistor R2. During the remainder of the time, in which T1 is in the non-conductive state, T3 is non-conductive so that at this time the resistor R2 can fulfil its damping function. Thus the resistor R2 itself carries out a damping function, but the power loss falling across the resistor R2 is greatly reduced. The circuit according to Figure 3 is particularly advantageous when vibrations produced by C2 and leakage inductances of Tr are additionally to be damped in the circuit.

If the circuit according to Figures 1 or 2 comprises a plurality of secondary windings 2 each with a diode D1 and a charging capacitor C1 for the generation of different

operating voltages, it is sufficient to employ the measure according to Figure 1 comprising the transistor T2 only in the case of one secondary winding.

Claims

1. A switched-mode power supply unit with a transformer (Tr) comprising a primary winding (1), which is arranged in series with a switching transistor (T1), and a secondary winding (2) which is connected via a diode (D1) to a charging capacitor (C1) and during the non-conductive period of the switching transistor (T1) supplies a charging current (i_D) via the diode (D1) to the charging capacitor (D1), wherein a first switch (T2) is arranged in parallel to the diode (D1), which first switch (T2) is controlled in such manner that when the charging current (i_D) has died out a current (i_{T2}) opposed to the charging current (i_D) flows from the charging capacitor (C1) into the secondary winding (2), characterised in that a network comprising the series connection of a capacitor (C2) and the parallel connection of a resistor (R2) and a diode (D2) is connected in parallel to the switching transistor (T1), and a second switch (T3) is arranged in parallel to the resistor (R2), which second switch (T3) is driven conductive by a control voltage (7) during the pulse flanks of the voltage (U_{ce}) across the primary winding (1).
2. A circuit as claimed in Claim 1, characterised in that the first or second switch (T2, T3) is formed by a field effect transistor (T2, T3).
3. A circuit as claimed in Claim 1 or 2, characterised in that the switch (T2, T3) is controlled by a pulse (6, 7) from a processor (4) which also controls the switching transistor (T1) in terms of stabilizing the generated operating voltage (U_1).
4. A circuit as claimed in Claim 1, characterised in that in the case of a plurality of secondary windings each



with a diode and a charging capacitor, the first switch (T2) is provided only in the case of one secondary winding.

