What is claimed is:

1. A memory device comprising:

a memory area including a first memory area including first memory cells storing N-bit data and a second memory area including second memory cells storing M-bit data, where 'M' and 'N' are natural numbers and M is greater than N; and

a controller configured to read data stored in the first memory area using a first read operation, read data stored in the second memory area using a second read operation different from the first read operation, selectively store data in one of the first memory area and the second memory area based on a frequency of use (FOU) of the data and an importance weighting of the data, and store data having a FOU lower than a FOU reference value and a weight higher than a predetermined threshold value in a security area.

2. The memory device of claim 1, wherein the controller is further configured to compare the FOU of the data with the FOU reference value, and to store the data in the second memory area upon determining that the FOU of the data is less than or equal to the FOU reference value, and to store the data in the first memory area upon determining that the FOU of the data is not less than or equal to the FOU reference value.

3. The memory device of claim 1, wherein the controller is further configured to store the data in the second memory area upon receipt of the data in the memory device, periodically detect a current FOU of the stored data, and to store the data in the first memory area upon determining that the current FOU of the data is not less than or equal to the FOU reference value.

4. The memory device of any one of claims 1 to 3, wherein the memory area includes a first memory plane including the first memory area, and a second memory plane different from the first memory plane including the second memory area.

5. The memory device of any one of claims 1 to 3, wherein the memory area includes a first memory bock including the first memory area, a second memory block including the second memory area, and

the first memory block and the second memory block are included in a single memory plane.

6. The memory device of any one of claims 1 to 3, wherein the first memory cells are connected to a first group of wordlines and the second memory cells are connected to a second group of wordlines different from the first group of wordlines, and the first group of wordlines and the second group of wordlines are included in a single memory block.

7. The memory device of claim 6, wherein the first group of wordlines are disposed below the second group of wordlines in the memory block.

8. The memory device of any one of claims 1 to 7, wherein the first read operation is a voltage sensing operation and the second read operation is a current sensing operation.

9. The memory device of claim 8, wherein during the voltage sensing operation, the controller is further configured to precharge a selected bitline connected to a selected

memory cell among the first memory cells and to connect the selected memory cell with a sensing node while developing the selected bitline.

10. The memory device of any one of claims 1 to 9, wherein the controller is further configured to compare the FOU of the data with a first FOU reference value and a second FOU reference value less than the first FOU reference value,

to store the data in the first memory area, upon determining that the FOU of the data is greater than the first FOU reference value, and to store the data in the second memory area, upon determining that the FOU of the data is less than or equal to the first FOU reference value and greater than the second FOU reference value, and

to store the data in a memory area other than the first memory area and the second memory area, upon determining that the FOU of the data is less than or equal to the second FOU reference value.

11. The memory device of any one of claims 1 to 10, wherein N=1 and M=2, and

the memory area further includes a third memory area including third memory cells each storing 3-bit data and a fourth memory area including fourth memory cells storing 4-bit data.

12. The memory device of claim 10 or claim 11, wherein the controller is further configured to compare the FOU of the data with a third FOU reference value,

to store the data in the third memory area, upon determining that the FOU of the data is less than or equal to the second FOU reference value and greater than the third FOU reference value, and

to store the data in the fourth memory area, upon determining that the FOU of the data is less than or equal to the third FOU reference value.

13. The memory device of claim 11 or claim 12, wherein the controller is further configured to allow erasure of the data stored in the fourth memory area if a user confirms erasure.

14. The memory device of claim 13, wherein the controller stores the data in the security area if the user does not confirm erasure when the weight assigned to the data exceeds the predetermined threshold value.

15. The memory device of any one of claims 1 to 14, wherein the memory area and the controller are commonly integrated on a single semiconductor chip.

16. A memory device comprising:

a memory area including a first memory area including first memory cells, another memory area including memory cells, and a security area; and

a controller configured to:

read data stored in the first memory area using a first read operation;

read data stored in the another memory area using a second read operation different from the first read operation;

selectively store data in one of the first memory area and the another memory area based on a frequency of use (FOU) of the data and an importance weighting of the data; and

store data having a FOU lower than a predetermined reference value and a

weight higher than a predetermined threshold value in the security area,

wherein each of the first memory cells stores 1-bit data, and each of the memory cells stores 2 or more bits data.

17. The memory device of claim 16, wherein the another memory area includes a second memory area including memory cells storing 2-bit data, a third memory area including memory cells storing 3-bit data, and a fourth memory area including memory cells storing 4-bit data, and

the security area includes at least a portion of at least one of the third memory area and the fourth memory area.

18. The memory device of claim 16 or claim 17, wherein the first read operation is a voltage sensing operation and the second read operation is a current sensing operation.

19. The memory device of claim 17, wherein the first read operation reads data stored in the first memory area faster than the second read operation reads data stored in the second memory area.

20. A computer system comprising:

a processor configured to control execution of a first operation at a first speed, control execution of a second operation at a second speed different from the first speed, and provide data to a memory device,

wherein the memory device comprises:

a memory area including a first memory area including memory cells operated as single level memory cells (SLC) and a second memory area including memory

cells operated as at least one of multi level memory cells (MLC), triple level memory cells (TLC) and quad level memory cells (QLC); and

a controller configured to:

read data stored in the first memory area using a first read operation in response to execution of the first operation;

read data stored in the second memory area using a second read operation different from the first read operation in response to execution of the second operation;

selectively store the data provided by the processor in one of the first memory area and the second memory area based on a frequency of use (FOU) of the data and an importance weighting of the data; and

store data having a FOU lower than a predetermined reference value and a weight higher than a predetermined threshold value in a security area.