What is claimed is:

1. A semiconductor memory device comprising:

a memory cell array;

a plurality of data input/output (I/O) pins configured to receive write data to be stored in the memory cell array or to output read data stored in the memory cell array; and

a clock divider configured to generate a second command clock signal based on a first command clock signal,

wherein:

the semiconductor memory device is configured to perform a burst operation in which a single data set comprising a plurality of data bits is input or output through the plurality of data I/O pins based on a single command received from an external memory controller,

a number of the plurality of data I/O pins corresponds to an integer that is not a power-of-two,

a burst length representing a unit of the burst operation corresponds to an integer that is not a power-of-two, and

the memory cell array and the plurality of data I/O pins are configured to operate based on the second command clock signal and a data clock signal.

2. The semiconductor memory device of Claim 1, wherein:

the single data set comprises the write data or the read data,

the plurality of data bits in the single data set comprise first data bits corresponding to the write data or the read data, and

a number of the first data bits corresponds to an integer that is a power-of-two.

3. The semiconductor memory device of Claim 2, wherein:

the single data set further comprises additional data associated with the write data or the read data, and

the plurality of data bits in the single data set further comprises second data bits other than the first data bits, the second data bits corresponding to the additional data.

4. The semiconductor memory device of Claim 3, wherein a number of the second data bits corresponds to an integer that is a power-of-two.

5. The semiconductor memory device of Claim 3 or Claim 4, wherein a number of the plurality of data bits including the first data bits and the second data bits corresponds to an integer that is not a power-of-two.

6. The semiconductor memory device of any one of Claims 3 to 5, wherein the additional data comprises at least one of data bus inversion (DBI) information, error correction code (ECC) information, and meta data.

7. The semiconductor memory device of Claim 2, wherein:

the single data set further comprises dummy data not relevant to the write data or the read data, and

the plurality of data bits in the single data set further comprises second data bits other than the first data bits, the second data bits corresponding to the dummy data.

8. The semiconductor memory device of any one of Claims 1 to 7, wherein the

burst length corresponds to an integer that is a multiple-of-three.

9. The semiconductor memory device of any one of Claims 1 to 8, wherein a division ratio of the clock divider corresponds to an integer that is not a power-of-two.

10. The semiconductor memory device of Claim 9, wherein the division ratio of the clock divider corresponds to an integer that is a multiple-of-three.

11. The semiconductor memory device of any one of Claims 1 to 10, wherein a value obtained by dividing a period of the second command clock signal by a period of the data clock signal corresponds to an integer that is not a power-of-two.

12. The semiconductor memory device of Claim 11, wherein the value obtained by dividing the period of the second command clock signal by the period of the data clock signal corresponds to an integer that is a multiple-of-three.

13. The semiconductor memory device of any one of Claims 1 to 10, wherein a value obtained by dividing a period of the first command clock signal by a period of the data clock signal corresponds to an integer that is a power-of-two.

14. The semiconductor memory device of any one of Claims 1 to 13, further comprising:

a data processing path between the memory cell array and the plurality of data I/O pins, and

wherein the data processing path is configured to operate based on the second

command clock signal and the data clock signal.

15. The semiconductor memory device of any one of Claims 1 to 4, wherein the burst length is twenty-four (24), the number of the plurality of data I/O pins is twelve (12), and a number of the plurality of data bits in the single data set is two hundred eighty-eight (288).

16. A method of operating a semiconductor memory device, the method comprising:

receiving a write command or a read command; and

performing at least one of: a data write operation in which write data is stored in a memory cell array; or a data read operation in which the read data stored in the memory cell array is retrieved from the memory cell array, wherein the performing is based on the write command or the read command; and

generating a second command clock signal by dividing a first command clock signal,

wherein:

during the data write operation, the write data is received through a plurality of data input/output (I/O) pins,

during the data read operation, the read data is output through the plurality of data I/O pins,

an operation of receiving the write data and/or an operation of outputting the read data is performed based on a burst operation in which a single data set comprising a plurality of data bits is input or output through the plurality of data I/O pins based on a single command received from an external memory controller,

a number of the plurality of data I/O pins corresponds to an integer that is

not a power-of-two,

a burst length representing a unit of the burst operation corresponds to an integer that is not a power-of-two, and

the operation of receiving the write data and/or the operation of outputting the read data is performed based on the second command clock signal and a data clock signal.

17. A semiconductor memory device comprising:

a memory cell array;

a plurality of data input/output (I/O) pins configured to receive write data to be stored in the memory cell array or to output read data stored in the memory cell array;

a data processing path between the memory cell array and the plurality of data I/O pins; and

a clock divider configured to generate a second command clock signal based on a first command clock signal,

wherein:

a data write operation in which write data is stored in the memory cell array is performed based on a write command, or a data read operation in which the read data stored in the memory cell array is retrieved from the memory cell array is performed based on a read command,

an operation of receiving the write data and/or an operation of outputting the read data is performed based on a burst operation in which a single data set comprising a plurality of data bits is input or output through the plurality of data I/O pins based on a single command received from an external memory controller,

a number of the plurality of data I/O pins corresponds to an integer that is not a power-of-two,

a burst length representing a unit of the burst operation corresponds to an integer that is not a power-of-two and corresponds to an integer that is a multiple-of-three,

the plurality of data bits in the single data set comprises first data bits corresponding to the write data or the read data,

a number of the first data bits corresponds to an integer that is a power-of-two,

the memory cell array, the data processing path, and the plurality of data I/O pins are configured to operate based on a data clock signal and the second command clock signal,

a division ratio of the clock divider corresponds to an integer that is not a power-of-two and corresponds to an integer that is a multiple-of-three, and

a value obtained by dividing a period of the second command clock signal by a period of the data clock signal corresponds to an integer that is not a power-of-two and corresponds to an integer that is a multiple-of-three.