WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a substrate;

an active pattern in an upper portion of the substrate and extending in a first direction;

a gate electrode crossing the active pattern and extending in a second direction intersecting the first direction;

a first gate spacer covering a side surface of the gate electrode;

a first inhibition layer between the gate electrode and the first gate spacer; and

a gate insulating layer between the gate electrode and the active pattern,

wherein the gate insulating layer includes a high-k dielectric layer and a gate oxide layer, the gate oxide layer is between the high-k dielectric layer and the active pattern,

the gate insulating layer does not overlap with the first inhibition layer and the first gate spacer in the first direction,

the high-k dielectric layer is locally provided between the gate oxide layer and the gate electrode,

the high-k dielectric layer is not in contact with the first inhibition layer, and

the first inhibition layer prevents or suppresses the high-k dielectric layer from being deposited on the side surface of the gate electrode.

2. The semiconductor device of claim 1, wherein

the active pattern comprises a plurality of channel layers,

the plurality of channel layers are stacked on top of each other,

the gate electrode surrounds the plurality of channel layers,

each of the plurality of channel layers comprises first portions and a second portion between the first portions,

each of the first portions are vertically overlapped by the first gate spacer,

the second portion extends in the first direction and is vertically overlapped by the gate electrode, and

a thickness of each of the first portions is larger than a thickness of the second portion.

3. The semiconductor device of claim 2, wherein the gate oxide layer and the high-k dielectric layer are in a space surrounded by inner side surfaces of the first portions and a top surface of the second portion.

4. The semiconductor device of claim 3, wherein the high-k dielectric layer covers a top surface of the gate oxide layer and contacts the inner side surfaces of the first portions.

5. The semiconductor device of claim 3, wherein

the gate oxide layer conformally covers the inner side surfaces of the first portions and the top surface of the second portion, and

the high-k dielectric layer is spaced apart from the plurality of channel layers with the gate oxide layer therebetween.

6. The semiconductor device of claim 5, wherein

a top surface of the high-k dielectric layer has a first surface and a second surface,

the first surface of the high-k dielectric layer is located at a level lower than a topmost surface of the gate oxide layer,

the second surface is located at a level higher than the first surface of the high-k dielectric layer and is coplanar with the topmost surface of the gate oxide layer, and

the gate electrode protrudes toward the second portion of each of the plurality of channel layers.

7. The semiconductor device of any one of claims 3 to 6, wherein each of the inner side surfaces of the first portions is at an acute angle relative to the top surface of the second portion.

8. The semiconductor device of any one of claims 3 to 6, wherein each of the inner side surfaces of the first portions is connected to the top surface of the second portion while having a continuously changing inclination angle.

9. The semiconductor device of any one of claims 2 to 8, further comprising:

a pair of source/drain patterns, which are provided at both sides of the gate electrode;

a second gate spacer, which is vertically overlapped by the first gate spacer and each of the first portions of the plurality of channel layers, the second gate spacer being in contact with one source/drain pattern among the pair of source/drain patterns; and

a second inhibition layer between the gate electrode and the second gate spacer,

wherein the second inhibition layer is in direct contact with the gate electrode, and

the second inhibition layer prevents or suppresses the high-k dielectric layer from being deposited on the side surface of the gate electrode.

10. The semiconductor device of claim 9, wherein the second inhibition layer surrounds the second gate spacer and is in contact with one source/drain pattern among the pair of source/drain patterns.

11. The semiconductor device of claim 1, wherein a top surface of the high-k dielectric layer is at a level that is lower than or equal to a bottom surface of the first gate spacer.

12. A semiconductor device, comprising:

a substrate;

an active pattern in an upper portion of the substrate and extending in a first direction;

a gate electrode crossing the active pattern and extending in a second direction intersecting the first direction;

a first gate spacer covering a side surface of the gate electrode;

a first inhibition layer between the gate electrode and the first gate spacer; and

a gate insulating layer between the gate electrode and the active pattern,

wherein the gate insulating layer comprises a high-k dielectric layer and a gate oxide layer,

the gate oxide layer is between the high-k dielectric layer and the active pattern,

the gate insulating layer does not overlap with the first inhibition layer and the first gate spacer in the first direction,

the first inhibition layer prevents or suppresses the high-k dielectric layer from being deposited on the side surface of the gate electrode,

the high-k dielectric layer extends along a top surface of the gate oxide layer and a side surface of the first inhibition layer,

the high-k dielectric layer includes a first thickness on the top surface of the gate oxide layer and a second thickness on the side surface of the first inhibition layer,

the first thickness of the high-k dielectric layer is in a third direction crossing both the first direction and the second direction and the second thickness of the high-k dielectric layer is in the first direction, and

the first thickness of the high-k dielectric layer is larger than the second thickness of the high-k dielectric layer.

13. The semiconductor device of claim 12, wherein

the active pattern comprises a plurality of channel layers,

the plurality of channel layers are stacked on top of each other,

the gate electrode surrounds the plurality of channel layers,

each of the plurality of channel layers comprises first portions and a second portion between the first portions,

each of the first portions is vertically overlapped by the first gate spacer, the second portion extends in the first direction and is vertically overlapped by the gate electrode, and

a thickness of each of the first portions is larger than a thickness of the second portion.

14. The semiconductor device of claim 13, further comprising:

a pair of source/drain patterns, which are provided at both sides of the gate electrode;

a second gate spacer, which is vertically overlapped by the first gate spacer and each of the first portions of the plurality of channel layers, the second gate spacer being in contact with one source/drain pattern among the pair of source/drain patterns; and

a second inhibition layer between the gate electrode and the second gate spacer,

wherein the high-k dielectric layer includes a third thickness on a side surface of the second inhibition layer, and the third thickness of the high-k dielectric layer is smaller than the first thickness of the high-k dielectric layer, and

the second inhibition layer prevents or suppresses the high-k dielectric layer from being deposited on the side surface of the gate electrode.

15. The semiconductor device of claim 14, wherein the high-k dielectric layer is spaced apart from the first gate spacer and the second gate spacer with the first inhibition layer or the second inhibition layer therebetween.

16. The semiconductor device of claim 14 or claim 15, wherein the second inhibition layer surrounds the second gate spacer and is in contact with one source/drain pattern among the pair of source/drain patterns.

17. The semiconductor device of any one of claims 13 to 16, wherein the high-k dielectric layer covers the top surface of the gate oxide layer and is in contact with inner side surfaces of the first portions.

18. A semiconductor device, comprising:

a substrate;

an active pattern in an upper portion of the substrate and extending in a first direction, the active pattern including a plurality of channel layers stacked on top of each other;

a gate electrode crossing the active pattern and surrounding the plurality of channel layers, the gate electrode extending in a second direction intersecting the first direction;

a gate spacer covering a side surface of the gate electrode;

an inhibition layer between the gate electrode and the gate spacer;

a pair of source/drain patterns at both sides of the gate electrode;

a gate insulating layer between the gate electrode and each of the plurality of channel layers;

an interlayer insulating layer covering the gate electrode and the gate spacer;

active contacts, the active contacts penetrating the interlayer insulating layer and being connected respectively to the pair of source/drain patterns; and

a gate contact penetrating at least a portion of the interlayer insulating layer and connecting to the gate electrode, wherein

the gate insulating layer includes a high-k dielectric layer and a gate oxide layer,

the gate oxide layer is between the high-k dielectric layer and each of the plurality of channel layers,

the gate insulating layer does not overlap with the inhibition layer and the gate spacer in the first direction,

the high-k dielectric layer is locally provided between the gate oxide layer and the gate electrode,

the high-k dielectric layer is not in contact with the inhibition layer, and

the inhibition layer prevents or suppresses the high-k dielectric layer from being deposited on the side surface of the gate electrode.

19. The semiconductor device of claim 18, wherein

each of the plurality of channel layers has a pillar shape crossing the gate electrode and extending in the first direction, and

a cross section of each of the plurality of channel layers is circular, elliptical or rectangular.

20. The semiconductor device of claim 18, wherein

each of the plurality of channel layers comprises first portions and a second portion between the first portions,

each of the first portions is vertically overlapped by the gate spacer,

the second portion extends in the first direction and is vertically overlapped by the gate electrode, and

a thickness of each of the first portions is larger than a thickness of the second portion.