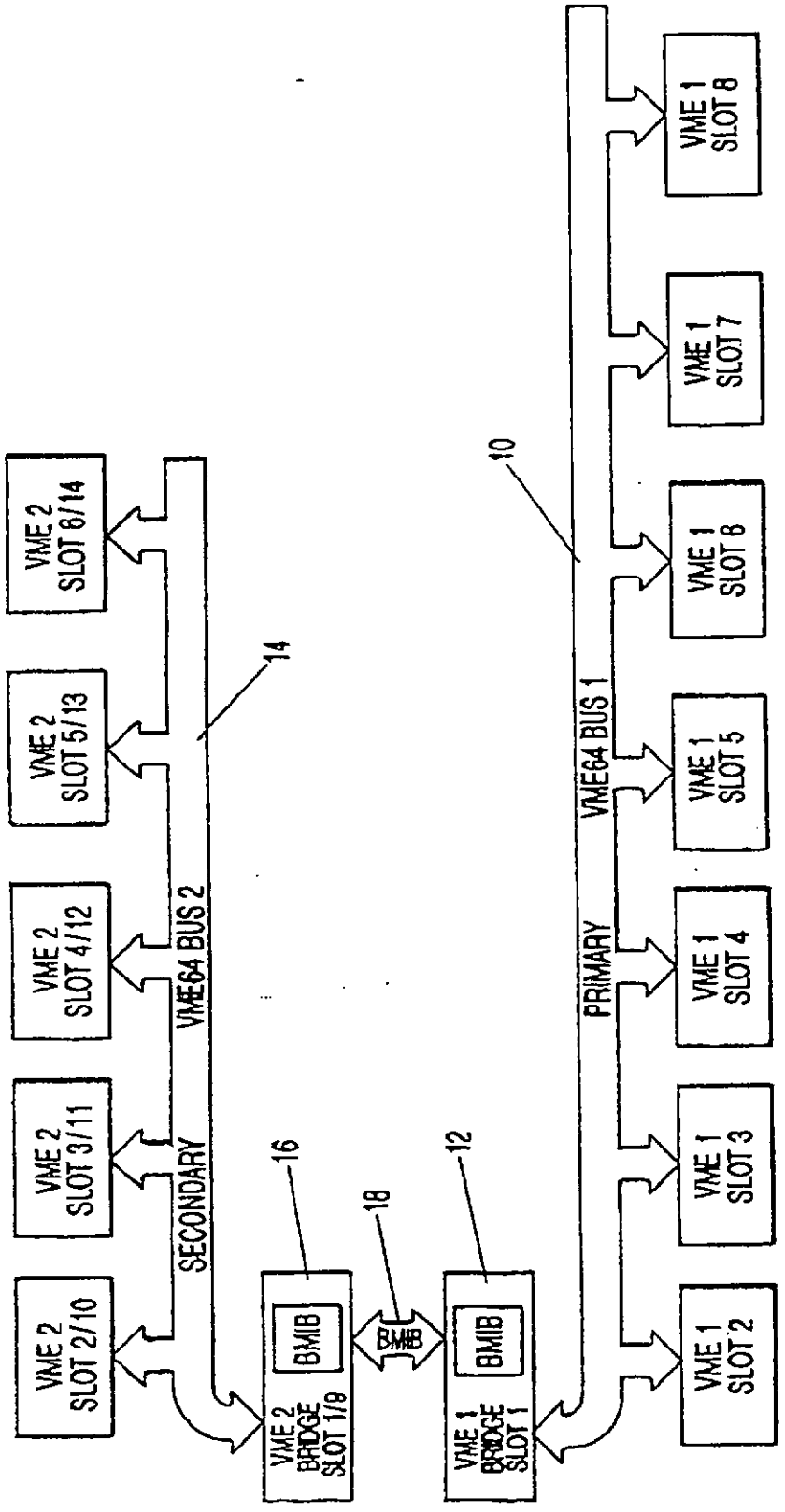

VME 2 SLOT 6/14
VME 2 SLOT 5/13
VME 2 SLOT 4/12
VME 2 SLOT 3/11
VME 2 SLOT 2/10
14
VME64 BUS 2
SECONDARY
16
VME 2 BRIDGE SLOT 1/9
BMIB
18
BMIB
12
VME 1 BRIDGE SLOT 1
BMIB
10
PRIMARY
VME64 BUS 1
VME 1 SLOT 8
VME 1 SLOT 7
VME 1 SLOT 6
VME 1 SLOT 5
VME 1 SLOT 4
VME 1 SLOT 3
VME 1 SLOT 2

FIG-1

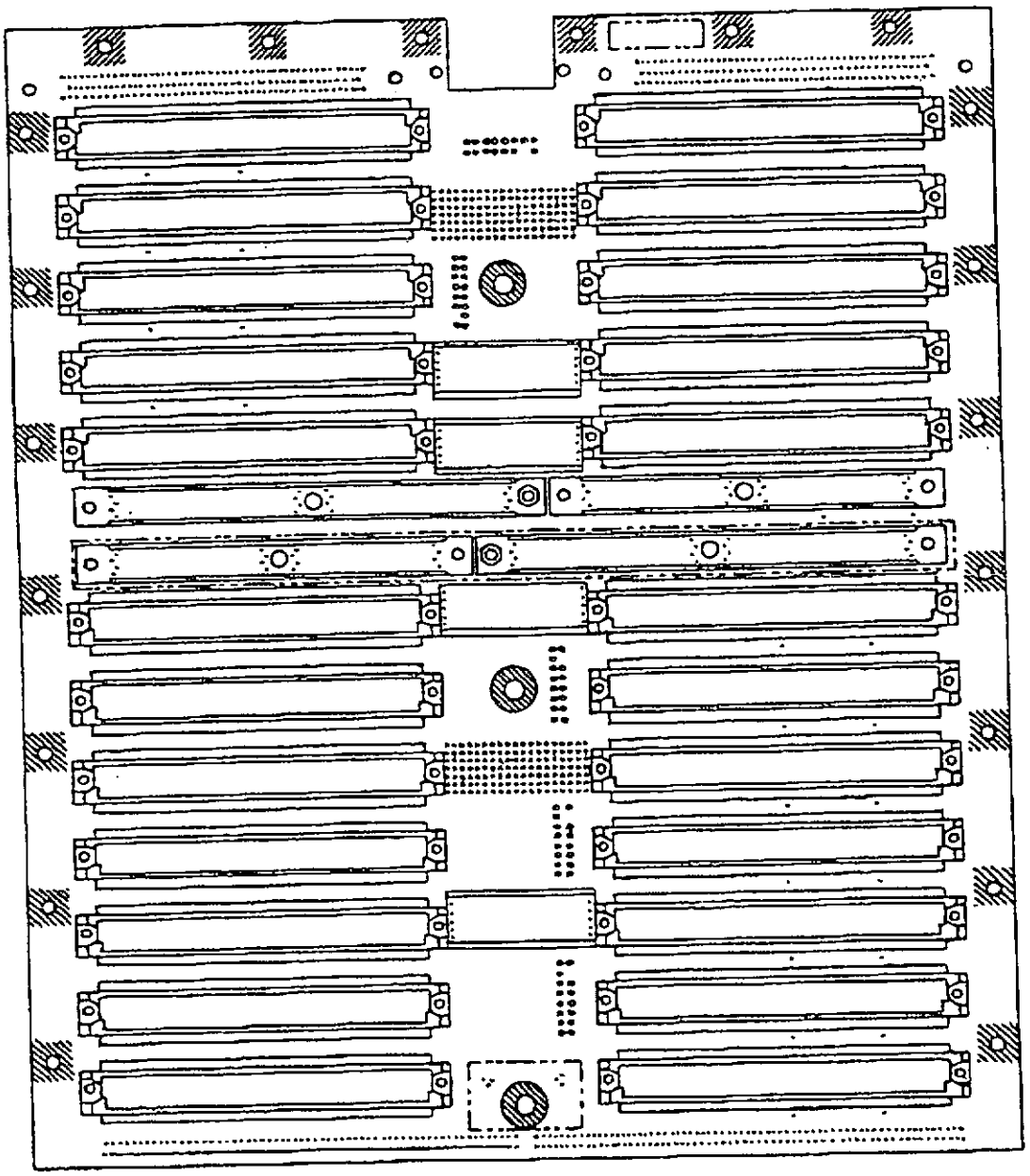


FIG-2

17 MAY 200

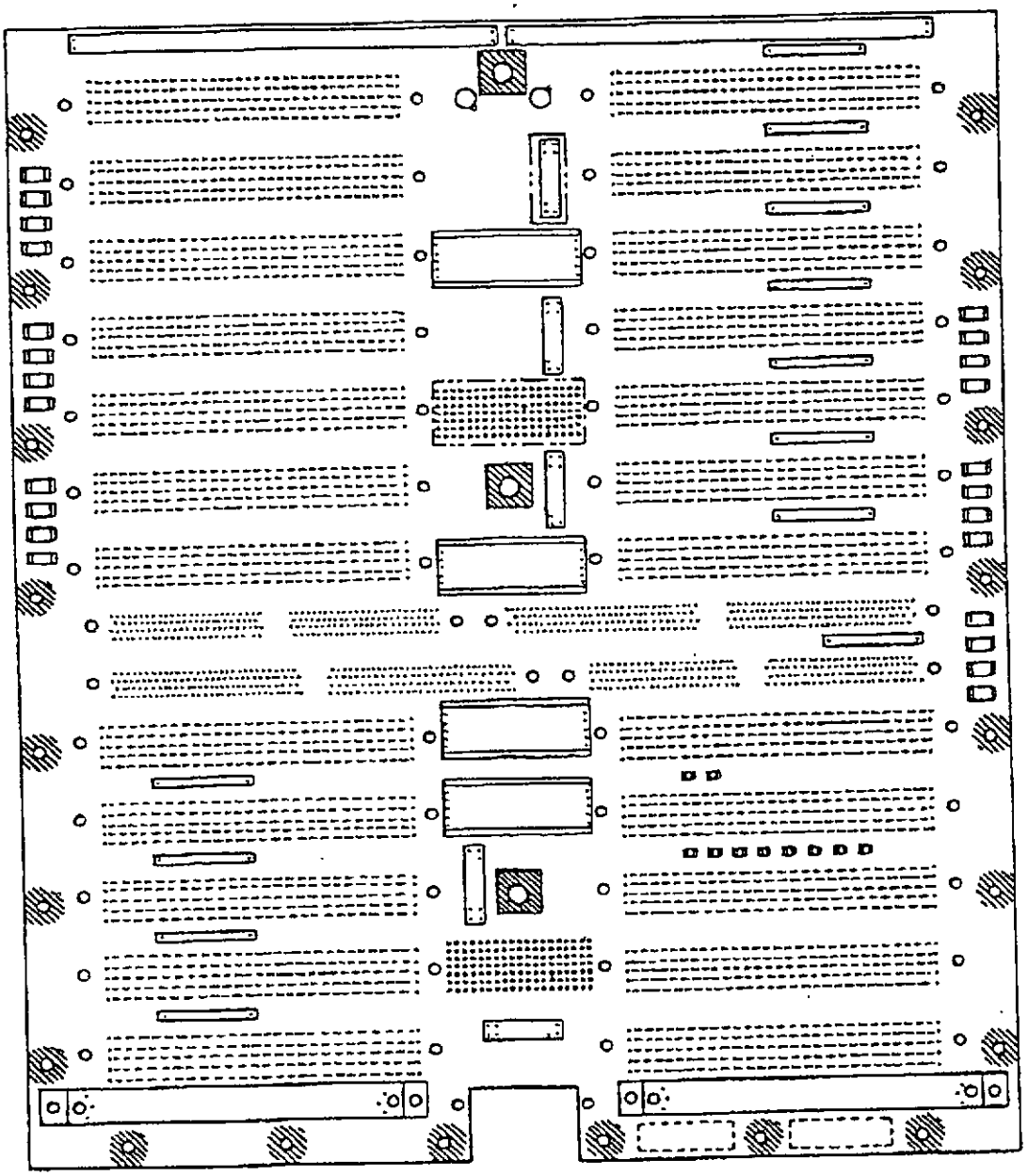


FIG-3

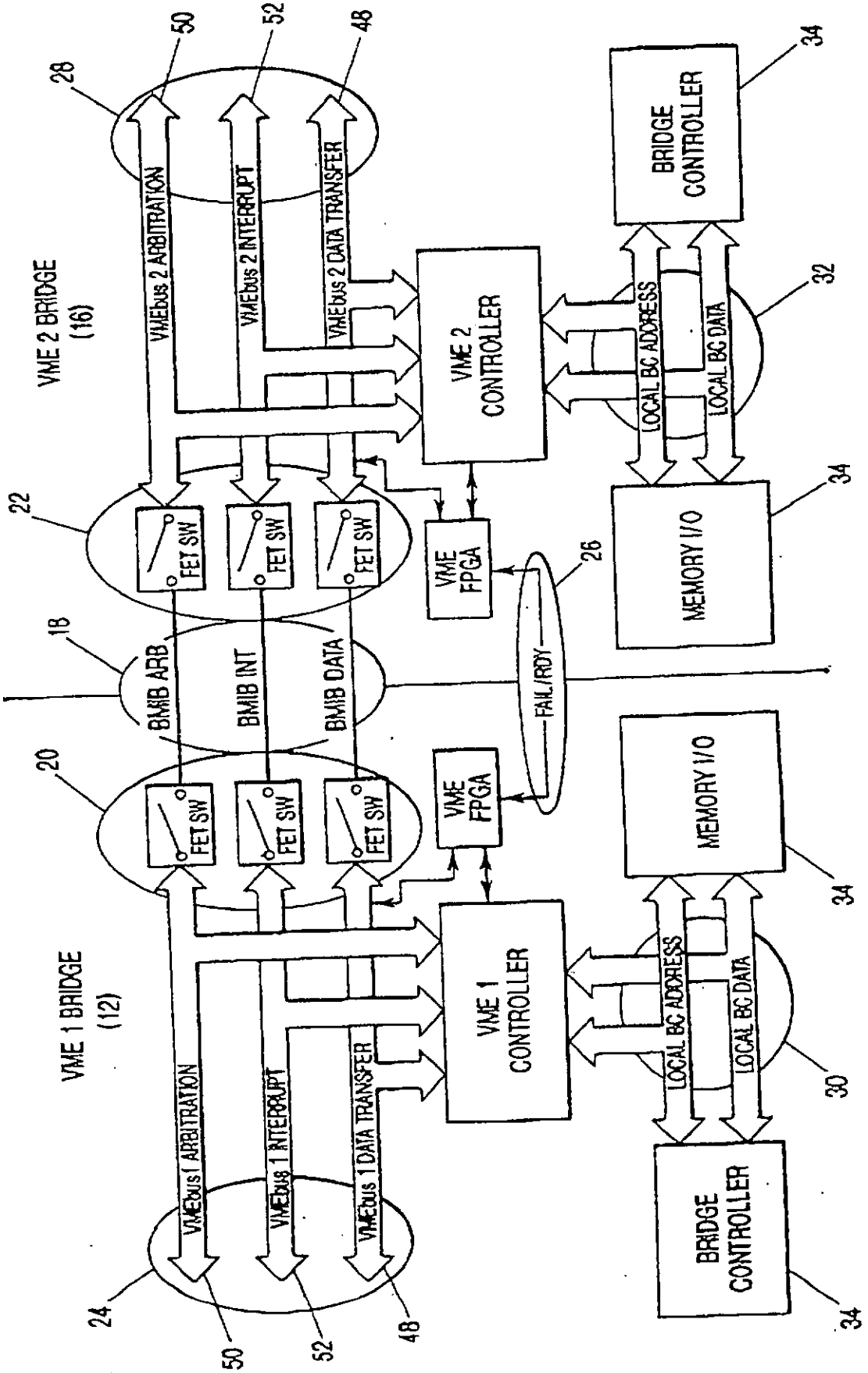

VME 2 BRIDGE (16)
VME 1 BRIDGE (12)
VMEbus 2 ARBITRATION
VMEbus 2 INTERRUPT
VMEbus 2 DATA TRANSFER
VMEbus 1 ARBITRATION
VMEbus 1 INTERRUPT
VMEbus 1 DATA TRANSFER
FET SW
BMIB ARB
BMIB INT
BMIB DATA
VME FPGA
FAIL/RDY
VME 2 CONTROLLER
VME 1 CONTROLLER
LOCAL BC ADDRESS
LOCAL BC DATA
BRIDGE CONTROLLER
MEMORY I/O
28
50
52
48
22
18
20
24
26
32
34
30

FIG-4

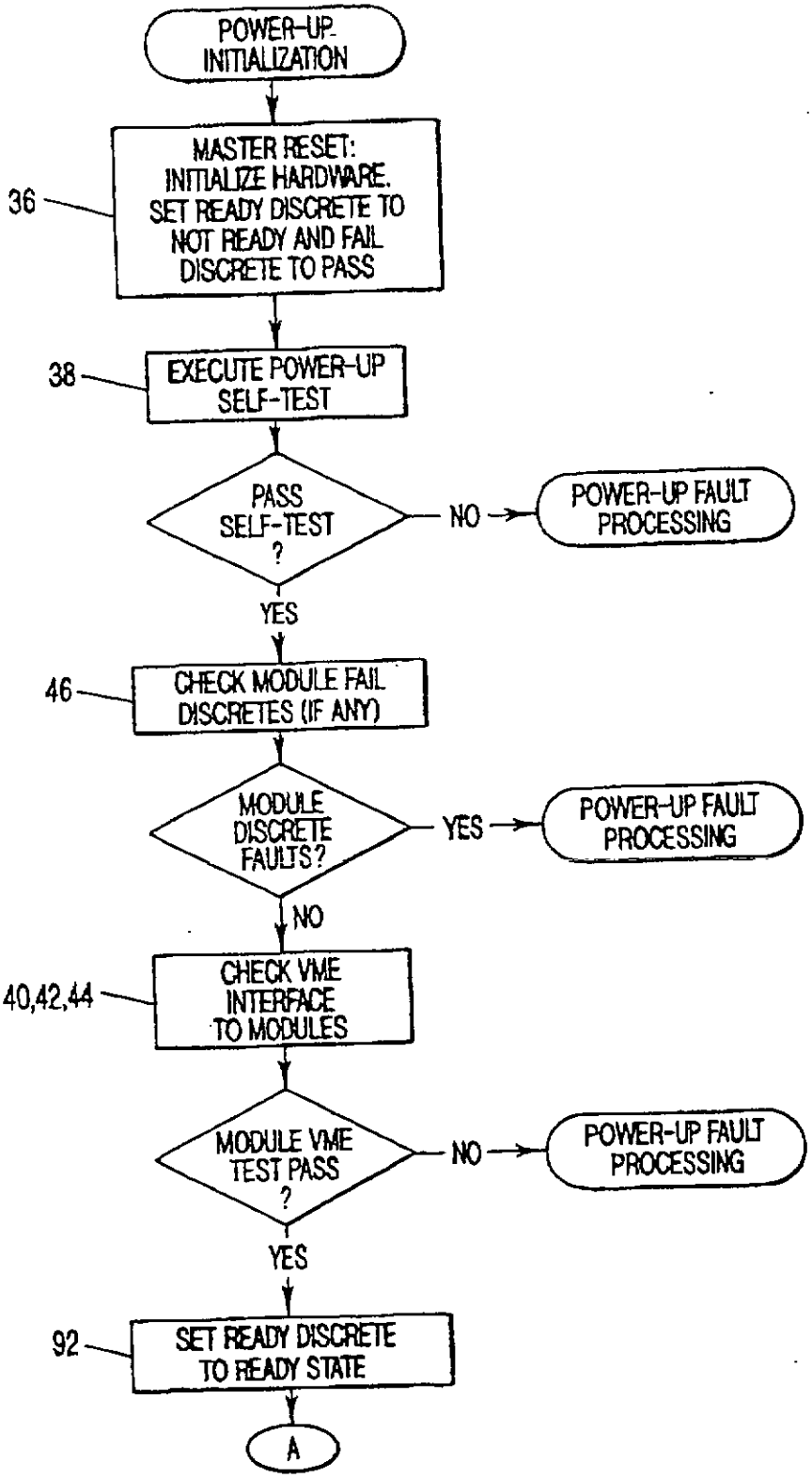

POWER-UP INITIALIZATION
MASTER RESET: INITIALIZE HARDWARE. SET READY DISCRETE TO NOT READY AND FAIL DISCRETE TO PASS
36
EXECUTE POWER-UP SELF-TEST
38
PASS SELF-TEST ?
NO
POWER-UP FAULT PROCESSING
YES
CHECK MODULE FAIL DISCRETES (IF ANY)
46
MODULE DISCRETE FAULTS?
YES
POWER-UP FAULT PROCESSING
NO
CHECK VME INTERFACE TO MODULES
40,42,44
MODULE VME TEST PASS ?
NO
POWER-UP FAULT PROCESSING
YES
SET READY DISCRETE TO READY STATE
92
A

FIG-5a

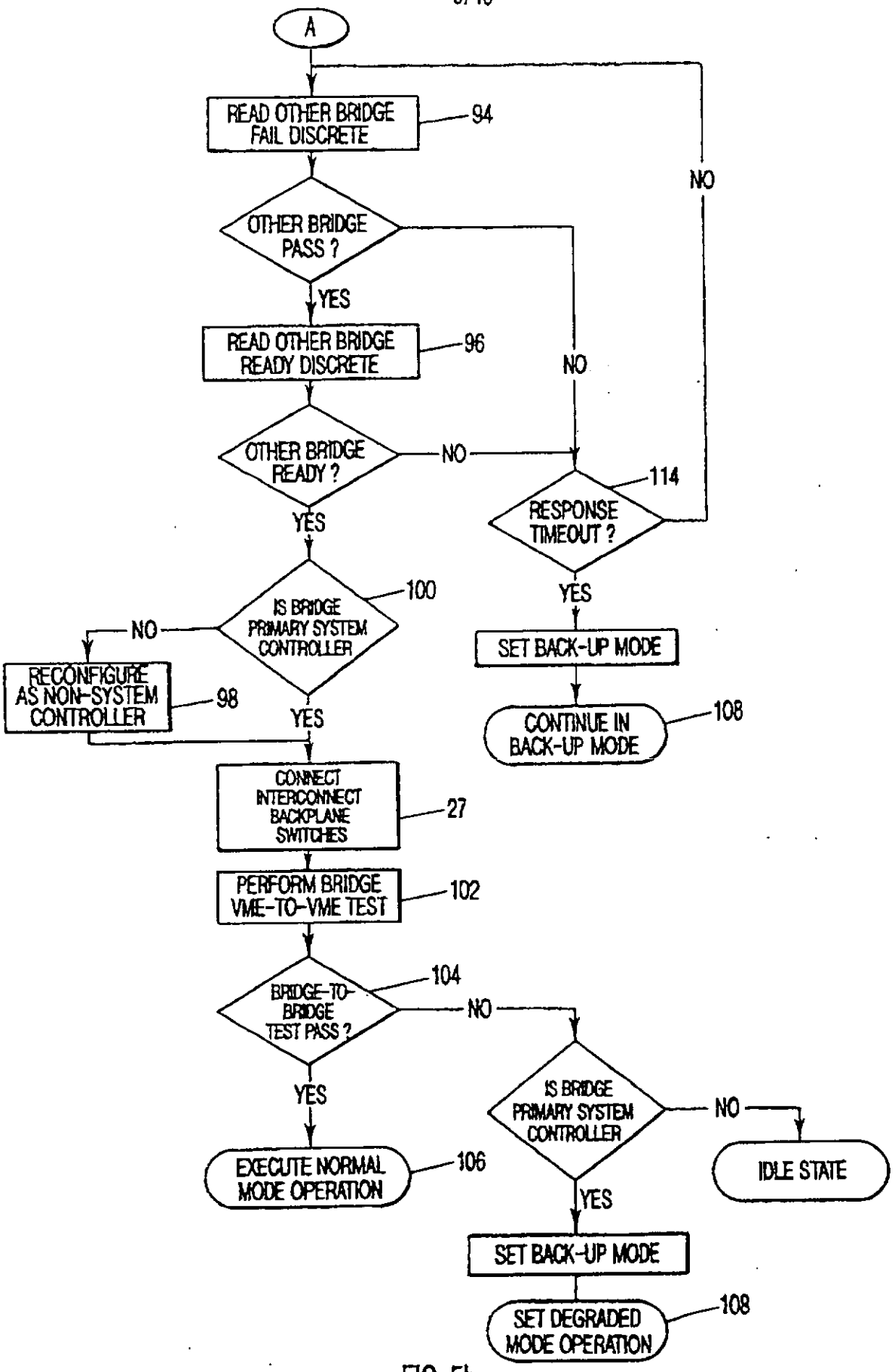

A
READ OTHER BRIDGE FAIL DISCRETE
94
OTHER BRIDGE PASS ?
NO
YES
READ OTHER BRIDGE READY DISCRETE
96
NO
OTHER BRIDGE READY ?
NO
114
RESPONSE TIMEOUT ?
YES
YES
IS BRIDGE PRIMARY SYSTEM CONTROLLER
100
NO
SET BACK-UP MODE
RECONFIGURE AS NON-SYSTEM CONTROLLER
98
YES
CONTINUE IN BACK-UP MODE
108
CONNECT INTERCONNECT BACKPLANE SWITCHES
27
PERFORM BRIDGE VME-TO-VME TEST
102
BRIDGE-TO-BRIDGE TEST PASS ?
104
NO
YES
IS BRIDGE PRIMARY SYSTEM CONTROLLER
NO
EXECUTE NORMAL MODE OPERATION
106
IDLE STATE
YES
SET BACK-UP MODE
SET DEGRADED MODE OPERATION
108

FIG-5b

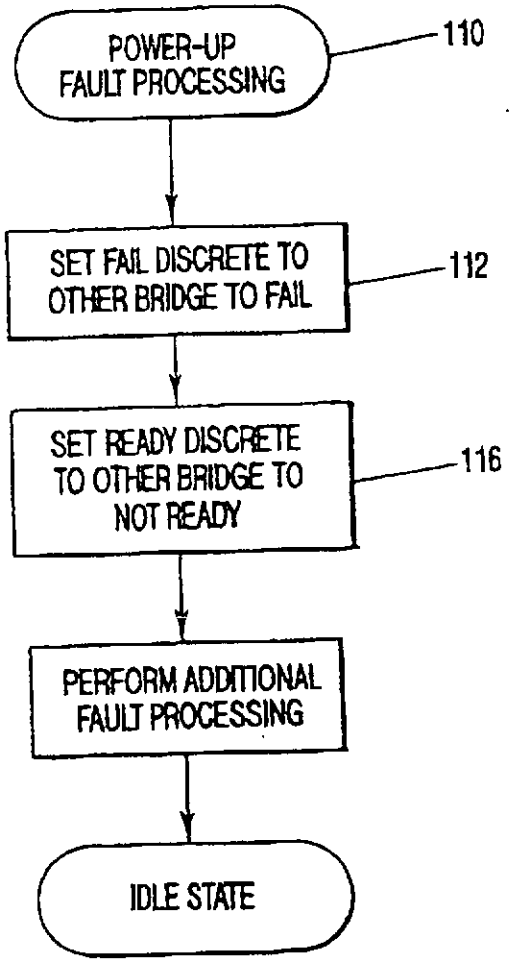

POWER-UP FAULT PROCESSING
110
SET FAIL DISCRETE TO OTHER BRIDGE TO FAIL
112
SET READY DISCRETE TO OTHER BRIDGE TO NOT READY
116
PERFORM ADDITIONAL FAULT PROCESSING
IDLE STATE

FIG-5c

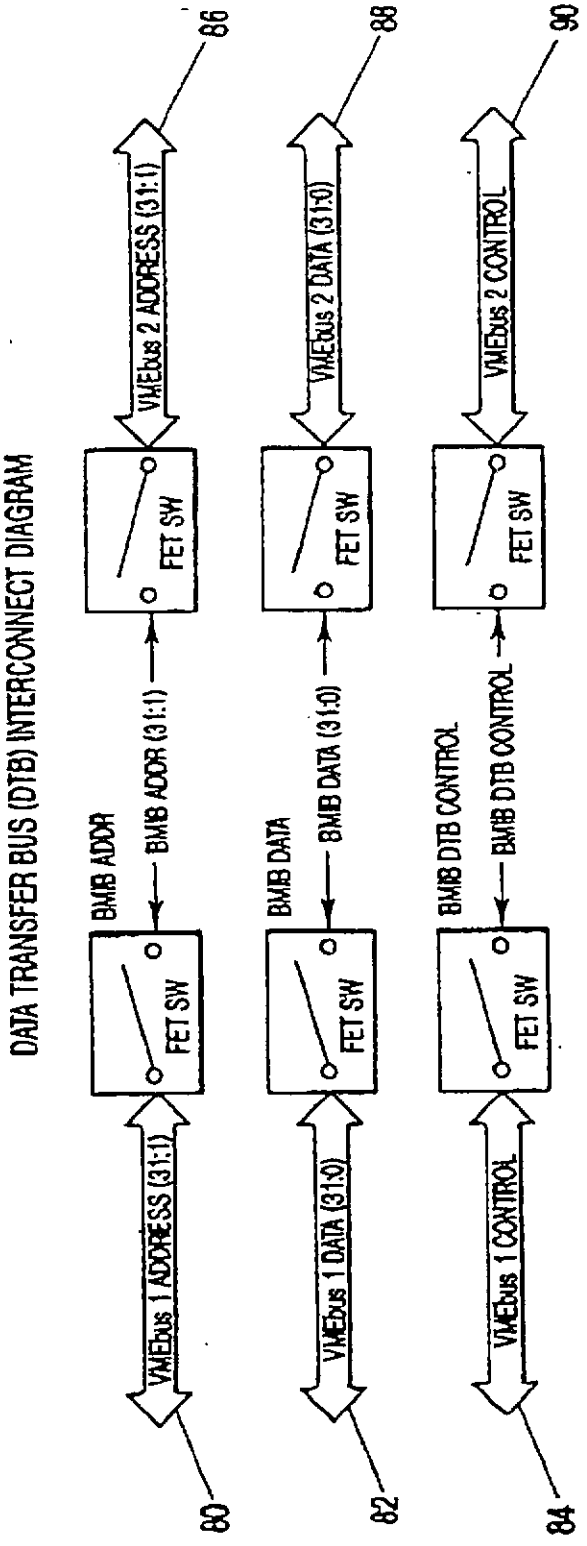

DATA TRANSFER BUS (DTB) INTERCONNECT DIAGRAM
VMEbus 1 ADDRESS (31:1)
VMEbus 1 DATA (31:0)
VMEbus 1 CONTROL
FET SW
FET SW
FET SW
BMB ADDR
BMB ADDR (31:1)
BMB DATA
BMB DATA (31:0)
BMB DTB CONTROL
BMB DTB CONTROL
FET SW
FET SW
FET SW
VMEbus 2 ADDRESS (31:1)
VMEbus 2 DATA (31:0)
VMEbus 2 CONTROL
80
82
84
86
88
90

FIG-6

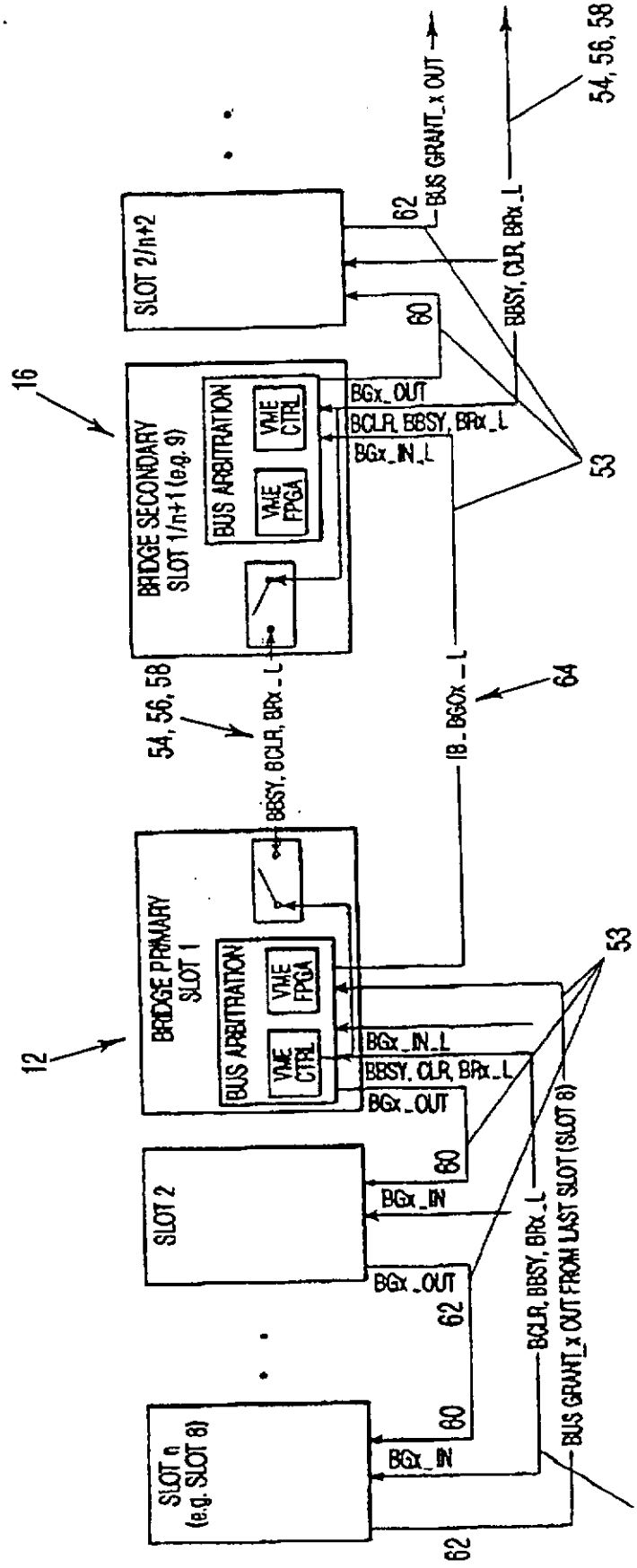

SLOT 2/n+2
62
BUS GRANT_x OUT
54, 56, 58
BBSY, CLR, BRx_L
60
16
BRIDGE SECONDARY
SLOT 1/n+1 (e.g. 9)
BUS ARBITRATION
VME CTRL
VME FPGA
BGx_OUT
BCLR, BBSY, BRx_L
BGx_IN_L
53
54, 56, 58
BBSY, BCLR, BRx_L
IB_BGOx_L
64
12
BRIDGE PRIMARY
SLOT 1
BUS ARBITRATION
VME FPGA
VME CTRL
BGx_IN_L
BBSY, CLR, BRx_L
BGx_OUT
53
SLOT 2
60
BGx_IN
BGx_OUT
62
SLOT n
(e.g. SLOT 8)
60
BGx_IN
BCLR, BBSY, BRx_L
BUS GRANT_x OUT FROM LAST SLOT (SLOT 8)
54, 56, 58
62

FIG-7

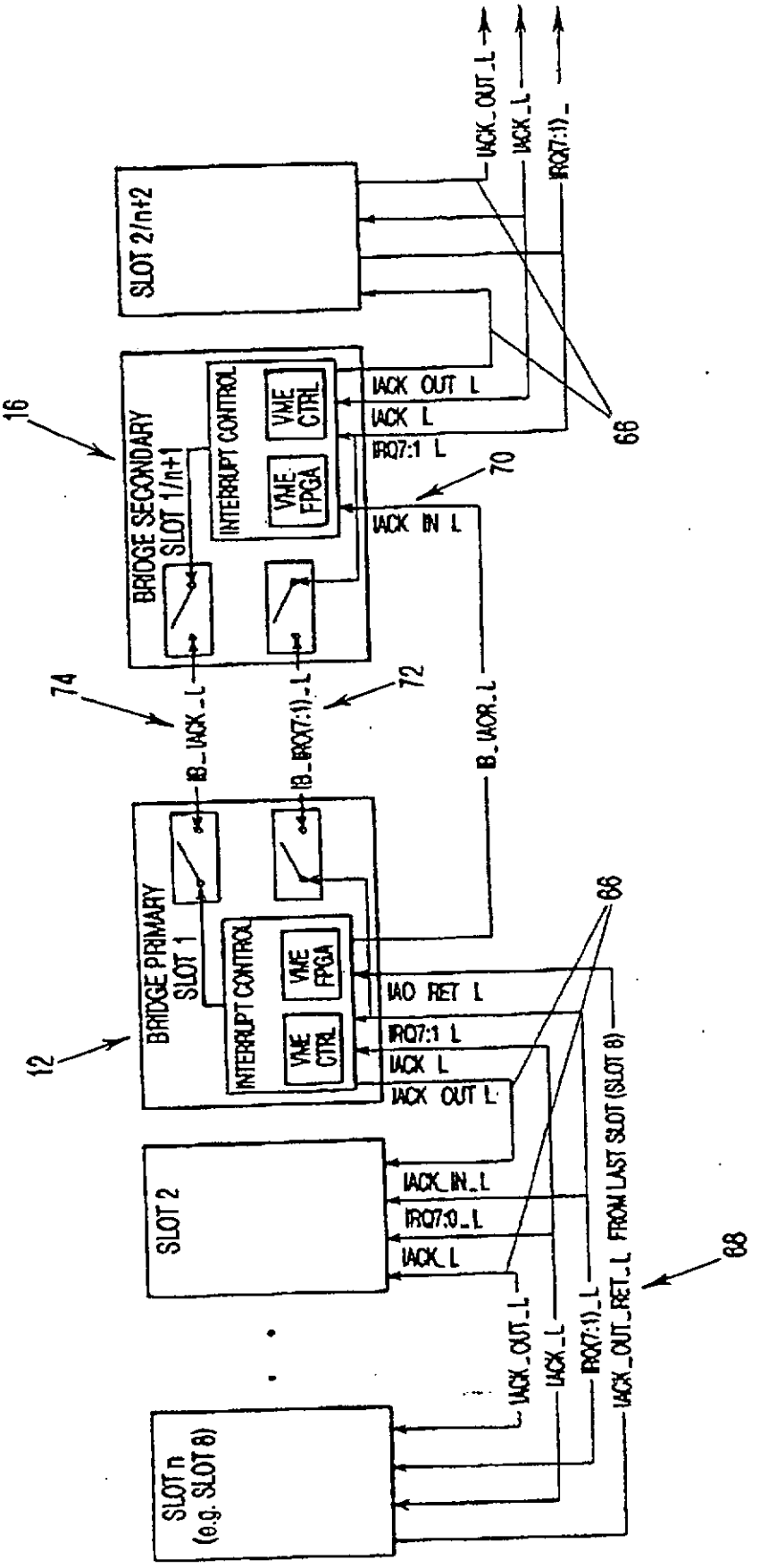

SLOT 2/n+2
IACK_OUT_L
IACK_L
IRQ7:1)_
BRIDGE SECONDARY
SLOT 1/n+1
INTERRUPT CONTROL
VME CTRL
VME FPGA
IACK OUT L
IACK L
IRQ7:1 L
IACK IN L
16
66
70
74
72
IB_IACK_L
IB_IRQ7:1)_L
B_IACKR_L
BRIDGE PRIMARY
SLOT 1
INTERRUPT CONTROL
VME FPGA
VME CTRL
IAO RET L
IRQ7:1 L
IACK L
IACK OUT L
12
SLOT 2
IACK_IN_L
IRQ7:0_L
IACK_L
IACK_OUT_L
IACK_L
IRQ7:1)_L
IACK_OUT_RET_L FROM LAST SLOT (SLOT 8)
68
SLOT n
(e.g. SLOT 8)

FIG-8