CLAIMS:

1. An electronic package, comprising:

a base substrate having a first side and a second side, the second side opposite the first side;

a component in a cavity of the base substrate, the component having a first side and a second side, the second side opposite the first side, and the component having a first sidewall and a second sidewall between the first side and the second side, the first sidewall laterally opposite the second sidewall, and wherein the cavity passes through a thickness of the base substrate and ends at the second side of the base substrate;

a first plurality of through substrate vias in the base substrate, the first plurality of through substrate vias laterally spaced apart from the first sidewall of the component;

a second plurality of through substrate vias in the base substrate, the second plurality of through substrate vias laterally spaced apart from the second sidewall of the component;

a mold layer having a first portion laterally between the first plurality of through substrate vias and the first sidewall of the component, and a second portion laterally between the second plurality of through substrate vias and the second sidewall of the component, the mold layer in contact with the first side of the component, the first sidewall of the component, and the second sidewall of the component;

a redistribution layer on the first side of the base substrate, the redistribution layer vertically over the component, vertically over the mold layer, vertically over the first plurality of through substrate vias, and vertically over the second plurality of through substrate vias;

a first plurality of interconnects coupling the first side of the component to the redistribution layer, wherein the first plurality of interconnects comprise a solder sandwiched between and in direct contact with a first plurality of pads exposed by the cavity and a second plurality of pads formed on the first side of the component;

a first die over a first portion of the redistribution layer, the first die over the first plurality of through substrate vias and over a first portion of the component;

a second plurality of interconnects coupling the first die to the first portion of the redistribution layer;

a second die over a second portion of the redistribution layer, the second die over the second plurality of through substrate vias and over a second portion of the component;

a third plurality of interconnects coupling the second die to the second portion of the redistribution layer; and

a plurality of bumps beneath the second side of the base substrate, the plurality of bumps vertically beneath the second side of the component, vertically beneath the first plurality of through substrate vias, and vertically beneath the second plurality of through substrate vias.

2. The electronic package of claim 1, wherein the first plurality of through substrate vias and the second plurality of through substrate vias have an uppermost surface at a same level as an uppermost surface of the base substrate.

3. The electronic package of claim 1, wherein the first plurality of through substrate vias and the second plurality of through substrate vias have a bottommost surface at a same level as a bottommost surface of the base substrate.

4. The electronic package of claim 1, wherein the first plurality of through substrate vias and the second plurality of through substrate vias have an uppermost surface at a same level as an uppermost surface of the base substrate, and wherein the first plurality of through substrate vias and the second plurality of through substrate vias have a bottommost surface at a same level as a bottommost surface of the base substrate.

5. The electronic package of claim 1, wherein the component has a bottommost surface at a same level as a bottommost surface of the mold layer.

6. The electronic package of claim 1, wherein the mold layer has an uppermost surface at a same level as an uppermost surface of the base substrate.

7. The electronic package of claim 1, wherein the mold layer has a bottommost surface at a same level as a bottommost surface of the base substrate.

8. The electronic package of claim 1, wherein the mold layer has an uppermost surface at a same level as an uppermost surface of the base substrate, and wherein the mold layer has a bottommost surface at a same level as a bottommost surface of the base substrate.

9. An electronic package, comprising:

a base substrate having a first side and a second side, the second side opposite the first side;

a first die in a cavity of the base substrate, and wherein the cavity passes through a thickness of the base substrate and ends at the second side of the base substrate;

a first plurality of through substrate vias in the base substrate, the first plurality of through substrate vias laterally spaced apart from a first sidewall of the first die;

a second plurality of through substrate vias in the base substrate, the second plurality of through substrate vias laterally spaced apart from a second sidewall of the first die;

a mold layer l having a first portion laterally between the first plurality of through substrate vias and the first sidewall of the first die, and a second portion laterally between the second plurality of through substrate vias and the second sidewall of the first die, the mold layer in contact with a top side of the first die, the first sidewall of the first die, and the second sidewall of the first die;

a redistribution layer on the first side of the base substrate, the redistribution layer vertically over the first die, vertically over the mold layer, vertically over the first plurality of through substrate vias, and vertically over the second plurality of through substrate vias;

a first plurality of interconnects coupling the first side of the first die to the redistribution layer, wherein the first plurality of interconnects comprise a solder sandwiched between and in direct contact with a first plurality of pads exposed by the cavity and a second plurality of pads formed on the first side of the component;

a second die over a first portion of the redistribution layer, the second die over the first plurality of through substrate vias and over a first portion of the first die;

a second plurality of interconnects coupling the second die to the first portion of the redistribution layer;

a third die over a second portion of the redistribution layer, the third die over the second plurality of through substrate vias and over a second portion of the first die;

a third plurality of interconnects coupling the third die to the second portion of the redistribution layer; and

a fourth plurality of interconnects beneath the second side of the base substrate, the fourth plurality of interconnects vertically beneath the second side of the first die, vertically beneath the first plurality of through substrate vias, and vertically beneath the second plurality of through substrate vias.

10. The electronic package of claim 9, wherein the fourth plurality of interconnects is a plurality of bumps.

11. The electronic package of claim 9, wherein the fourth plurality of interconnects is a plurality of solder balls.

12. The electronic package of claim 9, wherein the first plurality of through substrate vias and the second plurality of through substrate vias have an uppermost surface at a same level as an uppermost surface of the base substrate, and wherein the first plurality of through substrate vias and the second plurality of through substrate vias have a bottommost surface at a same level as a bottommost surface of the base substrate.

13. The electronic package of claim 9, wherein the first die has a bottommost surface at a same level as a bottommost surface of the mold layer.

14. The electronic package of claim 9, wherein the mold layer has an uppermost surface at a same level as an uppermost surface of the base substrate.

15. The electronic package of claim 9, wherein the mold layer has a bottommost surface at a same level as a bottommost surface of the base substrate.