Title

A Memory Storage Device

Technical Field

The invention concerns a memory storage device. In particular, the invention relates to a magnetic memory storage device**.**

Background of the Invention

There is a desire to increase the storage density, speed and endurance of recordable media. As the demands of speed, endurance, power and capacity on memory increase, new types of memory are required.

The discovery of new phenomena such as the magnetoresistance (MR) and giant magneto-resistive (GMR) effect have advanced the field of memory technology. These phenomena demonstrate that resistance of multilayer thin film comprised of ferromagnetic (FM) layers sandwiching a conducting or non-conductive layer is able to significantly change depending on the direction of an external magnetic field.

GMR is observable in magnetic metallic layered structures in which it is possible to orient the magnetic moments of the FM layers relative to one another. One example of a magnetic metallic layered structure consists of a layered structure of four magnetic thin films: a free magnetic layer, a non-magnetic conducting layer, a magnetic pinned layer and an exchange layer. Magnetic orientation of the pinned layer is fixed and held in place by the exchange layer. By applying an external magnetic field, the magnetic orientation of the free layer may be changed with respect to the magnetic orientation of the pinned layer. The change in the magnetic orientation generates a significant change in the resistance of the metallic layered structure. The resistance of the structure then determines the logical value to be stored.

Disk drives and Magnetic RAM (MRAM) are based on measuring magnetoresistance. MRAMs use a magneto-resistive element to store the data in a Dynamic Random Access Memory (DRAM) structure. One type of magneto-resistive element is a Magnetic Tunnel Junction (MTJ) connected with a transistor

and a metal line. Another metal line is used in the vicinity of the MTJ but not in contact with the MTJ. The MTJ consists of a magnetic pinned layer and a free magnetic layer separated by aluminum oxide which acts as an insulator. The magnetic pinned layer has a fixed orientation of magnetization. The free magnetic layer has a direction of magnetization dependent upon the direction of external magnetic field. When currents flow through the two metal lines, a magnetic field is generated.

The magnetic field generated by the current in the metal lines change the orientation of magnetization of the free magnetic layer. When the orientation of magnetization of the free magnetic layer is in the same direction as the orientation of magnetization of the magnetic pinned layer, the magnetoresistance of the MTJ is low. When the orientation of magnetization in the free magnetic layer is in the opposite to the orientation of magnetization in the magnetic pinned layer, the magnetoresistance of the MTJ is high. A high resistance state of MTJ and a low resistance of MTJ are interpreted as logic “1” and “0” respectively by associated sensing circuitry. In order to read the logical state of the MTJ, a low current is passed through the MTJ using the metal line connected with one end of the MTJ and the transistor connected to the other end of MTJ. The resultant voltage sensed by the sensing circuitry is dependent upon the magnetoresistance of the MTJ in “1” or “0” state.

Typically, MRAM uses a low coercivity magnetic material for the free magnetic layer so that the direction of magnetization in the free magnetic layer of the MTJ can be changed without requiring a high magnetic field. A high magnetic field requires a high current to pass through the metal lines which may damage the metal lines and the MTJ due to electromigration and heat. Another disadvantage of low coercivity material is that the orientation of magnetization in the free magnetic layer changes with a very low magnetic field due to current passing in neighboring lines or magnetic fields of neighboring MTJs. Another problem is that defects in the free magnetic layer may cause the orientation of magnetization to not completely change. This leads to non-functionality of the MRAM or loss of data, especially after many read/write cycles. A further problem with MRAM is that it requires at least one transistor per memory cell. The transistor is connected with the MTJ using an electrode. Increasing the size of the electrode increases the size of the memory cell in MRAM. Therefore MRAM is not capable of becoming a high density memory. Another problem with MRAM is the uniformity of the aluminum oxide

spacer between the pinned layer and free layer. It is difficult to create an aluminum oxide spacer that is completely free from defects. Non-uniformity and defects in the MTJ causes wide variations in the change in magnetoresistance between MTJs on the same chip. Therefore, large capacity MRAM has been elusive to achieve.

MRAM is unsuitable for current memory requirements due to its limited size and capacity. It also suffers from an inability to be integrated into most devices. Another reason MRAM is not commercially available is due to expensive manufacturing costs and unreliability.

Thus, a magnetic memory device without the limitation of access time or mechanical constraints of a disk drive and without the manufacturing and capacity problems of MRAM is desirable. It is therefore an object of at least one embodiment of the present invention to provide a memory device that is relatively fast and reliable. It is also advantageous that the memory device has high capacity and endurance.

Summary of the Invention

In a first preferred aspect, there is provided a memory storage device, the device comprising:

a plurality of magnetic recording bits, each recording bit storing at least one logical value;

a plurality of conducting lines to magnetize at least one recording bit when a magnetic field is induced by passing a current through the conducting lines; and

a plurality of sensors for measuring the magnetoresistance of the recording bits, each sensor corresponding to a recording bit, and where the at least one logical value stored by a recording bit is determined by the measured magnetoresistance of the recording bit;

wherein each sensor comprises a pinned layer and a sensing layer, the pinned layer having a fixed magnetic orientation and the sensing layer having a variable magnetic orientation; and wherein each recording bit comprises a recording layer having a variable magnetic orientation, the recording layer having a higher coercivity relative to the sensing layer such that the magnetic orientation of the sensing layer is stabilized by the recording layer.

Advantageously, the recording layer and the sensing layer have a relatively strong magnetic coupling to each other. This acts like a magnetization stabilizer and enables the sensing layer to maintain its magnetic orientation by being held in place or stabilized by the recording layer. This enables the memory storage device to function properly even though defects may be present in the sensing layer.

The measured magnetoresistance of the recording bit may indicate the magnetic orientation of the recording bit for determining the at least one logical value stored by the recording bit.

A spacer may be provided between the recording layer and the sensing layer.

The recording layer may be a single ferromagnetic layer. The single ferromagnetic layer may have a coercivity at least twice that of the sensing layer. The single ferromagnetic layer may have a coercivity exceeding 80 oersteds.
The recording layer may be an exchange coupled multilayer of ferromagnetic material.

The recording bit may have a single magnetic domain.

The sensor may be a Spin Valve sensor, Magnetic Tunnel Junction (MTJ) sensor, or colossal magneto-resistive (CMR) sensor to detect magnetoresistance (MR) or giant magneto-resistive (GMR) effect.

Each recording bit may be disposed between a plurality of conducting lines. Each recording bit may be disposed between at least three conducting lines.
The conducting lines may be copper conductors.

The reading and writing operation of the memory storage device may be performed and controlled by separate circuits.

The control circuits select a desired recording bit during a write operation and select a desired sensor during a read operation. The control circuits may be located externally from the sensors and the recording bits. Advantageously, active circuit elements are kept apart from the magnetic material to prevent leakage and bit to bit interference.

Advantageously, the invention eliminates the need for transistors since the read operation uses a circuitry independent of the write circuitry. Thus during a write operation, there is no need to isolate the read lines and this eliminates the need for one transistor per cell. This also improves the density and reliability of the memory storage device.

More advantageously, the present invention provides natural magnetic isolation between the memory cells because the recording bits are disposed between the conducting lines. Also, by having a corresponding sensor for each recording bit, seek time and latency time is minimised.

Mechanical components such as a spindle motor or servo are unnecessary. As a result, the memory storage device is not hindered by mechanical limitations. Thus the present invention is less likely to be damaged from shock or vibration.

Brief Description of the Drawings

An example of the invention will now be described with reference to the accompanying drawings, in which:

Figure 1 is a schematic top view of a recording bit array (not to scale);

Figure 2 is schematic bottom view of a sensor array (not to scale);

Figure 3a is a schematic top view of storage cell;

Figure 3b is a schematic cross sectional view of the storage cell of Figure 3a;

Figure 4 shows a cross sectional view of structure having sensor and recording bit array;

Figure 5a shows a cross sectional view of a sensor;

Figure 5b shows a cross sectional view of a recording bit; and

Figure 5c shows a cross sectional view of a storage cell unit having a sensor array and a recording bit.

Detailed Description of the Drawings

Referring to Figure 1, a memory storage device is provided. The device comprises a plurality of magnetic recording bits 104, a plurality of conducting lines 102 and a plurality of sensors 204. Each recording bit 104 stores at least one logical value. The conducting lines 102 magnetize at least one recording bit 104 when a magnetic field is induced by passing a current through the conducting lines 102.

The sensors 204 measure the magnetoresistance of the recording bits 104. Each sensor 204 corresponds to a recording bit 104. The at least one logical value stored by a recording bit 104 is determined by the measured magnetoresistance of the recording bit 104. Each sensor 204 comprises a pinned layer 502 and a sensing layer 504. The pinned layer 502 has a fixed magnetic orientation and the sensing layer 504 has a variable magnetic orientation. Each recording bit 104 comprises a recording layer 506 having a variable magnetic orientation. The recording layer 506 has a higher coercivity relative to the sensing layer 504 such that the magnetic orientation of the sensing layer 504 is stabilized by the recording layer 506.

The recording bits 104 are arranged into a recording bit array 100. The recording bit array 100 comprises the plurality of conducting lines 102. Magnetic recording bits 104 are disposed between the conducting lines 102. A control circuit (not shown) selects a specific recording bit 104 from the recording bit array 100. A current is passed through the conducting lines 102 to induce a magnetic filed which magnetizes the selected recording bit 104 to a desired magnetic orientation. The magnetic recording bits 104 have a single axis of magnetization. The magnetic orientation may be in one direction along the axis. The magnetic orientation is changed by the induced magnetic field and interpreted as a binary “1” or “0”.

Each magnetic recording bit 104 is capable of storing at least one bit of data such as a binary “1” or “0”. Each magnetic recording bit 104 is magnetically isolated from other recording bits 104 in the array 100. The recording bit 104 is a single ferromagnetic layer with a coercivity exceeding 80 oersteds. In another example, the recording bit 104 is an exchange coupled multilayer of ferromagnetic material. Each magnetic recording bit 104 is substantially the same size and preferably has a single magnetic domain.

Referring to Figure 2, a schematic bottom view of a sensor array 200 is illustrated. The sensor array 200 comprises of an array of sensors 204. The sensors 204 may be an MR, GMR, MTJ or CMR sensor or read head. Each sensor 204 of corresponds with a recording bit 104 on the recording bit array 100. The magnetoresistance measured by the sensor 204 depends on the magnetic orientation of the corresponding recording bit 104 of the recording bit array 100 illustrated in Figure 1. The magnetoresistance measured by the sensor 204 determines the logical value that is stored by the recording bit 104.

In one embodiment, the reading and writing operation is performed by two separate circuits. The write operation is performed by the recording bit array 100 and its controlling circuits. The read operation is performed by the sensor array 200 and its controlling circuits. Separating the circuits to perform reading and writing enables greater control over the circuits. This is addresses the problem of defects which usually prevent the sensing layer 504 of the sensor 204 from completely changing and maintaining its desired magnetic orientation.

The magnetic orientation of the sensing layer 504 in the sensor 204 is stabilized and held by the strong magnetic coupling between the sensing layer 504 and the recording layer 506 of the recording bit 104. The sensing layer 504 of the sensor 204 requires a weaker magnetic field to change its magnetic orientation than the magnetic field for changing the magnetic orientation of the recording layer 506 of the recording bit 104. The magnetic orientation of the sensing layer 504 is stabilized and held by the magnetic field of the recording layer 506. Therefore the magnetic orientation of the sensing layer 504 of the sensor 204 is changed after a writing operation. The changing of magnetic orientation may even be performed using a poor quality MTJ sensor 204.

Referring to Figure 3a, a top view of an individual storage cell 300 on a recording bit array (not shown) is illustrated. The cell 300 includes conductive lines 302. A magnetic recording bit 304 is disposed between the conductive lines 302. A current is passed through the conductive lines 302 to induce a magnetic field around the recording bit 304. This in turn magnetizes the recording bit 304 to a desired magnetic orientation. The magnetic recording bit 304 has a single axis of magnetization. The magnetic orientation is interpreted as a binary “1” or “0”. Figure 3b shows a cross sectional view of the storage cell 300 shown in Figure 3a. Figure 3b also shows the conductive lines 302 and magnetic recording bit 304 disposed between the conductive lines 302.

Referring to Figure 4, a cross sectional view of a magnetic storage device 400 is illustrated. The device 400 includes a sensor array 402 and a recording bit array 406. The sensor array 402 has sensors 404. The recording bit array 406 has magnetic recording bits 408 disposed between conductive lines (not shown). A current is passed through conducting lines (not shown) to induce a magnetic field. This in turn magnetizes the recording bit 408 to a desired magnetic orientation. The

magnetic recording bit 408 has a single axis of magnetization. The magnetic orientation is interpreted as a binary “1” or “0”. That is, the value stored in the recording bit 408 is either a “1” or “0”. This is detected by the sensor 304 by measuring the magnetoresistance of the recording bit 408.

Referring to Figure 5a, a cross sectional view of a sensor 500 is shown. The sensor 500 includes a pinned layer 502 and a sensing layer 504. The magnetic orientation of the pinned layer 502 is fixed. The magnetic orientation of the sensing layer 504 is variable.

Figure 5b shows a cross sectional view of a recording bit 503. The recording bit 503 has a recording layer 506. The magnetic orientation of the recording layer 506 controls the magnetic orientation of the sensing layer 504 in the sensor 500. The recording bit 503 may be an exchange coupled ferromagnetic layer.

Figure 5c shows a magnetic unit cell 520 in the magnetic storage device (not shown). The magnetic unit cell 520 includes sensor 500 of Figure 5a and a recording bit 503 of Figure 5b. The sensor 500 and the recording bit 503 are separated by a conductive layer 508 of the sensor 500. The conductive layer 508 may be omitted in other embodiments. The conductive layer 508 functions similarly like a router to make connection with the control circuit (not shown). The conductive layer 508 is fabricated from paramagnetic material such as tantalum. The pinned layer 502 and the sensing layer 504 of the sensor 500 form the MR, GMR or the CMR.

A write operation involves passing current through conductive lines 102 surrounding the recording bit 503 to induce a magnetic field. The induced magnetic field magnetizes the recording layer 506 of the recording bit 503 to a desired magnetic orientation. The magnetic orientation of the recording layer 506 is dependent on the logical value for storage in the recording bit 503. The recording layer 506 and the sensing layer 504 are magnetically coupled, thus the magnetic orientation of the recording layer 506 stabilizes the magnetic orientation of the sensing layer 504. If the magnetic orientation of the sensing layer 504 and the pinned layer 502 are in the same direction, the magnetoresistance is low. If the magnetic orientation of the sensing layer 504 and the pinned layer 502 are in an opposite direction to each other, the magnetoresistance is high. If a low magnetoresistance is measured, the value is determined as a logical “1”. If a high

magnetoresistance is measured, the value is determined as a logical “0”. The reading operation is performed by measuring the magnetoresistance of the sensing layer 504 and the pinned layer 502.

It is envisaged that the memory size of the storage device 400 as described may vary depending on the application. The size may range from megabits to gigabits. The memory storage device 400 may also be integrated into most devices since the active circuit elements are separate from the magnetic elements.

The physical size of the recording bit array 100 may range from a fraction of a square centimeter to several hundred square centimeters. Also the number of conducting lines for passing a current around a recording bit to magnetize the free layer in the recording bit is adjustable according to the amount of current necessary to effect magnetization of the free layer.

Although an array has been illustrated, the invention may be implemented in any shape or form. For example, the recording bits and sensors may be arranged in a circular or ellipsoidal formation.

It will be appreciated by persons skilled in the art that numerous variations and/or modifications may be made to the invention as shown in the specific embodiments without departing from the scope or spirit of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects illustrative and not restrictive.

WE CLAIM:

1. A memory storage device, the device comprising:

a plurality of magnetic recording bits, each recording bit storing at least one logical value;

a plurality of conducting lines to magnetize at least one recording bit when a magnetic field is induced by passing a current through the conducting lines; and

a plurality of sensors for measuring the magnetoresistance of the recording bits, each sensor corresponding to a recording bit, and where the at least one logical value stored by a recording bit is determined by the measured magnetoresistance of the recording bit;

wherein each sensor comprises a pinned layer and a sensing layer, the pinned layer having a fixed magnetic orientation and the sensing layer having a variable magnetic orientation; and wherein each recording bit comprises a recording layer having a variable magnetic orientation, the recording layer having a higher coercivity relative to the sensing layer such that the magnetic orientation of the sensing layer is stabilized by the recording layer.

2. The device according to claim 1, wherein the measured magnetoresistance of the recording bit indicates the magnetic orientation of the recording bit for determining the at least one logical value stored by the recording bit.

3. The device according to claim 1, wherein a spacer is provided between the recording layer and the sensing layer.

4. The device according to claim 1, wherein the recording layer us a single ferromagnetic layer.

5. The device according to claim 4, wherein the single ferromagnetic layer has a coercivity at least twice that of the sensing layer.

6. The device according to claim 4, wherein the single ferromagnetic layer has a coercivity exceeding 80 oersteds.

7. The device according to claim 1, wherein the recording layer is an exchange coupled multilayer of ferromagnetic material.

8. The device according to claim 1, wherein the recording bit has a single magnetic domain.

9. The device according to claim 1, wherein the sensor includes any one of a Spin Valve sensor, Magnetic Tunnel Junction (MTJ) sensor, or colossal magneto-resistive (CMR) sensor to detect magnetoresistance (MR) or giant magneto-resistive (GMR) effect.

10. The device according to claim 1, wherein each recording bit is disposed between the plurality of conducting lines.

11. The device according to claim 10, wherein each recording bit is disposed between at least three conducting lines.

12. The device according to claim 1, wherein the conducting lines are copper conductors to provide magnetic isolation to the recording bits.

13. The device according to claim 1, wherein a reading and writing operation of the memory storage device is performed and controlled by separate circuits.

14. The device according to claim 13, wherein for a reading operation, a control circuit selects a sensor from the plurality of sensors.

14. The device according to claim 13, wherein for a write operation, a control circuit selects a recording bit from the plurality of recording bits.

15. The device according to claim 13, wherein the separate circuits are located externally from the sensors and the recording bits.