ABSTRACT

SELECTIVE SALICIDE PROCESS BY REFORMATION OF SILICON NITRIDE SIDEWALL SPACERS

A new method of forming selective salicide structures is described whereby robust salicide structures are formed on exposed logic FET's, while blocking salicide formation on memory FET's. Thus, yielding logic FET's with robust salicide structures which exhibit low sheet rho lines and contacts, while blocking salicide formation on the sensitive memory FET's which operate at low voltage and have low leakage, shallow junctions. A conformal layer of thick silicon nitride in conjunction with a salicide blockout mask forms robust selective salicide structures. These structures exhibit low leakage and lack leakage problems caused by bridging, silicide ribbons or stringers.

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)