

PATENT SPECIFICATION

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(54) DELTA MODULATOR

(71) We, MOTOROLA, INC., a corporation of the State of Delaware, United States of America, of 5725 East River Road, Chicago, Illinois 60631, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

10 This invention relates generally to modulators for converting analogue signals to digital signals, and more particularly to delta modulators having an improved loop filter for increasing the dynamic range of the modulator within a predetermined band of frequencies.

There are many applications wherein it is necessary to provide a modulator for converting analogue signals into digital signals. One such application is in a digital voice transmission system of the privacy type wherein voice signals are converted into binary digits prior to transmission to prevent unauthorized interception of confidential messages. The binary digits generated by the modulator may be transmitted directly, or may be combined with a pseudo random bit sequence prior to transmission to increase the degree of security.

30 Several techniques for converting analogue signals to binary signals are known. One such system utilizes a delta modulator employing a single or double integrator in the feedback loop thereof to convert the analogue signal into binary digits.

Whereas this technique provides a simple way to convert an analogue signal into a digital bit stream, the distortion produced by a delta modulator, particularly a modulator utilizing a single integrator in the feedback loop, is substantial. The distortion can be reduced by increasing the bit rate or by employing a double integrator, however, increasing the bit rate increases the bandwidth of the digital signal, and the use of a double

integrator provides only a slight improvement and tends to make the modulator unstable.

According to the present invention there is provided a delta modulator for providing a digital signal at an output point thereof in response to an analogue signal having frequencies within a predetermined band applied to an input point thereof, including means for comparing said analogue signal with a second analogue signal and providing a first discrete level signal when the amplitude of said first analogue signal exceeds the amplitude of said second analogue signal, and a second discrete level signal when the amplitude of said second analogue signal exceeds the amplitude of said first analogue signal, said comparison means being connected to said input point for receiving said first analogue signal and to said output point for providing said first and second discrete level signals thereto to provide said digital signal and loop filter means having an input connected to said output point and receiving said digital signal therefrom and providing said second analogue signal in response thereto, said loop filter means including means for attenuating frequencies above and below said predetermined band to limit the bandwidth of said second analogue signal.

In a preferred embodiment of the invention, a bandpass filter provides as much attenuation as possible above and below the frequency band of the modulating signal consistent with phase shifts that do not generate undesired instabilities. The aforementioned filter may be synthesized utilizing for example, a conventional resistance-capacitance integrator in conjunction with an underdamped high pass filter. In another embodiment, several single tuned or doubled tuned bandpass filters coupled to suitable phase correcting networks may be used.

The invention will now be described by

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way of example only with particular reference to the accompanying drawings wherein:

Figure 1 shows, in block diagram form, a typical delta modulator, including a loop filter;

Figure 2 shows a circuit diagram of a single integrator type loop filter of the prior art;

Figure 2a is a graph of the amplitude characteristic of the loop filter of Figure 2;

Figure 3 is a circuit diagram of a loop filter for the delta modulator of the invention;

Figure 3a shows the amplitude characteristic of the circuit of Figure 3 relative to the amplitude characteristic of the prior art circuit of Figure 2;

Figure 4 is a block diagram of another loop filter for the delta modulator of the invention;

Figure 4a shows the amplitude characteristic of the circuit of Figure 4 and

Figure 4b is a graph of the phase characteristics of the prior art circuit of Figure 2 and the circuit of Figure 4.

Referring to Figure 1, a delta modulator has a comparator 12 having a non-inverting input connected to an analogue signal input point 10. The output of the comparator 12 is connected to an input of an amplifier 14 which has an output connected to a flip-flop 16. An enabling input of the flip-flop 16 is connected to the output of a clock 18, and the output of the flip-flop 16 is connected to a digital signal output point 20 and to a loop filter 22. The output of the loop filter 22 is connected to an inverting input of the comparator 12.

In operation, an analogue signal, such as, for example, an audio signal having a predetermined bandwidth is applied to the input point 10. The analogue input signal from point 10 is compared with the signal from the loop filter 22 by the comparator 12 which provides a signal to the amplifier 14 indicative of the difference between the analogue signals from point 10 and the loop filter 22. The signal from the comparator 12 is amplified by the amplifier 14 and used to control the state or condition of the flip-flop 16. The flip-flop 16 provides either a 1 or a 0 when a clock pulse is received thereby. Whether a 1 or an 0 is generated is determined by the signal applied to the flip-flop 16 by the amplifier 14. For example, if the signal applied to the input point 10 is greater than the signal from the loop filter 22, the signal from the amplifier 14 will cause the flip-flop 16 to provide a 1 when the next clock pulse is received. Conversely, if the signal at input point 10 is less than the signal from the loop filter 22, a 0 will be provided by the flip-flop 16. The digital signal provided by the flip-flop 16 is applied to the signal output point 20

and to the loop filter 22, which integrates the digital signal from the flip-flop 16 to provide an analogue signal to the comparator 12 for comparison with the input signal from point 10. Decoding of the digital signal from point 20 is accomplished by utilizing an integrator similar to the loop filter 22 at the receiver to regenerate the analogue signal. The clock 18 provides pulses to the flip-flop 16 at a predetermined rate, each pulse enabling the flip-flop 16 to respond to the signal from the amplifier 14 to generate either a 1 or a 0.

The performance of the delta modulator shown in Figure 1 is to a large extent determined by its dynamic range. Accordingly, the concept of dynamic range will be used to explain the relevant concepts of the instant invention, and to show the improvement over the prior art provided by the present invention. The upper limit of the dynamic range of a delta modulator at a particular modulating frequency is determined by the magnitude of the output signal from the flip-flop 16 and the effect of the loop filter 22 on the output signals from the flip-flop 16 at that particular frequency. For example, if a large amplitude signal is applied to the input point 10, a 1 having a particular amplitude is generated by the flip-flop 16. Since the 1 from the flip-flop 16 is integrated by the loop filter 22 to approximate the analogue input signal, the magnitude of the integrated signal from the loop filter 22 resulting from the integrated 1's must be sufficiently large to allow the integrated signal to follow the analogue signal applied to the input point 10. If the effect on the integrated signal caused by output 1's from the flip-flop 16 is small, the slope of the signal provided by the loop filter 22 as a result of integrating the 1's will be less than the slope of the input analogue signal, and a faithful reproduction of the input analogue signal will not be achieved. The aforesaid condition is commonly known as slope limiting or slope overload.

The lower limit of the dynamic range of a delta modulator is determined by the attenuation of the loop filter 22 to signals at one-half the clock frequency. Under conditions of no audio input, the output of a delta modulator is an idle pattern consisting of alternating 1's and 0's which, when integrated by the loop filter 22 provide the closest approximation to the zero voltage analogue signal input. Because the magnitude of the 1's is the same whether an idle pattern or modulation is present, it is desirable to provide as much attenuation as possible to the idle pattern to provide the zero approximation. The loop filter 22, which integrates the 1-0 bit stream, provides a substantially triangular waveform having a positive slope when a 1 is present and

a negative slope when a 0 is present the average value of the integrated waveform being equal to zero, and the peak-to-peak value being related to the magnitude of the signals from the flip-flop 16 and the attenuation to one-half the clock frequency provided by the loop filter 22. The integrated waveform need not be a perfect triangle and will generally be determined by the response of the loop filter used. Since the aforementioned substantially triangular waveform is applied to the comparator 12 even with no signal being applied to the input point 10, any signal applied to the input point 10 smaller than the peak-to-peak value of the triangular waveform does not appreciably affect the operation of the delta modulator, and hence signals having an amplitude smaller than the peak-to-peak value of the triangular wave from the loop filter 22 cannot be encoded. Hence, the peak-to-peak value of the triangular waveform defines the threshold, or the minimum analogue input signal necessary to interrupt the idle pattern, and difference in attenuation provided by the loop filter 22 to modulating the frequencies relative to one-half the clock frequency determines the dynamic range of the delta modulator.

In delta modulators of the prior art, the loop filter 22 generally comprises a simple resistance capacitance integrator as shown in Figure 2. Figure 2 shows the 6 db/octave amplitude characteristic of a simple integrator such as the one shown in Figure 2. If we assume that the analogue signal applied to the input point 10 is a band limited audio signal having a frequency band extending from 300 Hz to 3 KHz, and a clock frequency of 20 KHz, the difference in attenuation between 1 KHz audio signal and one-half the clock frequency, or 10 KHz is 20 db. This results in a 20 db dynamic range for the delta modulator for 1 KHz input signals when a simple integrator is used. The dynamic range decreases at 6db/octave for modulating signals in excess of 1 KHz. Reference to Figure 2a also shows the reason an increase in the clock rate results in an increase in modulator performance. For example, if the clock rate is doubled to 40 KHz, the difference in attenuation provided by the loop filter of Figure 2 between a 1 KHz modulating tone and one-half of the 40 KHz clock rate, or 20 KHz is 26 db rather than 20 db, resulting in a 6 db improvement in dynamic range. Other prior art attempts to improve dynamic range by increasing the slope of the integrator response curve by utilizing a double integrator rather than a 6 db/octave simple integrator have provided some improvement, however, substantial improvements have not been obtained. Furthermore, a double integrator may cause instability, so in practical systems,

the slope is limited to less than 12db/octave to prevent excessive phase shift which causes instability.

The dynamic range of a delta modulator can be significantly improved by utilizing a bandpass filter such as, for example, the high pass-low pass filter shown in Figure 3. The circuit of Figures 3 includes a high pass section including a capacitor 30, a resistor 32 and an inductor 34. The inductor 34 may be a passive inductor, as shown, or may be fabricated as an active inductor utilizing an active feedback network. The values of the inductor 34 and capacitor 30 are chosen to form a high pass filter having a passband beginning near the lower limit of the band of modulating frequencies, in this embodiment, approximately 300 Hz. The value of the resistor 32 is chosen to provide a slightly underdamped characteristic. The loop filter of Figure 3 also includes a low pass filter comprising a resistor 36 and a capacitor 38. The resistor 36 and capacitor 38 provides integration for the digital bit stream from the flip-flop 16 and serve to attenuate the idle pattern at one-half the clock frequency. Although Figure 3 shows a high pass filter followed by a low pass filter, the filters may be cascaded in either order to provide the desired bandpass characteristic. Furthermore, a second low pass filter may be connected in cascade with the circuit of Figure 3 to provide a double integration.

The amplitude characteristic of the filter of Figure 3 is shown in Figure 3a. The amplitude characteristic of the filter of Figure 3 is represented by the line 40, and a 6db/octave line 42 is shown to provide a comparison to the prior art integrator of Figure 2. The underdamped characteristic of the high pass filter results in the line 40 being above the line 42 within the bandwidth of the analogue signals, thereby providing a higher dynamic range within the frequency range of the modulating signal. The phase shift of the high pass filter portion of the filter of Figure 3 is opposite the phase shift of the low pass portion, thereby reducing the total phase shift of the network, and stability is maintained. Stability in a delta modulator is actually a lack of undesired instability rather than absolute stability, since the idle pattern is really a form of desired instability. Furthermore, it has been noted experimentally that the attenuation of low frequencies provided by the filter of Figure 3 results in improved modulator fidelity. It is believed that intermodulation components between harmonics of the analogue signal and the clock signal provide low frequency distortion components, which are reduced by the low frequency cut off of the loop filter according to the invention, thereby providing a further

improvement in modulator fidelity.

Referring to Figure 4, there is shown a block diagram of another embodiment of a loop filter for use in the invention utilizing a plurality of bandpass filters designed to maximize the filter response within the bandwidth of the modulating signals relative to the response above and below the modulating signal bandwidth while maintaining a phase shift consistent with modulator stability as previously defined. The circuit of Figure 4 employs a second order high pass filter 50 followed by a second order low pass filter 52 to provide a high pass-low pass combination similar to the high pass-low pass circuit of Figure 3 with the low pass portion of the circuit of Figure 3 being replaced by a second order filter rather than the resistor 36 and capacitor 38. A double tuned bandpass filter 54 is connected in parallel with the series combination of the filter 50 and 52 to enhance the response within the 650 to 1000 Hz range. A single tuned bandpass filter at 800 Hz is connected in parallel with the aforementioned filters to further enhance the response at 800 Hz. A pair of resistance-capacitance or R-C phase compensation networks 58 and 60 are connected in series with the various bandpass filters to prevent the total phase shift of the flip-flop 16 and the filter from approaching $\pm 180^\circ$. The phase shift of the flip-flop 16 must be considered because the flip-flop cannot respond until a clock pulse is received, and a random time delay is thereby introduced. The bandwidth of the R-C phase compensating networks 58 and 60 is broad compared to the bandwidth of the bandpass filters, and the parameters thereof are selected to provide the necessary overall phase characteristic with the amplitude characteristics of the filter being determined primarily by the bandpass filters. Three current summing resistors 62, 64 and 66 are employed to combine the outputs of the various bandpass filters and to provide a degree of isolation therebetween.

The amplitude characteristic of the circuit of Figure 4 is indicated by the line 70 of Figure 4a. As in Figure 3a, a 6db/octave reference line 72 is provided to show the improvement in dynamic range over a standard simple integrator. The response characteristic of the circuit of Figure 4, as shown by line 70, has been tailored to an analogue modulating signal such as an audio signal having a bandwidth of 300-3000 Hz. Note that the response of the circuit of Figure 4 drops sharply below 300 Hz and above 3 KHz, and that the response is enhanced in the 300 Hz-3 KHz range. Hence a delta modulator employing a loop filter similar to the filter shown in Figure 4 has an increased dynamic range to frequencies within the 300 Hz-3 KHz range of modulating

frequencies and a reduced response to frequencies outside of that range, thereby reducing out of band distortion and intermodulation resulting from the out of band distortion.

Figure 4a shows the phase characteristic of the circuit of Figure 4. In a delta modulator circuit as shown in Figure 1, the total phase shift of the flip-flop 16 and the loop filter 22 must not reach 180° positive nor 180° negative nor an integral multiple of 180° , if undesired oscillation (other than the idle pattern) is to be avoided. For purposes of discussion, the idle pattern is not considered to be an oscillation. The line 74 of Figure 4b shows the phase shift of the circuit of Figure 4 relative to a relatively fixed 90° phase shift of a simple integrator, as indicated by the line 76. The rapid phase transition of the phase characteristic between nearly 180° positive and nearly 140° negative allows for the steep amplitude characteristic shown in Figure 4a, but since the phase shift never reaches $\pm 180^\circ$, stability is maintained.

In this embodiment, as shown in Figure 1, because the signals from the input 10 and the signals from the loop filters 22 are applied to opposite polarity inputs of the comparator 12, and because the input connected to the loop filter 22 is an inverting input, the total phase shift of the loop filter 22 and the flip-flop 16 must be maintained within the previously mentioned $\pm 180^\circ$ limits. Should the input and feedback signals be applied to similar inputs of comparator 12, such as both inverting or both non-inverting inputs, then the necessary phase shift provided by the loop filter 22 must be adjusted accordingly, the criterion being that the loop provide negative feedback, and that phase shifts resulting in positive feedback which generates undesired oscillations be avoided. These criteria are well known in feedback theory, and simply stated, say that 0° or integral multiples of 360° phase shift around the loop must be avoided for all frequencies for which the loop gain exceeds unity. Because of the randomness of the phase shift provided by the flip-flop 16, the phase shift thereof being determined by the timing of the clock pulses relative to the modulating signal, the phase shift around the loop varies. As a result, the phase shift of the loop filter may be made very close to $\pm 180^\circ$, and the total phase shift of the flip-flop 16 and loop filter can be allowed to momentarily exceed $\pm 180^\circ$ without causing sustained oscillation. Only short periods of oscillation will occur when the total phase shift exceeds $\pm 180^\circ$. The amount of oscillation that can be tolerated is best determined by listening tests.

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WHAT WE CLAIM IS:—

1. A delta modulator for providing a digital signal at an output point thereof in response to an analogue signal having frequencies within a predetermined band applied to an input point thereof, including means for comparing said analogue signal with a second analogue signal and providing a first discrete level signal when the amplitude of said first analogue signal exceeds the amplitude of said second analogue signal, said comparison means being connected to said input point for receiving said first analogue signal and to said output point for providing said first and second discrete level signals thereto to provide said digital signal and loop filter means having an input connected to said output point and receiving said digital signal therefrom and providing said second analogue signal in response thereto, said loop filter means including means for attenuating frequencies above and below said predetermined band to limit the bandwidth of said second analogue signal.
2. A delta modulator as claimed in claim 1 wherein said loop filter means further includes means for maintaining the phase relationship between said first and second analogue signals within predetermined limits to prevent oscillation sustaining positive feedback.
3. A delta modulator as claimed in claim 2 wherein said phase relationship maintaining means includes means for preventing the phase shift between the input and the output of said loop filter means from attaining a value equal to an integral multiple of 180 degrees.
4. A delta modulator as claimed in claim 1 wherein said loop filter further includes a resistance-capacitance phase compensation circuit.
5. A delta modulator as claimed in claim 1 and including means for receiving said analogue signals, said comparison means having first and second inputs, and an output, for comparing signals applied to said inputs and providing an error signal at the output thereof in response to the difference of said analogue signals, said first input being connected to said receiving means, binary means having an input junction connected to the output of said comparison means, and an output junction, said binary means being responsive to said comparison means for providing said first discrete level signal when said error signal exceeds a predetermined magnitude and said second discrete level signal when said error signal is less than said predetermined magnitude, clock means connected to said binary means for periodically rendering said binary means responsive to said comparison means at a predetermined clock rate greater than twice the highest frequency within said predetermined band and said loop filter means having an input terminal connected to the output junction of said binary means and an output terminal connected to said second input of said comparison means, said loop filter means having a bandpass characteristic for substantially passing signals having a frequency within said predetermined band from said input terminal to said output terminal, and providing a phase shift between said input and output terminals within predetermined limits for signals having frequencies within said predetermined band to prevent oscillation sustaining positive feedback.
6. A delta modulator as claimed in claim 5 wherein said comparison means includes means for comparing the amplitudes of said analogue signal and said signals passing through said loop filter, and wherein said loop filter means has a phase shift between the input and output terminals thereof of less than $\pm 180^\circ$ to signals having frequencies within said predetermined band.
7. A delta modulator as claimed in claim 5 wherein said loop filter means includes means for attenuating signals having frequencies substantially equal to one-half of the predetermined clock rate.
8. A delta modulator as claimed in claim 1 or 7 wherein said loop filter means includes a high pass and a low pass filter connected in cascade.
9. A delta modulator as claimed in claim 8 wherein said high pass filter is an underdamped high pass filter.
10. A delta modulator as claimed in claim 9 wherein said high pass filter includes an inductor and a capacitor.
11. A delta modulator as claimed in claim 9 further including a bandpass filter connected in parallel with said cascaded combination of high pass and low pass filters.
12. A delta modulator as claimed in claim 11 further including phase correcting means for maintaining said phase shift within said predetermined limits.
13. A delta modulator as claimed in claim 12 wherein said phase correcting means includes a resistance-capacitance network.
14. A delta modulator as claimed in claim 12 further including a second bandpass filter connected in parallel with said parallel connected filter and said phase correcting means.
15. A method of providing a digital signal using the delta modulator claimed in claim 1 including the steps of sampling said analogue signal at a predetermined rate greater than twice the highest frequency within said predetermined band, sensing the level of each sample of said analogue signal and providing said first level signal for each sample that exceeds the level of the analogue



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comparison signal and providing said second level signal for each sample of magnitude less than the level of said comparison signal to generate said digital signal, filtering said digital signal to attenuate frequencies thereof both above and below said predetermined band to generate said analogue comparison signal and maintaining the phase shift between said analogue signal and said comparison signal within predetermined limits to prevent oscillation.

16. A method as claimed in claim 15 wherein the step of maintaining the phase shift within predetermined limits includes

the step of maintaining said phase shift within a predetermined range.

17. A delta modulator substantially as hereinbefore described including a loop filter substantially as described with reference to Figures 3 and 3a, or Figures 4, 4a and 4b of the accompanying drawings.

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