CLAIMS

Claim 1

A process for manufacturing a semiconductor package having a hollow chamber used for accommodating an electronic device includes:

providing a bottom substrate having a bottom plate, a ring wall and a slot, wherein the ring wall is formed on the bottom plate, the ring wall comprises a surface, wherein the ring wall and the bottom plate form the slot;

forming a first under ball metallurgy layer on the surface of the ring wall, wherein the first under ball metallurgy layer comprises a surface;

bumping a plurality of solder balls on the surface of the first under ball metallurgy layer, wherein each of the solder balls comprises a diameter, wherein a spacing is spaced apart between two adjacent solder balls, and the spacing is not smaller than half the diameter of each of the solder balls;

performing reflow soldering to the solder balls for making the solder balls melting and interconnecting to form a connection layer, wherein the connection layer covers the surface of the first under ball metallurgy layer; and

connecting a top substrate to the bottom substrate, wherein the top substrate comprises a connection surface connected to the connection layer, wherein the slot of the bottom substrate is sealed by the top substrate to form a hollow chamber.

Claim 2

The process for manufacturing a semiconductor package having a hollow chamber in accordance with claim 1, wherein the ratio between the diameter of each of the solder balls and the spacing within two adjacent solder balls ranges from 1:0.5 to 1:3.

Claim 3

The process for manufacturing a semiconductor package having a hollow chamber in accordance with claim 1 or 2, wherein the surface of the ring wall comprises a width, and the ratio between the diameter of each of the solder balls and the width of the surface of the ring wall ranges from 1:3 to 1:0.5.

Claim 4

The process for manufacturing a semiconductor package having a hollow chamber in accordance with claim 1, wherein the top substrate comprises a second under ball metallurgy layer, the second under ball metallurgy layer is formed on the connection surface, wherein when the top substrate connects to the bottom substrate, the second under ball metallurgy layer contacts the connection layer.

Claim 5

The process for manufacturing a semiconductor package having a hollow chamber in accordance with claim 4, wherein the top substrate comprises a protruding portion, and the connection surface is the surface of the protruding portion.

Claim 6

The process for manufacturing a semiconductor package having a hollow chamber in accordance with claim 1 further includes a step of coating a flux onto the connection layer prior to the step of connecting

the top substrate to the bottom substrate.

Claim 7

The process for manufacturing a semiconductor package having a hollow chamber in accordance with claim 1, wherein the ring wall of the bottom substrate comprises a plurality of corners, wherein in the step of bumping a plurality of solder balls onto the surface of the first under ball metallurgy layer, at least one solder ball is bumped at each of the corners.

Claim 8

The process for manufacturing a semiconductor package having a hollow chamber in accordance with claim 1 or 7, wherein the connection layer completely covers the surface of the first under ball metallurgy layer.

Claim 9

The process for manufacturing a semiconductor package having a hollow chamber in accordance with claim 1, wherein the surface of the ring wall comprises a width ranged between 8 μm to 500 μm.

Claim 10

The process for manufacturing a semiconductor package having a hollow chamber in accordance with claim 3, wherein the width of the surface of the ring wall ranged between 8 μm to 500 μm.