CLAIMS

1. A semiconductor structure, comprising:

a semiconductor base, comprising a logical device region and a memory region;

a bit line and an electrical contact layer disposed in a same layer as the bit line, the bit line being located on the semiconductor base in the memory region, the electrical contact layer being located on the semiconductor base in the logical device region;

a first semiconductor channel, located on a surface of the bit line, in a direction from the semiconductor base to the bit line, the first semiconductor channel comprising a first doped region, a first channel region and a second doped region that are sequentially arranged, the first doped region being in contact with the bit line;

a second semiconductor channel, disposed in a same layer as the first semiconductor channels, and located on a surface of the electrical contact layers, in a direction from the semiconductor base to the electrical contact layer, the second semiconductor channel comprising a third doped region, a second channel region and a fourth doped region that are sequentially arranged, the third doped region being in contact with the electrical contact layer;

a word line and a gate disposed in a same layer as the word line, the word line being disposed surrounding the first channel region, the gate being disposed surrounding the second channel region;

a capacitor structure, located on a side of the second doped region away from the first channel region, and in contact with the second doped region;

an electrical connection structure, located on a side of the fourth doped region away from the second channel region, and in contact with the fourth doped region; and

a dielectric layer, located between the bit line and the word line, and further located on a side of the word line away from the semiconductor base.

2. The semiconductor structure according to claim 1, wherein the semiconductor base comprises:

a semiconductor substrate;

a first semiconductor trap layer, disposed on the semiconductor substrate in the memory region, the bit line being located on a surface of the first semiconductor trap layer away from the semiconductor substrate; and

a second semiconductor trap layer, disposed on the semiconductor substrate in the logical device region, the electrical contact layer being located on a surface of the second semiconductor trap layer away from the semiconductor substrate.

3. The semiconductor structure according to claim 2, wherein an orthographic projection of the first semiconductor trap layer onto the semiconductor substrate coincide with an orthographic projection of the bit line onto the semiconductor substrate.

4. The semiconductor structure according to claim 2, wherein the logical device region comprises an NMOS region and a PMOS region; and the semiconductor base in the logical device region further comprises: an isolation structure, located between two adjacent ones of second semiconductor trap layers, and further located between two adjacent ones of electrical contact layers.

5. The semiconductor structure according to claim 1, wherein the bit line and the first semiconductor channel have a same semiconductor element, a resistivity of the bit line is less than a resistivity of the first doped region, the electrical contact layer and the second semiconductor channel have a same semiconductor element, and a resistivity of the electrical contact layer is less than a resistivity of the third doped region.

6. The semiconductor structure according to claim 5, wherein a material of the electrical contact layer is the same as a material of the bit line.

7. The semiconductor structure according to claim 6, wherein a material of the bit line comprises a metal semiconductor compound,

preferably, the semiconductor element comprises at least one of silicon, carbon, germanium, arsenic, gallium or indium; and a metal element in the metal semiconductor compound comprises at least one of cobalt, nickel, molybdenum, titanium, tungsten, tantalum or platinum; and

more preferably the second doped region comprises: a first metal contact layer, in contact

with the capacitor structure, a resistivity of the first metal contact layer being less than a resistivity of the second doped region other than the first metal contact layer; and

the fourth doped region comprises: a second metal contact layer, located in a same layer as the first metal contact layer, the second metal contact layer being in contact with the electrical connection structure, a resistivity of the second metal contact layer being less than a resistivity of the fourth doped region other than the second metal contact layer.

8. The semiconductor structure according to claim 1, wherein the first semiconductor channel constitutes a channel of a junctionless transistor; and the second semiconductor channel constitutes a channel of a junctionless transistor.

9. The semiconductor structure according to claim 8, wherein the first doped region, the first channel region and the second doped region have a same type of doped ions; and the third doped region, the second channel region and the fourth doped region have a same type of doped ions.

10. The semiconductor structure according to claim 1, wherein the word line comprises:

a first gate dielectric layer, disposed surrounding the first channel region, located on a sidewall surface of the first semiconductor channel in which the first channel region is located, and further located on a sidewall surface of the first semiconductor channel in which the second doped region is located; and

a first gate conductive layer, disposed surrounding the first channel region, and located on a sidewall surface of the first gate dielectric layer corresponding to the first channel region.

11. The semiconductor structure according to claim 10, wherein the gate comprises:

a second gate dielectric layer, located in a same layer as the first gate dielectric layer, disposed surrounding the second channel region, located on a sidewall surface of the second semiconductor channel in which the second channel region is located, and further located on a sidewall surface of the second semiconductor channel in which the fourth doped region is located; and

a second gate conductive layer, located in a same layer as the first gate conductive layer, disposed surrounding the second channel region, and located on a sidewall surface of the

second gate dielectric layer corresponding to the second channel region.

12. The semiconductor structure according to claim 1, wherein the memory region comprises a dynamic random access memory (DRAM) region, and the capacitor structure of the DRAM region comprises: a first conductive structure, in contact with the second doped region; a lower electrode layer, in contact with the first conductive structure; a capacitor dielectric layer, located on a surface of the lower electrode layer; and an upper electrode layer, located on a surface of the capacitor dielectric layer; and

the electrical connection structure comprises: a second conductive structure, located in a same layer as the first conductive structure, the second conductive structure being in contact with the fourth doped region; and a third conductive structure, in contact with a side of the second conductive structure away from the fourth doped region.

13. The semiconductor structure according to claim 12, wherein in a direction perpendicular to a surface of the semiconductor base, a depth of the lower electrode layer is the same as a depth of the third conductive structure.

14. The semiconductor structure according to claim 1, further comprising: an insulating layer, located on a surface of the dielectric layer, the capacitor structure and the electrical connection structure being located in the insulating layer, and a relative dielectric constant of a material of the insulating layer being less than a relative dielectric constant of a material of the dielectric layer.

15. The semiconductor structure according to claim 1, wherein the memory region further comprises a non-volatile memory (NVM) region; and the semiconductor structure further comprises: a free layer, a tunneling layer, and a pinned layer stacked on the second doped region of the NVM region, and the free layer is electrically connected to the second doped region of the NVM region.

16. A method for manufacturing a semiconductor structure, comprising:

providing a semiconductor base, the semiconductor base comprising a logical device region and a memory region;

forming a bit line and an electrical contact layer disposed in the same layer as the bit line, the bit line being located on the semiconductor base in the memory region, the electrical

contact layer being located on the semiconductor base in the logical device region;

forming a first semiconductor channel and a second semiconductor channel disposed in a same layer as the first semiconductor channel, the first semiconductor channel being located on a surface of the bit line, in a direction from the semiconductor base to the bit line, the first semiconductor channel comprising a first doped region, a first channel region, and a second doped region that are sequentially arranged, the first doped region being in contact with the bit line, the second semiconductor channel being located on a surface of the electrical contact layer, in a direction from the semiconductor base to the electrical contact layer, the second semiconductor channel comprising a third doped region, a second channel region, and a fourth doped region that are sequentially arranged, the third doped region being in contact with the electrical contact layer;

forming a word line and a gate disposed in the same layer as the word line, the word line being disposed surrounding the first channel region, the gate being disposed surrounding the second channel region;

forming a capacitor structure, located on a side of the second doped region away from the first channel region, the capacitor structure being in contact with the second doped region;

forming an electrical connection structure, the electrical connection structure being located on a side of the fourth doped region away from the second channel region, the electrical connection structure being in contact with the fourth doped region; and

forming a dielectric layer, the dielectric layer being located between the bit line and the word line, and being further located on a side of the word line away from the semiconductor base.

17. The manufacturing method according to claim 16, wherein providing the semiconductor base and forming the bit line, the electrical contact layer, the first semiconductor channel and the second semiconductor channel comprise:

providing an initial semiconductor base;

patterning a partial thickness of the initial semiconductor base, to form the first semiconductor channel and the second semiconductor channel; and

metallizing a remaining partial thickness of the initial semiconductor base, to convert a partial thickness of the initial semiconductor base located below the first semiconductor channel into the bit line and convert a partial thickness of the initial semiconductor base located below the second semiconductor channel into the electrical contact layer, and the remaining initial semiconductor base serving as the semiconductor base.

18. The manufacturing method according to claim 17, wherein the initial semiconductor base comprises a semiconductor substrate, an initial first semiconductor trap layer and an initial second semiconductor trap layer, the initial first semiconductor trap layer is located on the semiconductor substrate in the memory region, and the initial second semiconductor trap layer is located on the semiconductor substrate in the logical device region;

patterning the partial thickness of the initial semiconductor base comprises: patterning a partial thickness of the initial first semiconductor trap layer and a partial thickness of the initial second semiconductor trap layer, to form the first semiconductor channel and the second semiconductor channel; and

metallizing the remaining partial thickness of the initial semiconductor base comprises: metallizing a remaining partial thickness of the initial first semiconductor trap layer and a partial thickness of the initial second semiconductor trap layer.

19. The manufacturing method according to claim 18, wherein a process of the metallization comprise:

forming a barrier layer, the barrier layer covering sidewall surfaces of the first semiconductor channel and the second semiconductor channel;

forming a metal layer on surfaces of the initial first semiconductor trap layer and the initial second semiconductor trap layer;

performing annealing to convert the partial thickness of the initial first semiconductor trap layer into the bit line and convert the partial thickness of the initial second semiconductor trap layer into the electrical contact layer; and

after the bit line and the electrical contact layer are formed, removing the barrier layer and the remaining metal layer.

20. The manufacturing method according to claim 16, further comprising: metallizing an end surface of the second doped region away from the semiconductor base and an end surface of the fourth doped region away from the semiconductor base, to convert a partial thickness of the second doped region to a first metal contact layer, and convert a partial thickness of the fourth doped region to a second metal contact layer, and materials of the first metal contact layer and the second metal contact layer respectively being a metal semiconductor compound.