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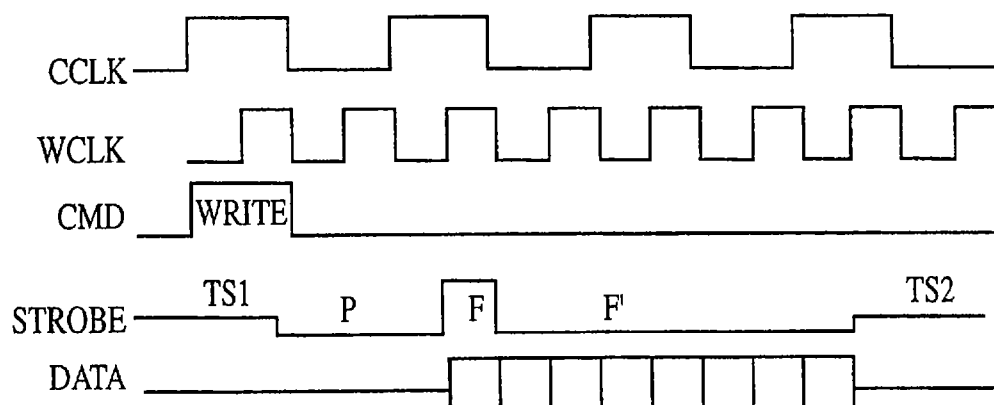
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(54) Title: SYNCHRONIZED WRITE DATA ON A HIGH SPEED MEMORY BUS



(57) Abstract: Some synchronous semiconductor memory devices accept a command clock which is buffered and a write clock which is unbuffered. Write command are synchronized to the command clock while the associated write data is synchronized to the write clock. Due to the use of the buffer, an arbitrary phase shift can exist between the command and write clocks. The presence of the phase shift between the two clocks makes it difficult to determine when a memory device should accept write data associated a write command. A synchronous memory device in accordance with the present invention utilizes the unbuffered strobe signal which is normally tristated during writes as a flag to mark the start of write data. A preamble signal may be asserted on the strobe signal line prior to asserting the flag signal in order to simplify flag detection.

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