FIG. 1A

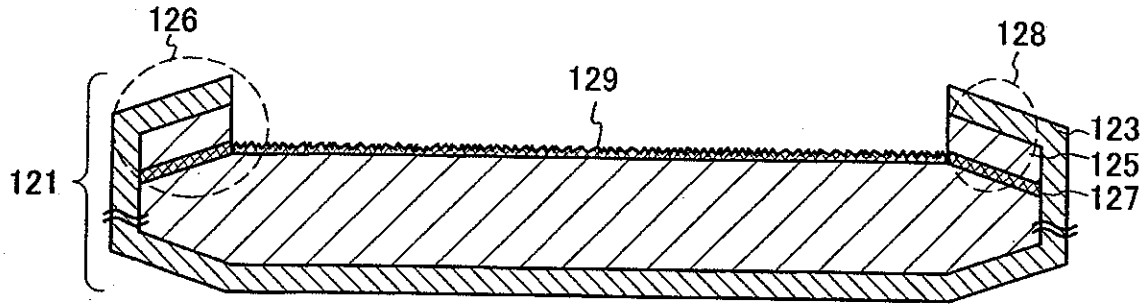


FIG. 1B

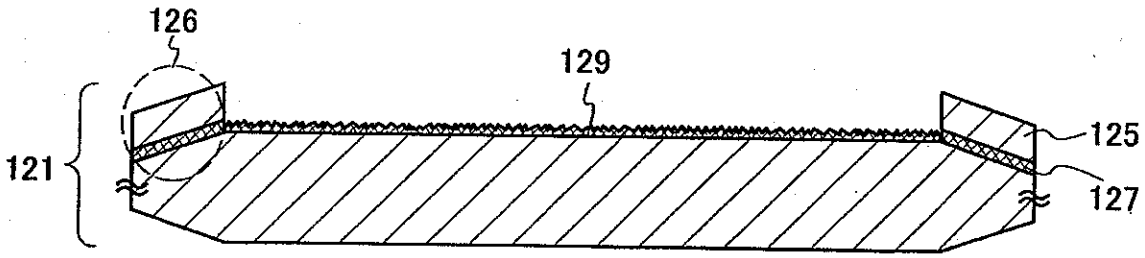


FIG. 1C

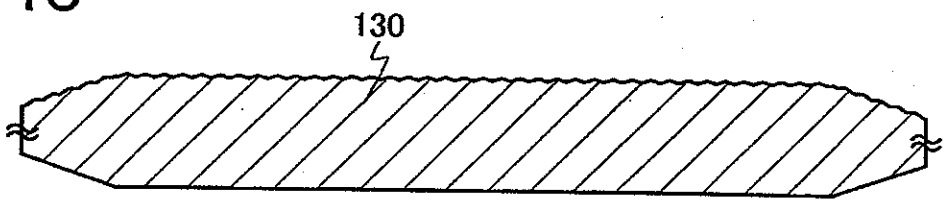


FIG. 1D

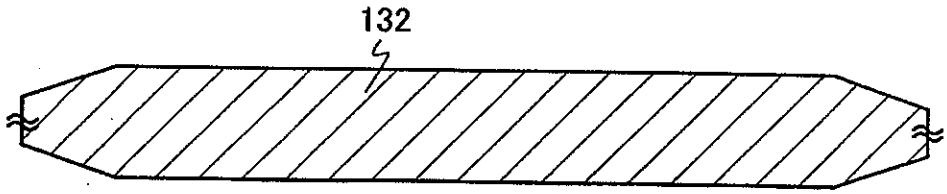


FIG. 2A

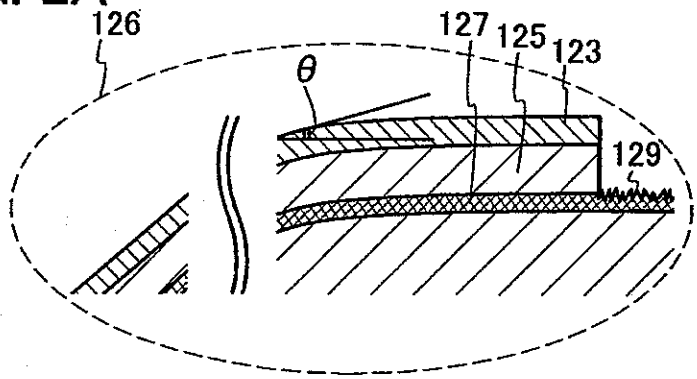


FIG. 2B

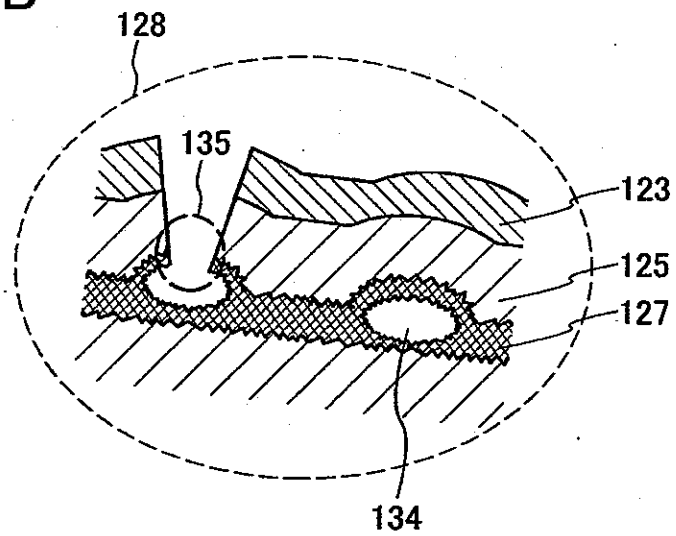


FIG. 3A

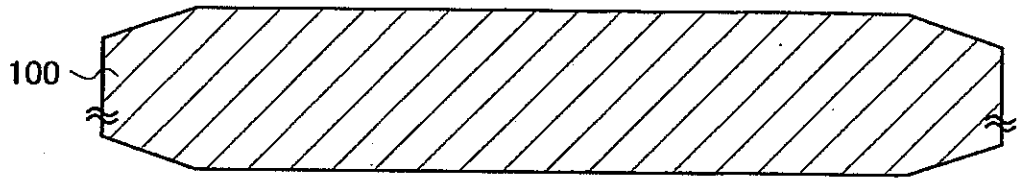


FIG. 3B

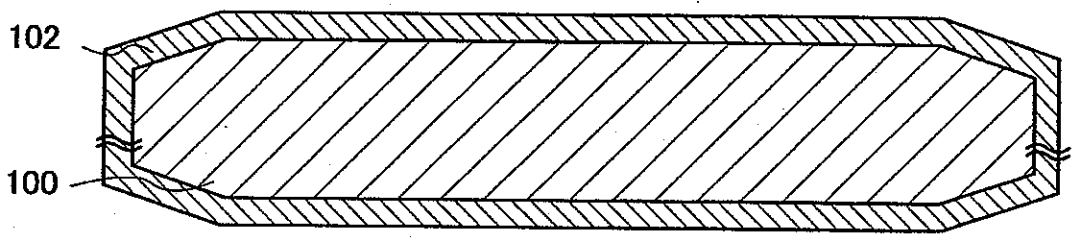


FIG. 3C

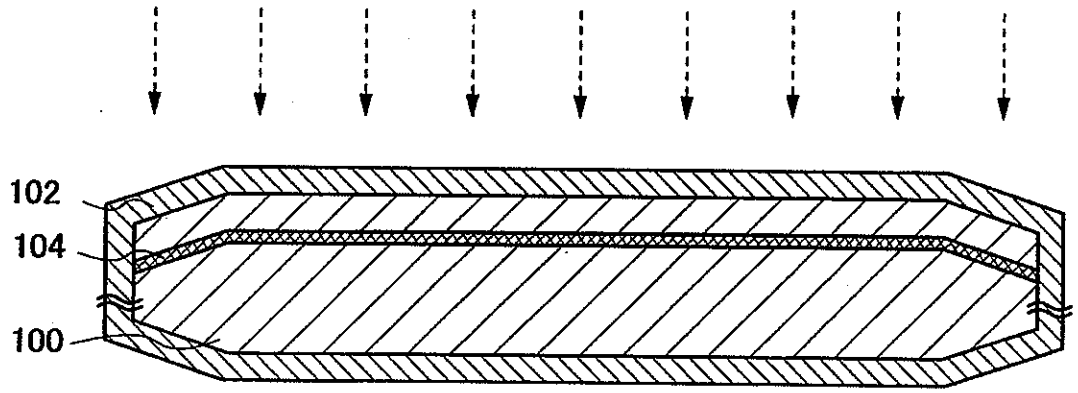


FIG. 4A

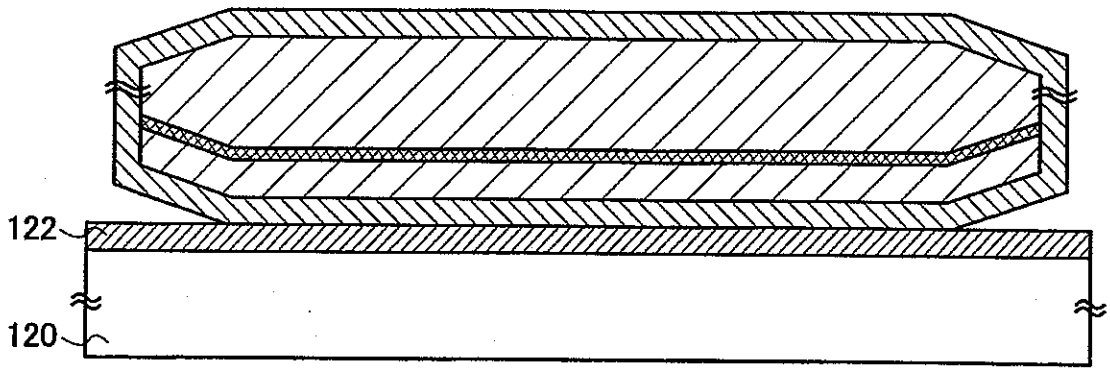


FIG. 4B

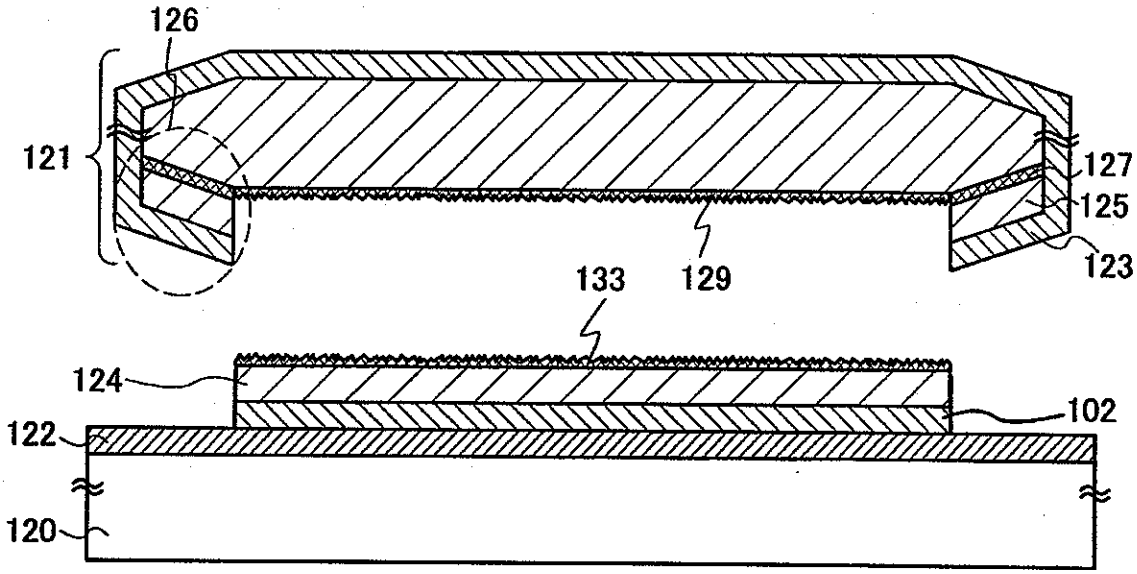


FIG. 4C

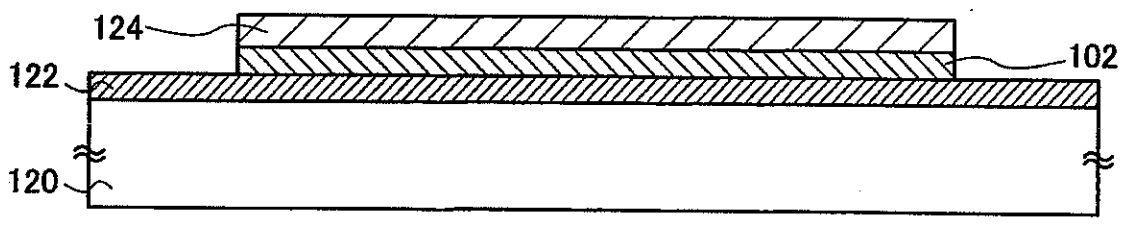


FIG. 5A

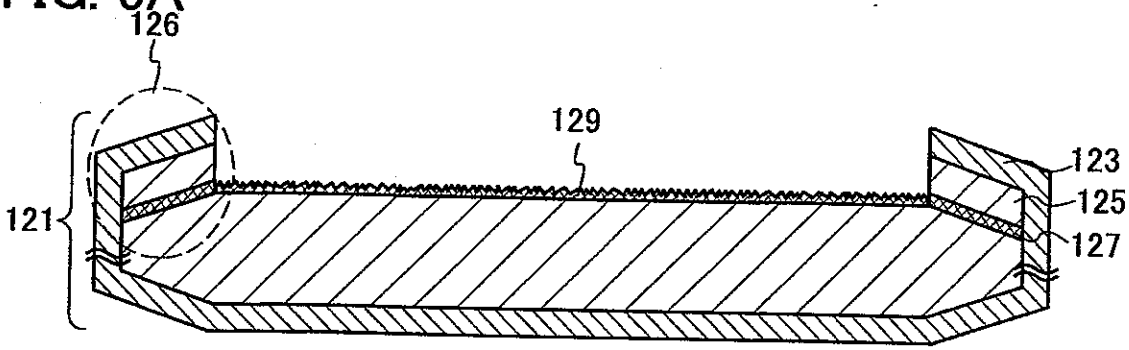


FIG. 5B

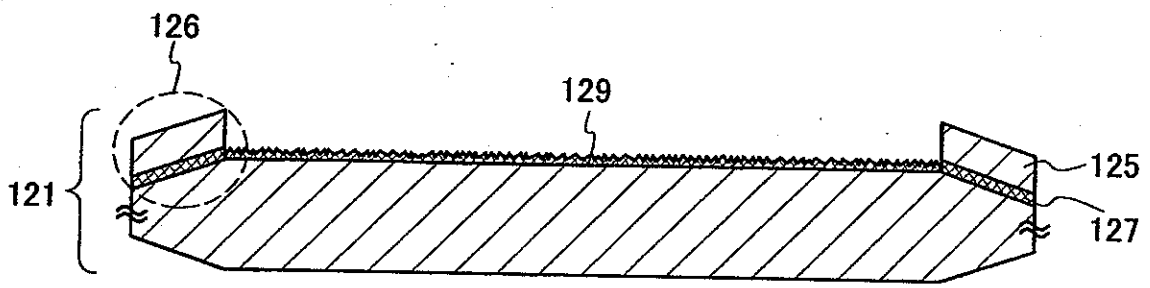


FIG. 5C

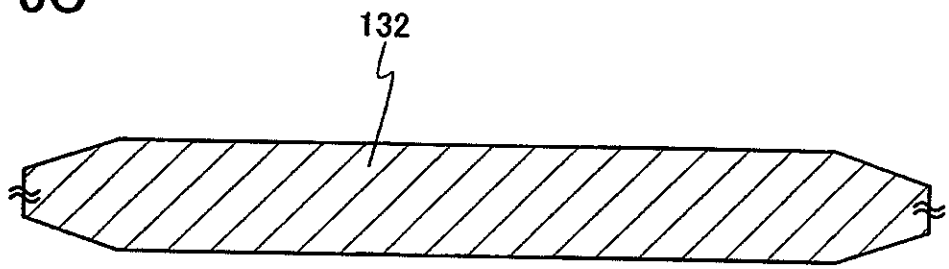


FIG. 6

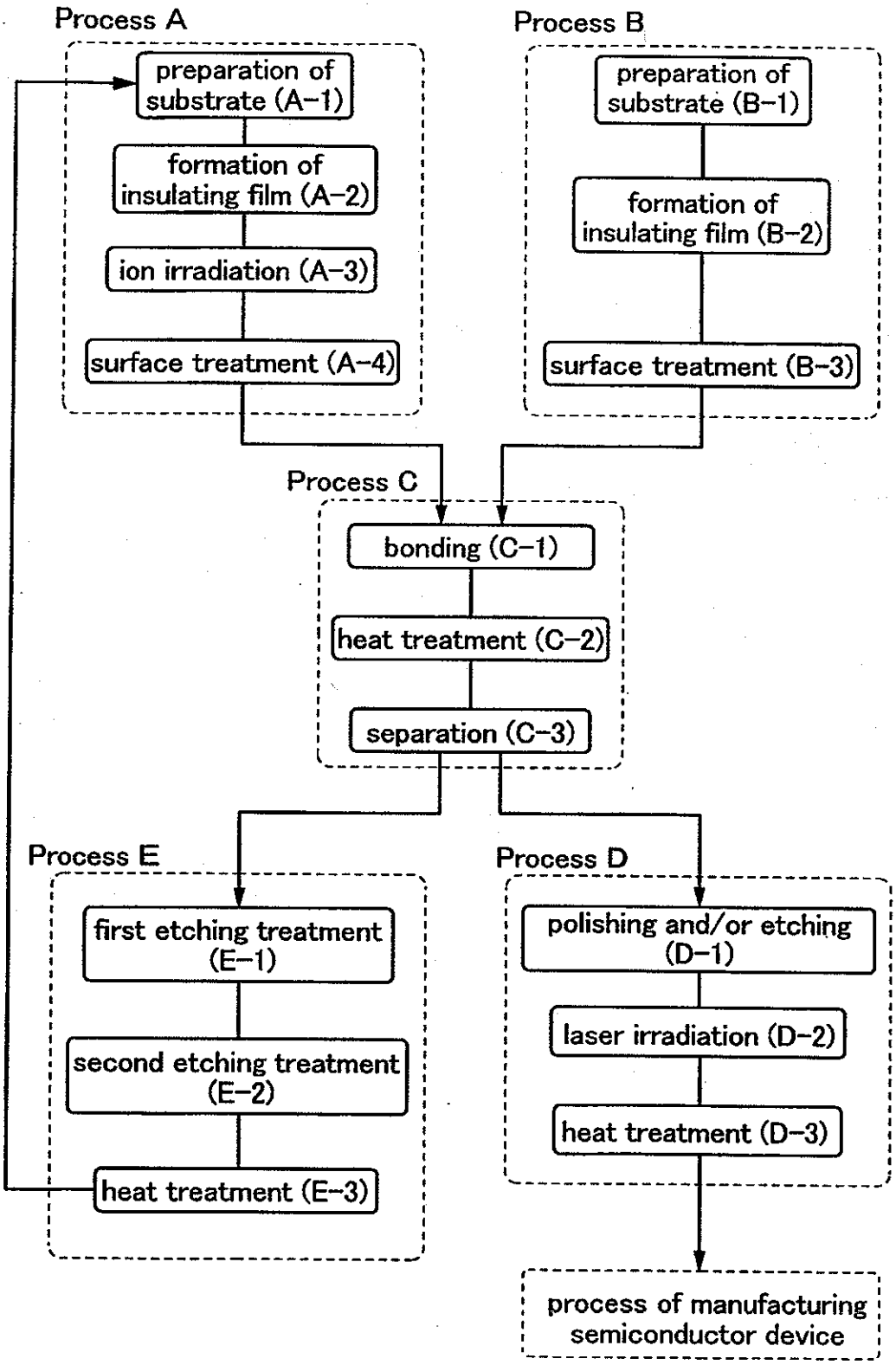

Process A
preparation of substrate (A-1)
formation of insulating film (A-2)
ion irradiation (A-3)
surface treatment (A-4)
Process B
preparation of substrate (B-1)
formation of insulating film (B-2)
surface treatment (B-3)
Process C
bonding (C-1)
heat treatment (C-2)
separation (C-3)
Process E
first etching treatment (E-1)
second etching treatment (E-2)
heat treatment (E-3)
Process D
polishing and/or etching (D-1)
laser irradiation (D-2)
heat treatment (D-3)
process of manufacturing semiconductor device

FIG. 7

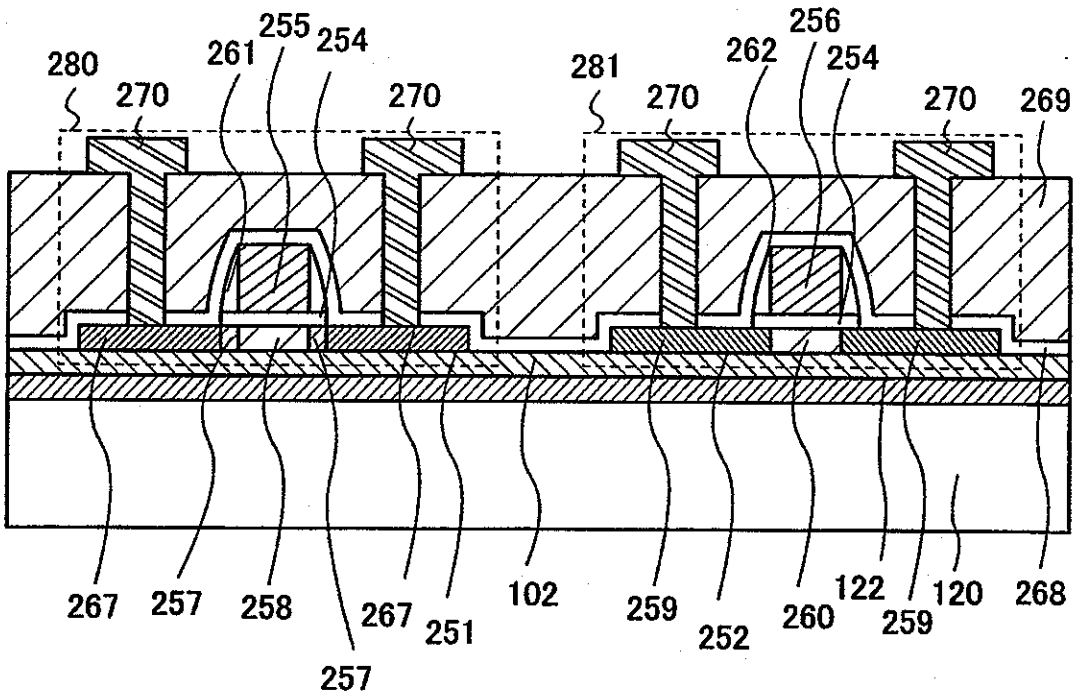

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268

FIG. 8A

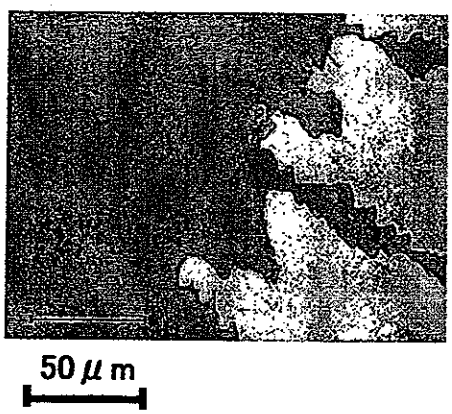


FIG. 8B

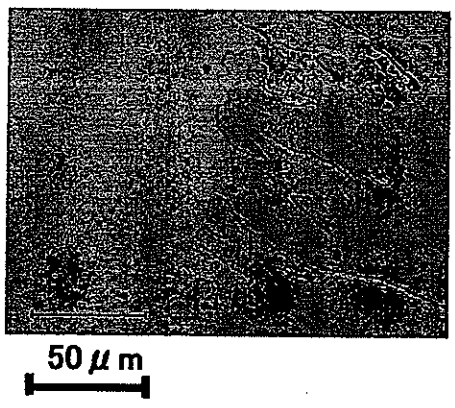


FIG. 9A

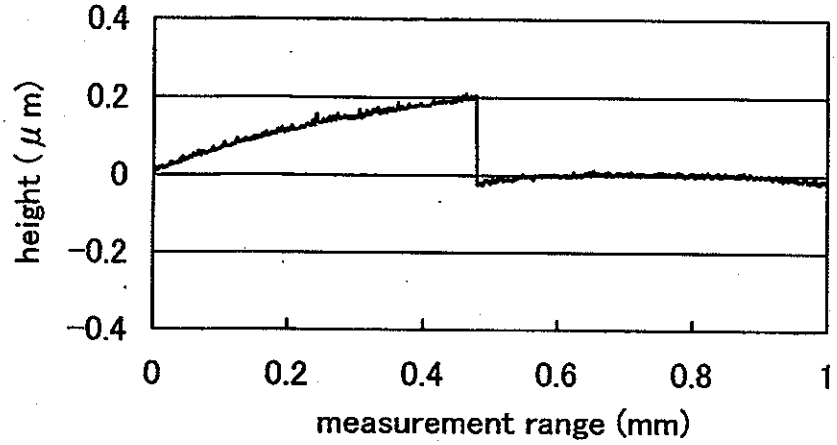

0.4
0.2
0
−0.2
−0.4
height (μm)
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0.2
0.4
0.6
0.8
1
measurement range (mm)

FIG. 9B

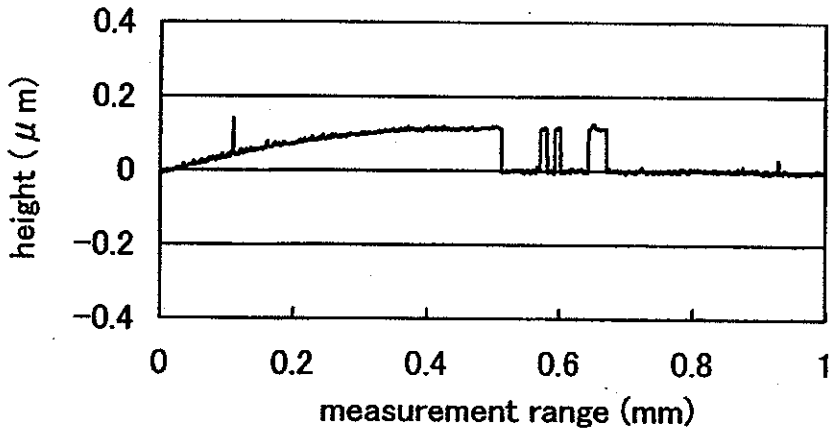

0.4
0.2
0
−0.2
−0.4
height (μm)
0
0.2
0.4
0.6
0.8
1
measurement range (mm)

FIG. 10A1

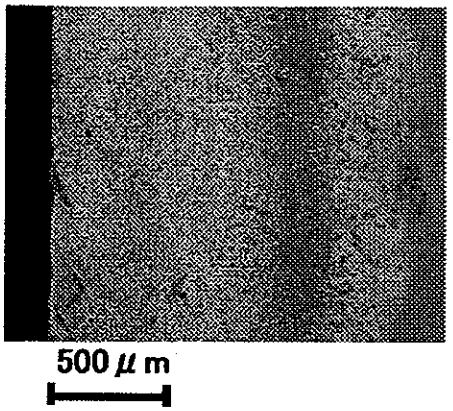


FIG. 10A2

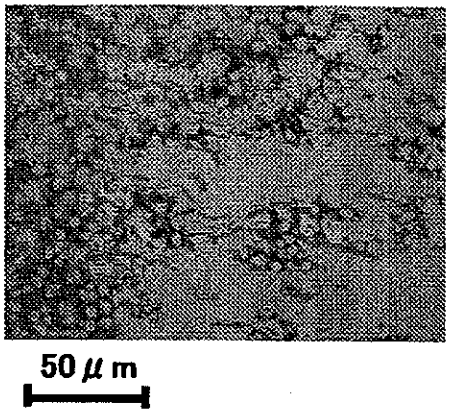


FIG. 10B1

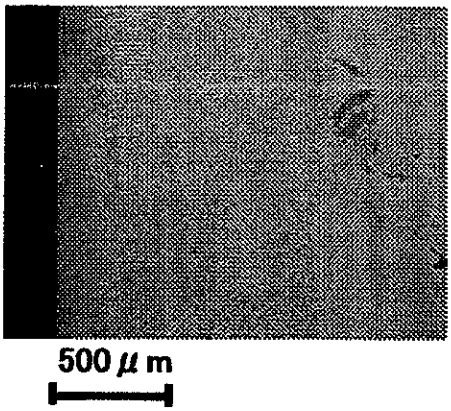


FIG. 10B2

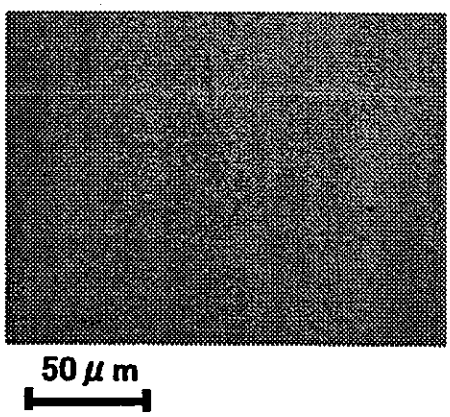


FIG. 10C1

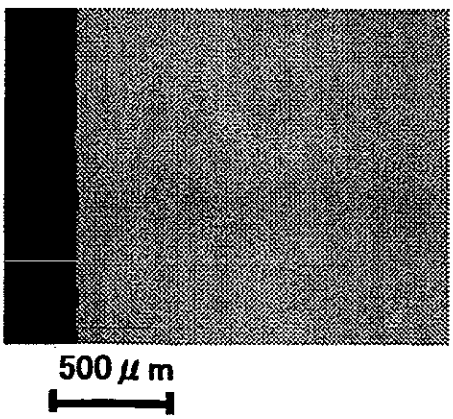


FIG. 10C2

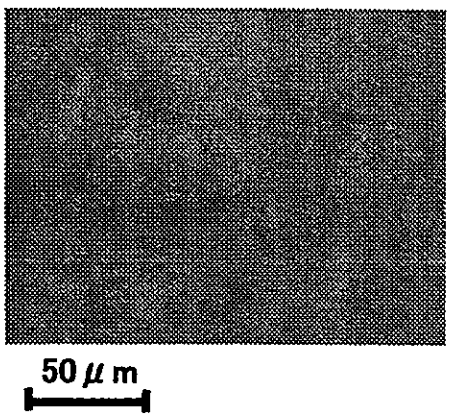


FIG. 11A1

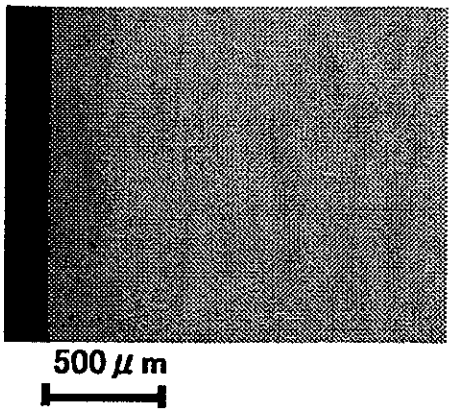


FIG. 11A2

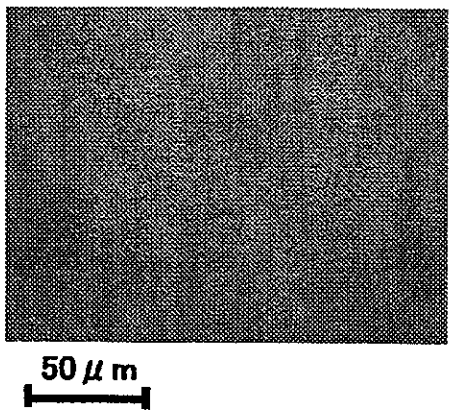


FIG. 11B1

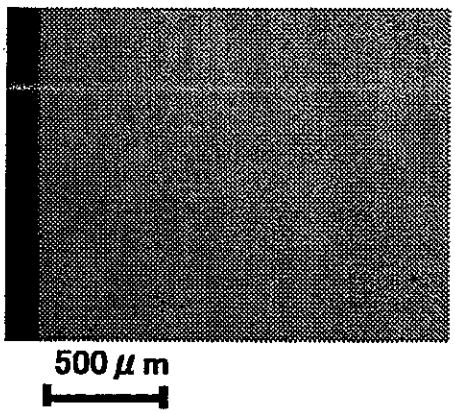


FIG. 11B2

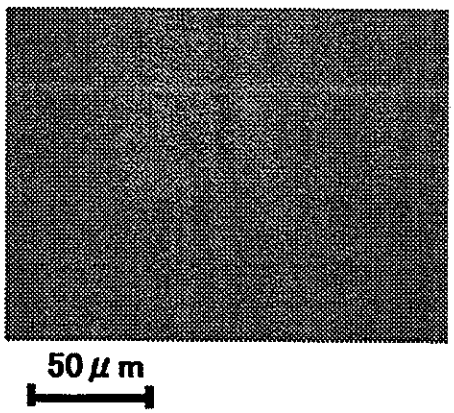


FIG. 11C1

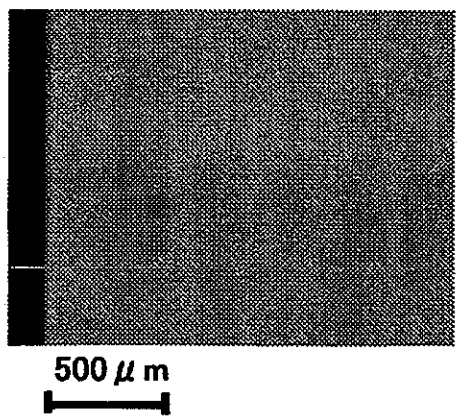


FIG. 11C2

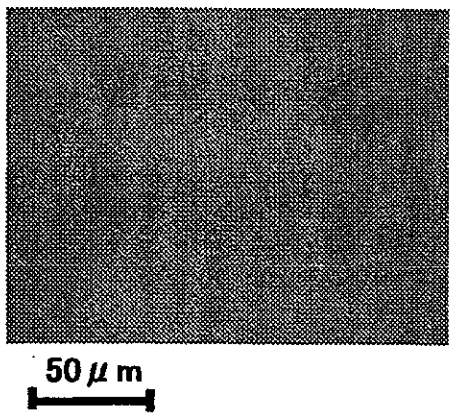


FIG. 12A

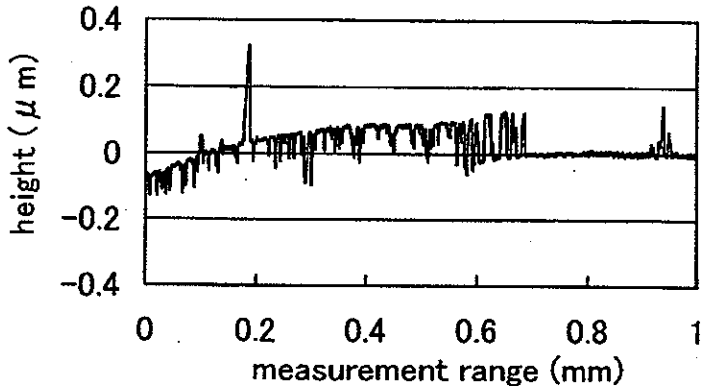


FIG. 12B

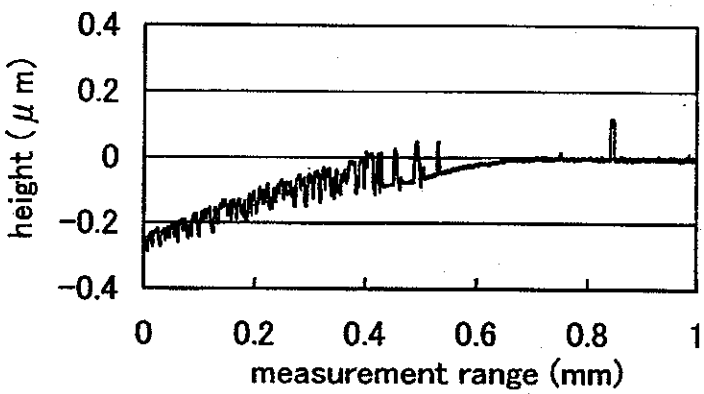


FIG. 12C

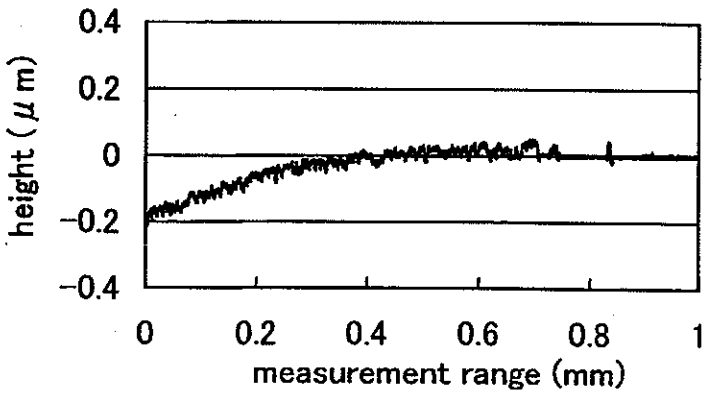


FIG. 13A

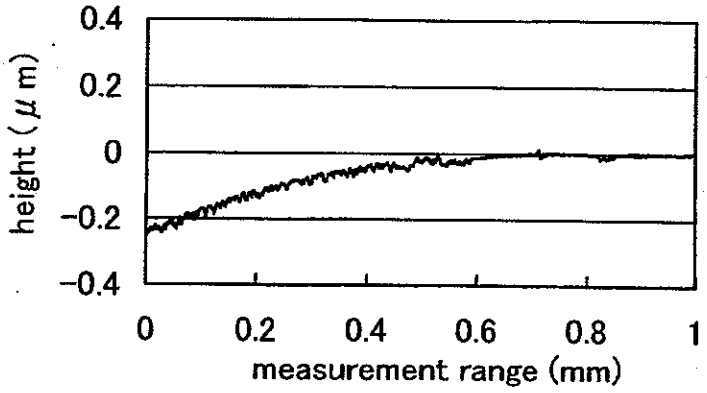


FIG. 13B

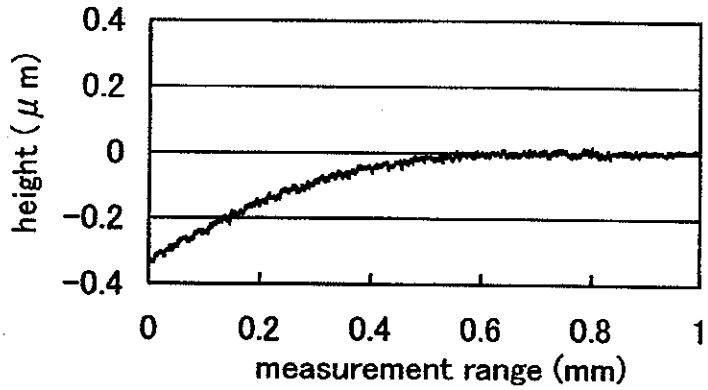


FIG. 13C

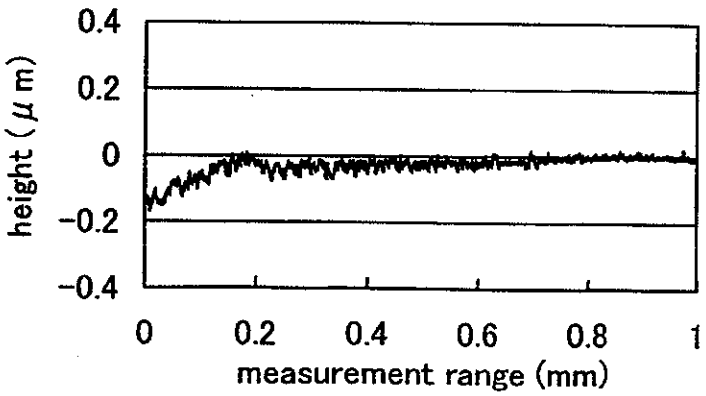


FIG. 14A

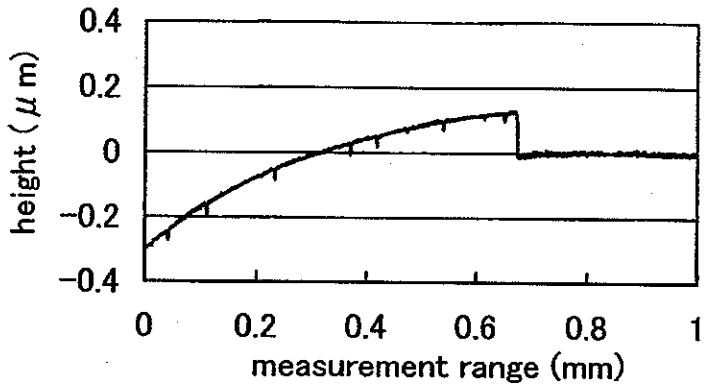


FIG. 14B

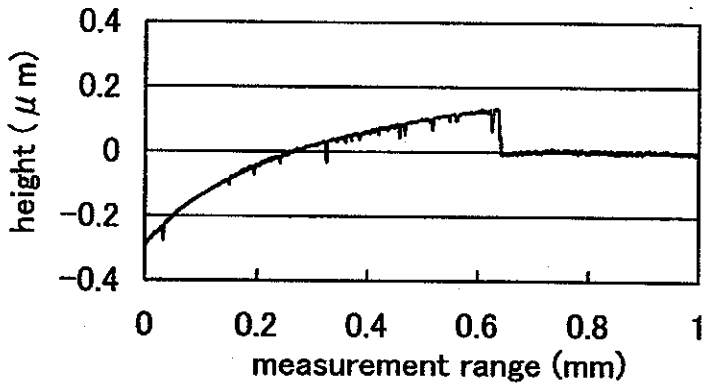


FIG. 14C

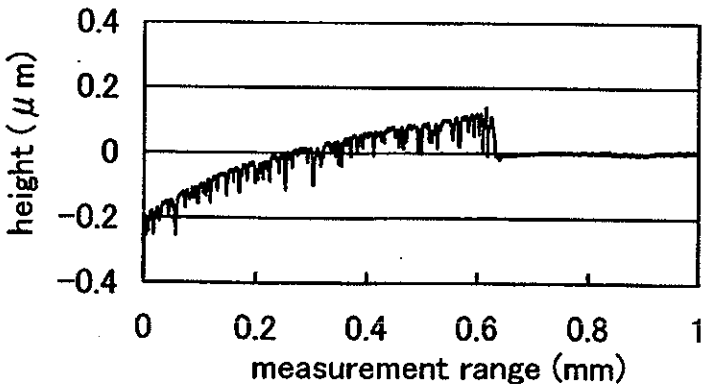


FIG. 15A

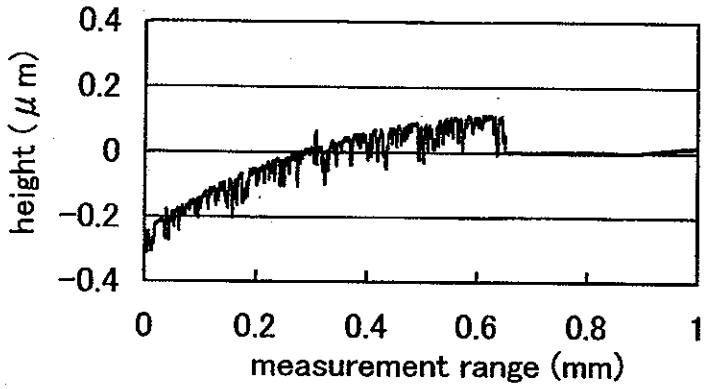


FIG. 15B

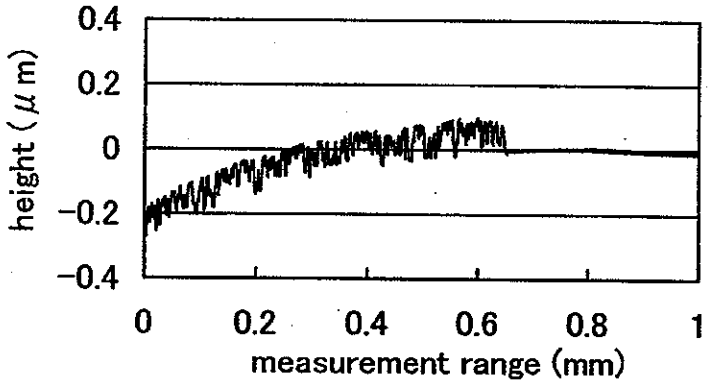


FIG. 15C

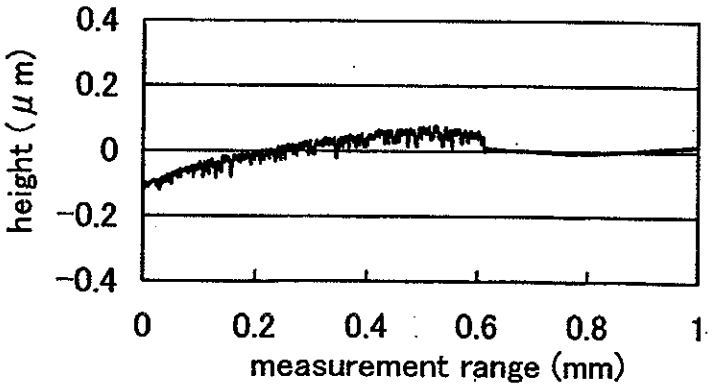


FIG. 16A

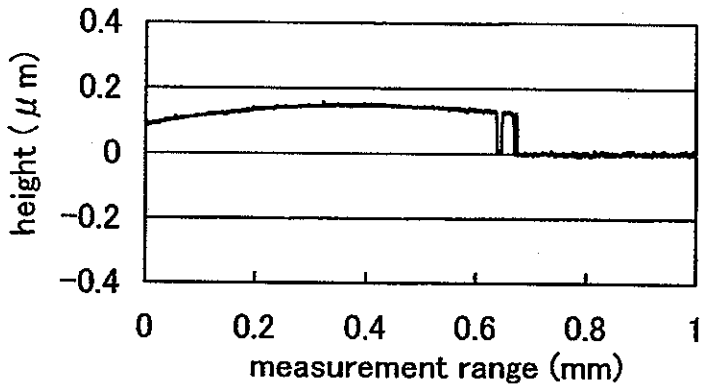


FIG. 16B

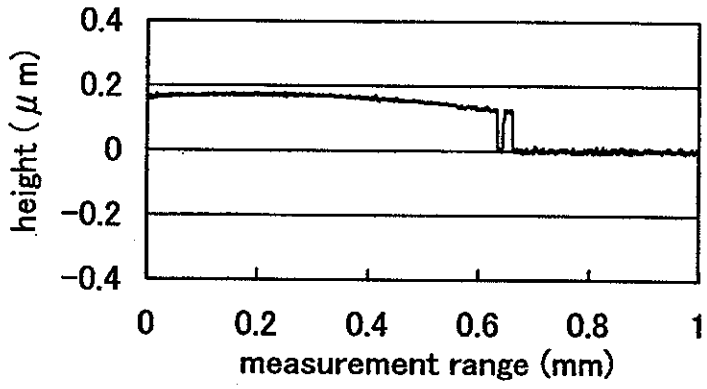


FIG. 16C

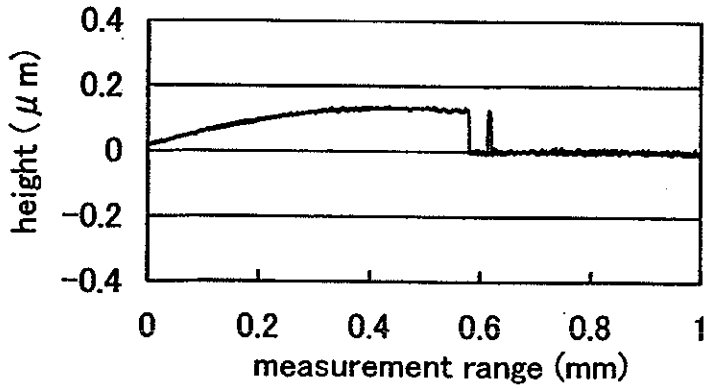


FIG. 17A

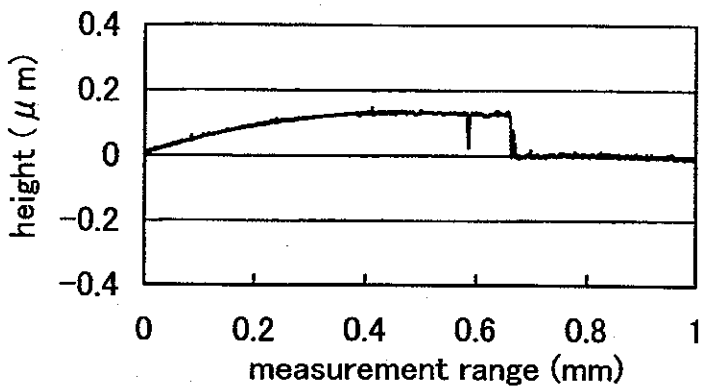


FIG. 17B

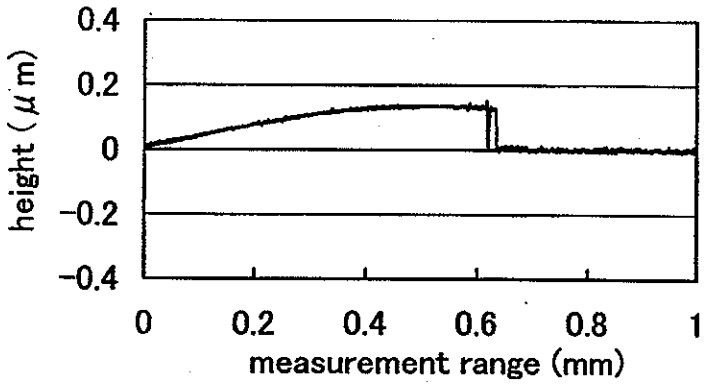


FIG. 17C

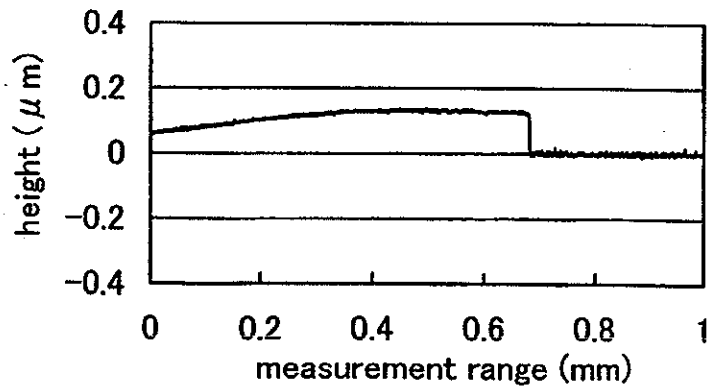


FIG. 18A

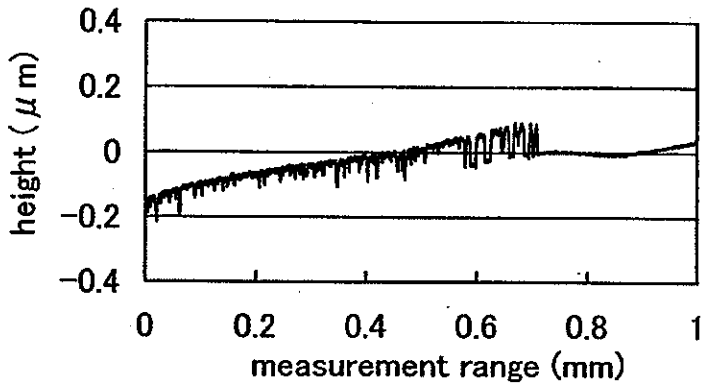


FIG. 18B

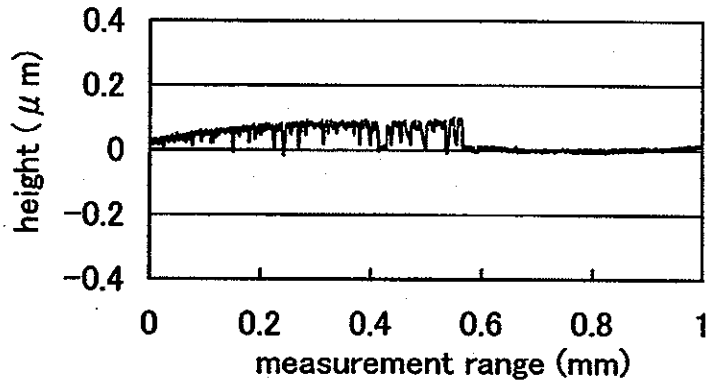


FIG. 18C

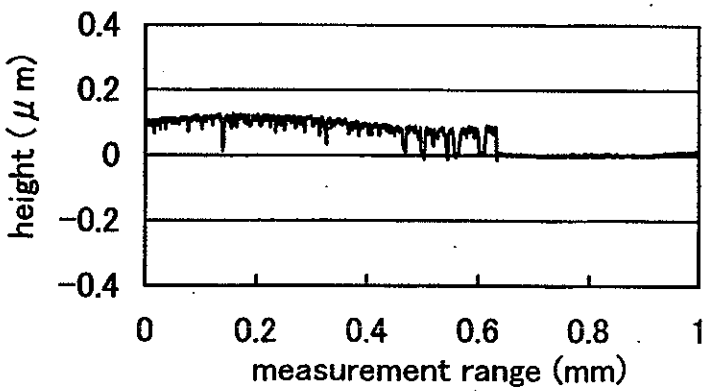


FIG. 19A

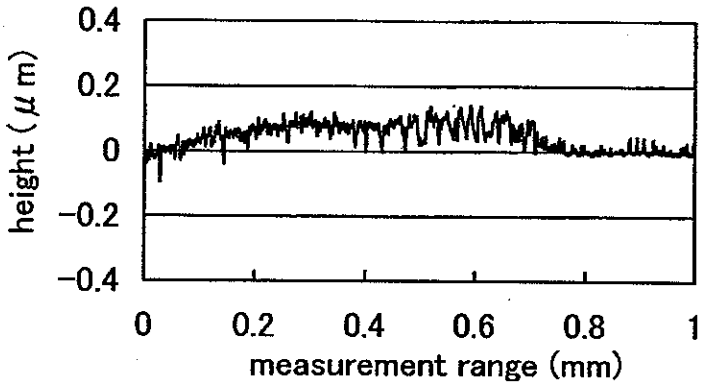


FIG. 19B

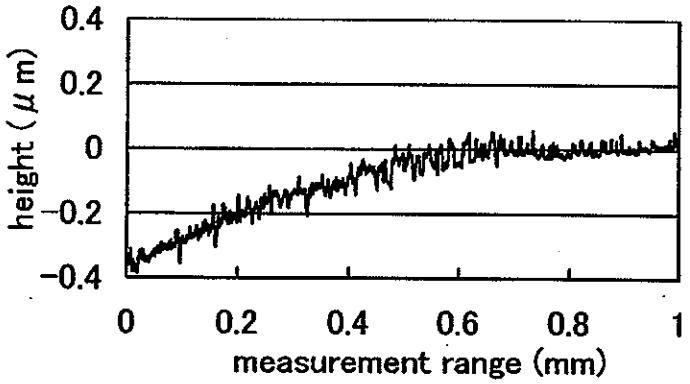


FIG. 19C

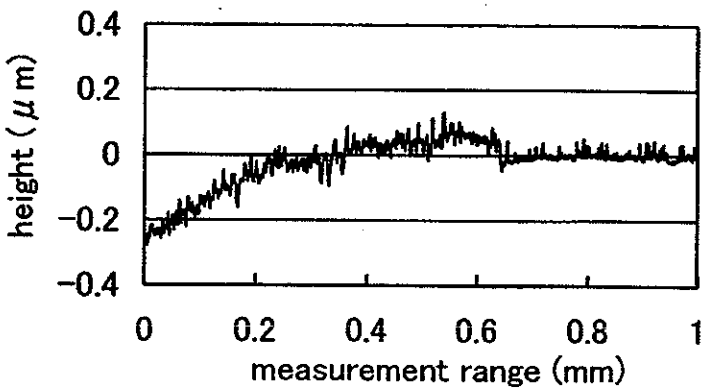


FIG. 20A

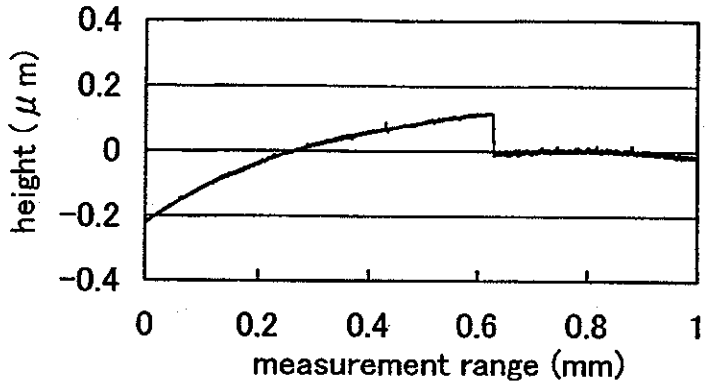


FIG. 20B

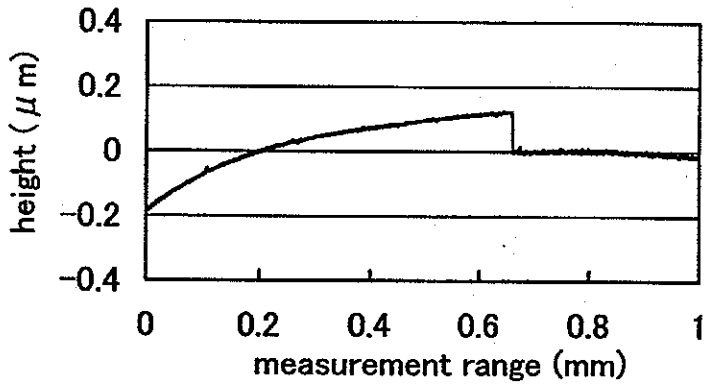


FIG. 20C

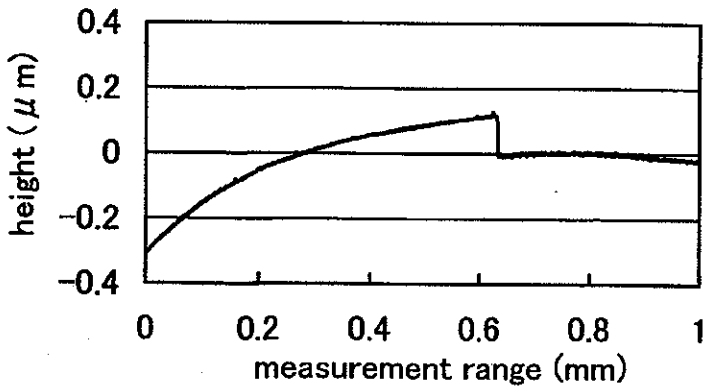


FIG. 21A

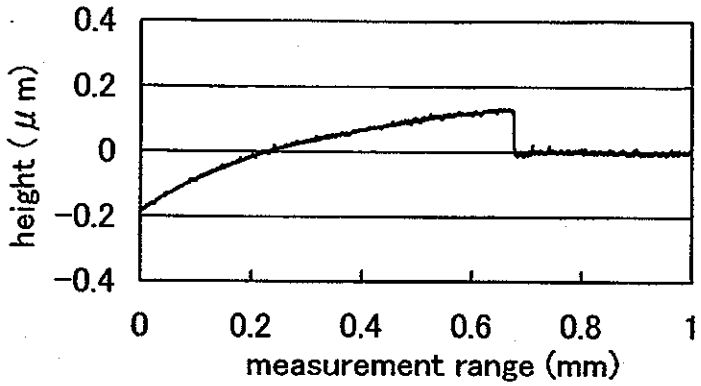


FIG. 21B

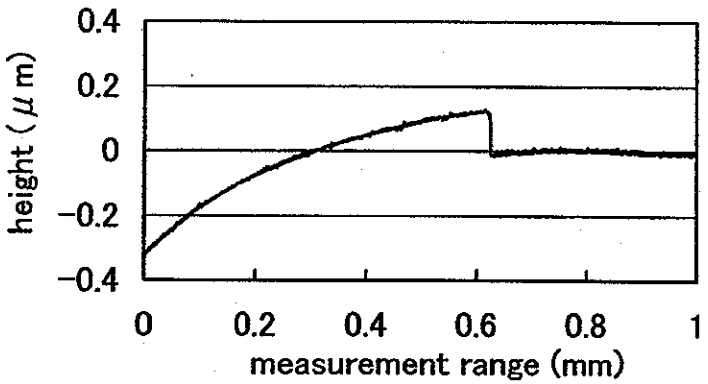


FIG. 21C

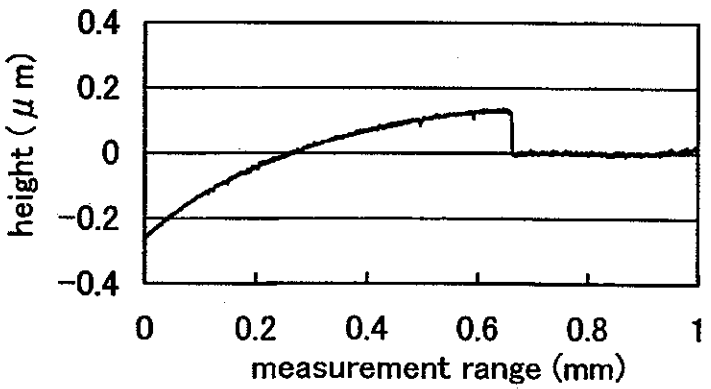


FIG. 22A

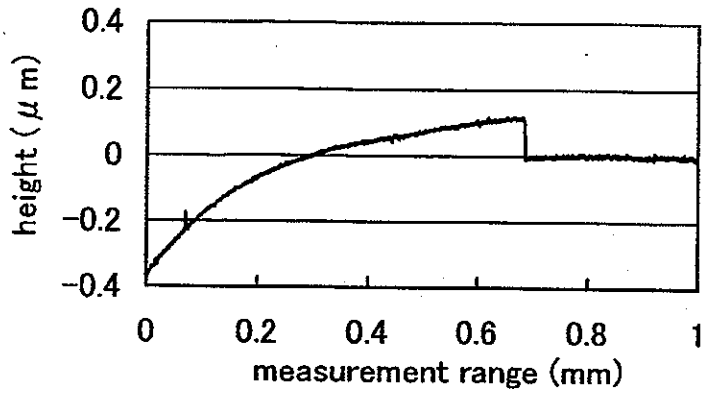


FIG. 22B

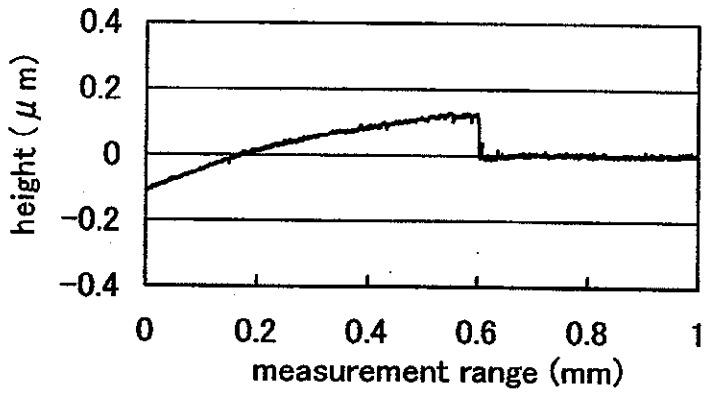


FIG. 22C

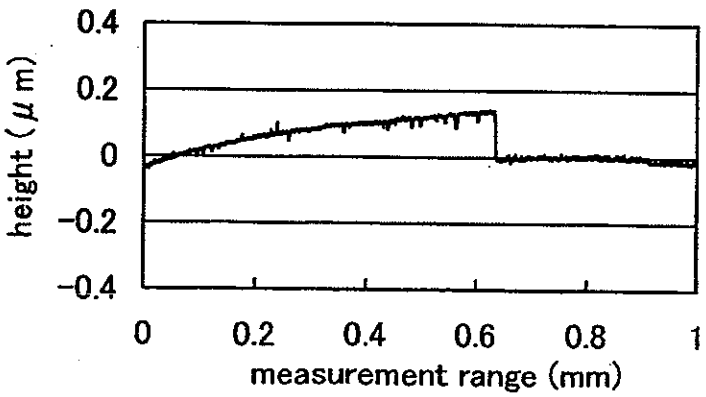


FIG. 23A

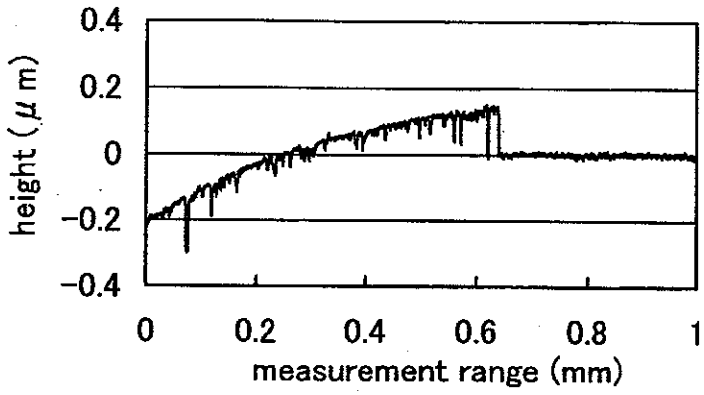


FIG. 23B

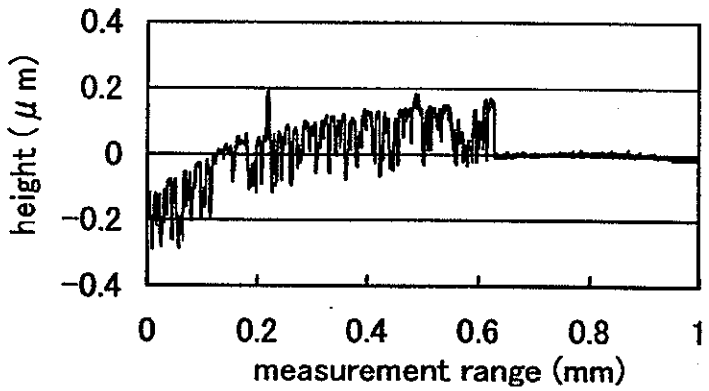


FIG. 23C

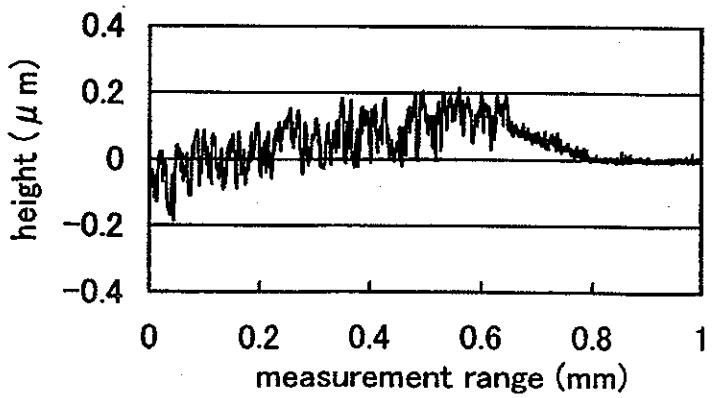


FIG. 24

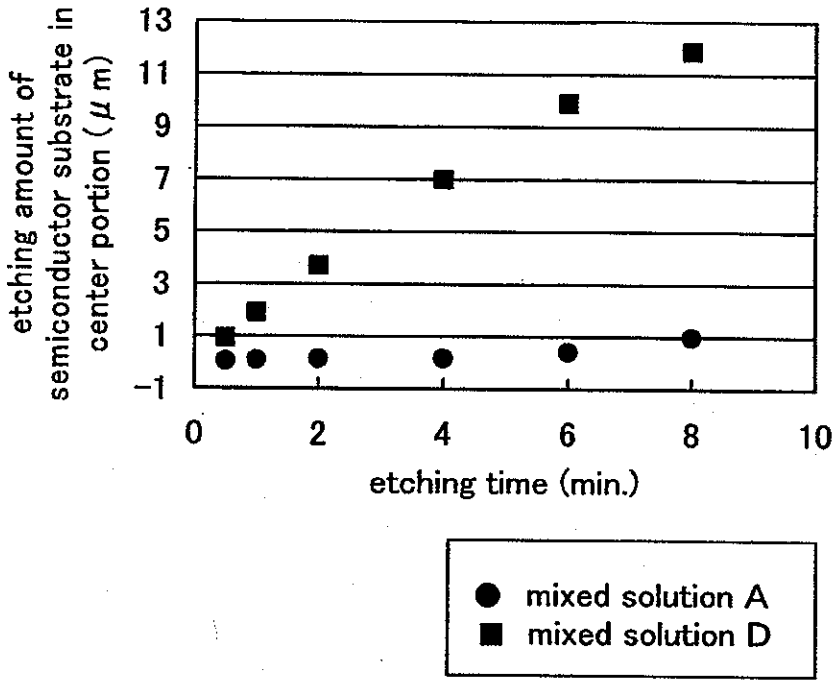

etching amount of semiconductor substrate in center portion (μm)
13
11
9
7
5
3
1
−1
0
2
4
6
8
10
etching time (min.)
mixed solution A
mixed solution D

FIG. 25A

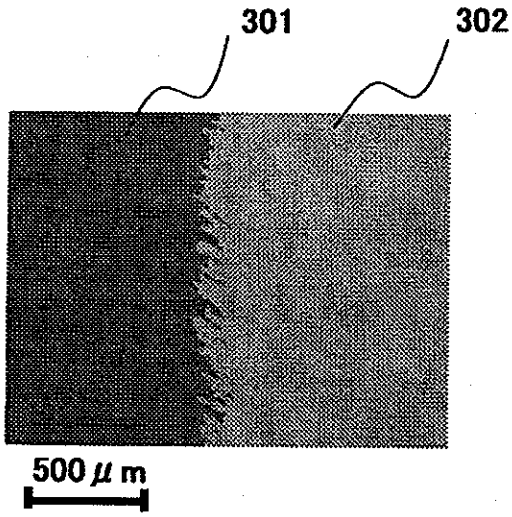


FIG. 25B

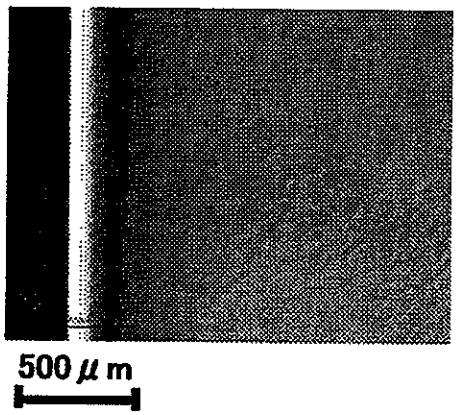


FIG. 26A

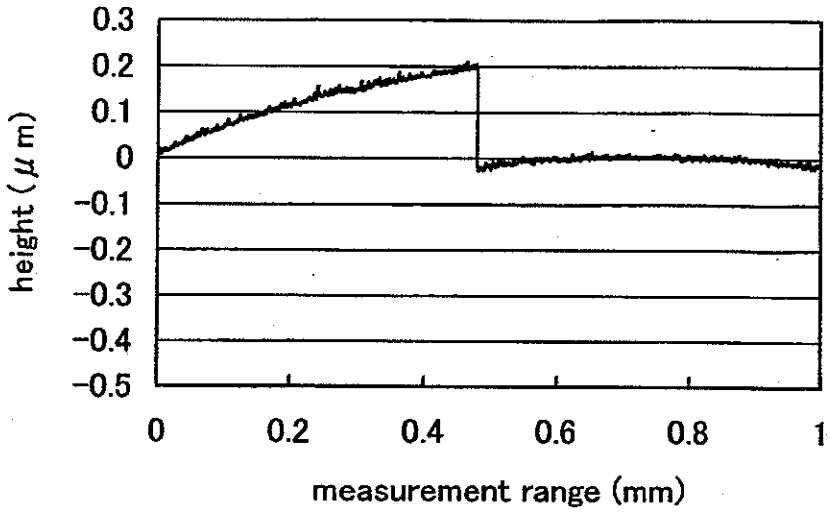


FIG. 26B

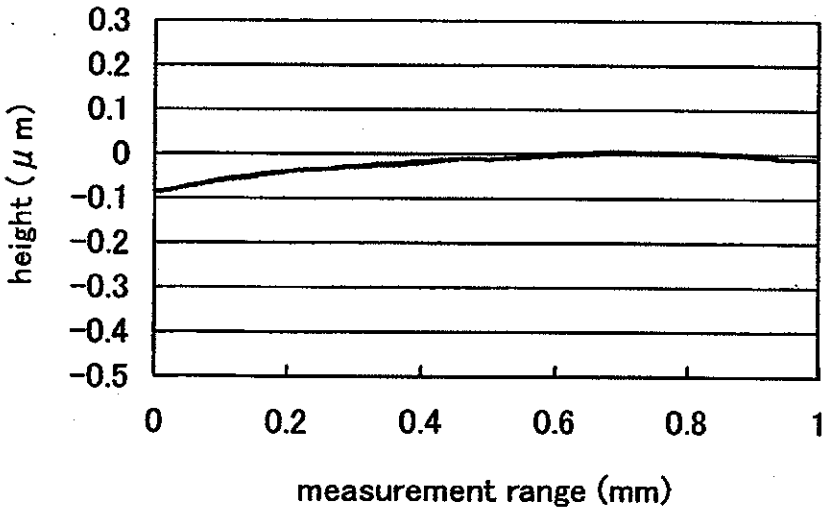


FIG. 27A

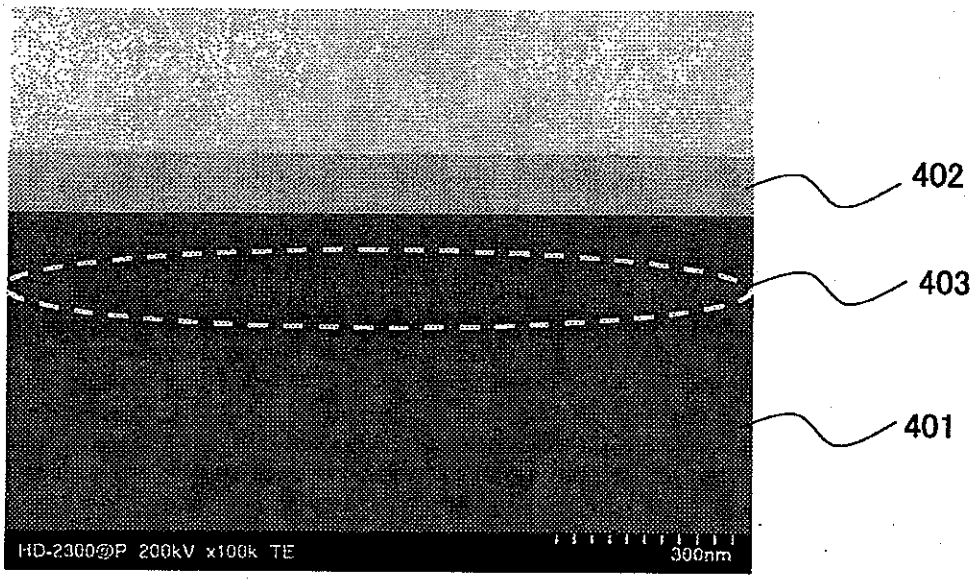


FIG. 27B

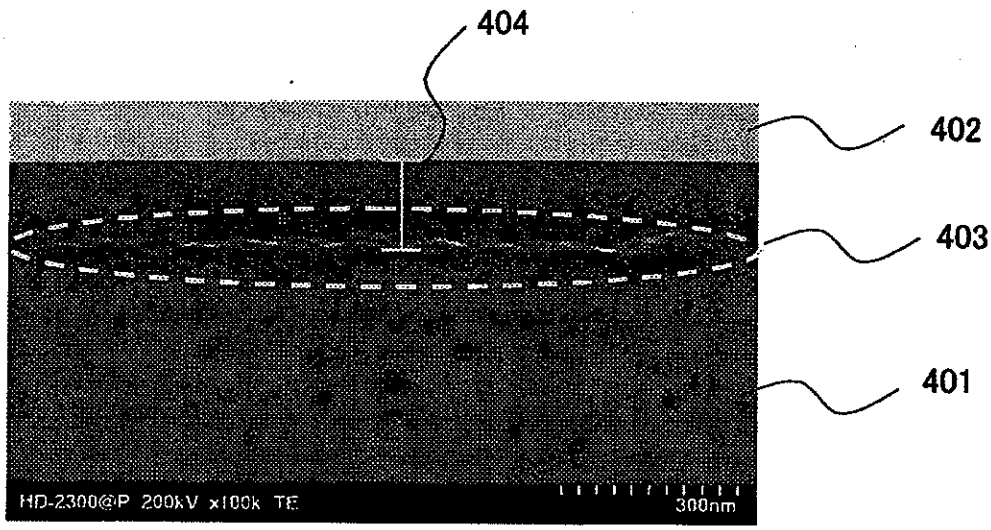


FIG. 28A

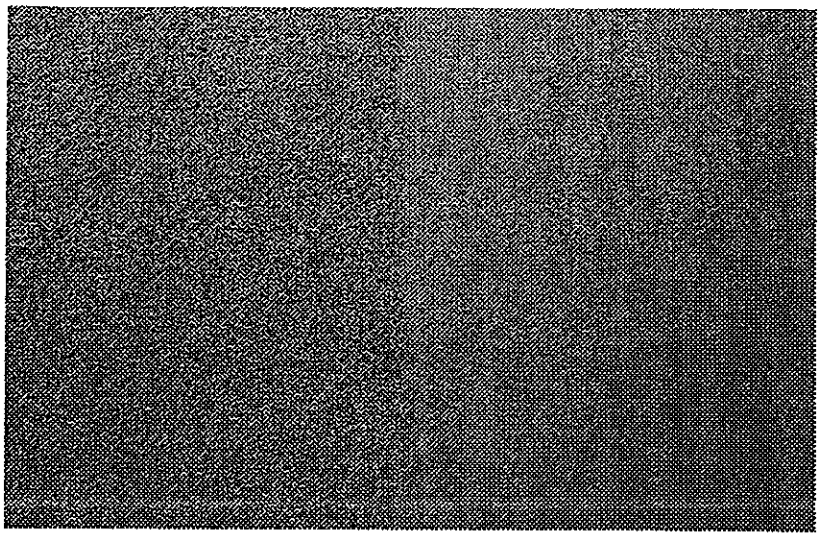


FIG. 28B

