CLAIMS

1. A method for forming a semiconductor structure, comprising:

providing a substrate, the substrate comprising a first isolation groove extending in a first direction and a plurality of active columns arranged in an array along the first direction and a third direction, the substrate being divided into a first area and a second area by the first isolation groove along a second direction, the active columns being supported through support structures, the first direction, the second direction and the third direction being perpendicular to each other in pairs, the first direction and the second direction being parallel to an upper surface of the substrate;

sequentially forming a medium layer and a first metal layer on surfaces of the active columns in gaps between the active columns, wherein the first metal layer located in the first area forms a lower electrode portion of capacitor structures, and the medium layer and the first metal layer located in the second area constitute gate-all-around structures;

processing the active columns, the medium layer and the first metal layer in the first area to form capacitor structures extending in the second direction; and

forming first connecting structures connecting the gate-all-around structures and the capacitor structures in the first isolation groove.

2. The method of claim 1, wherein the substrate further comprises a semiconductor substrate, and the active columns and the supporting structures are formed on the semiconductor substrate; wherein the processing the active columns, the medium layer and the first metal layer in the first area comprises:

forming a first opening extending in the first direction in the first area, the first opening exposing the semiconductor substrate;

removing the active columns and the medium layer in the first area through the first opening to form a first gap; and

sequentially forming a dielectric layer and a second metal layer in the first opening and the first gap, the first metal layer, the dielectric layer and the second metal layer located in the first area constituting the capacitor structure,

wherein after forming the first metal layer, the method further comprises:

forming a first isolation layer between the first metal layers and in the first isolation groove.

3. The method of claim 2, wherein the forming first connecting structures comprises:

removing the first isolation layer located in the first isolation groove, and removing the medium layer and the first metal layer located on a side wall of the second area in the first isolation groove to form a second isolation groove extending in the first direction, the second isolation groove exposing the active columns in the second area and the first metal layer on a side wall of the first area;

epitaxially growing the first connecting structure on a surface of the exposed active column, the first connecting structure being in contact with the first metal layer in the first area.

4. The method of claim 3, after forming the first connecting structure, the method further comprises:

forming a second isolation layer in the second isolation groove and between the first connecting structures, a surface of the second isolation layer being flush with a surface of the first isolation layer.

5. The method of claim 4, further comprising:

forming a bit line structure, and a stepped word line structure connected to the gate-all-around structure,

wherein the forming a bit line structure comprises:

etching an end, far away from the capacitor structure, of the active column to form a bit line trench extending in the first direction, the bit line trench exposing the semiconductor substrate in the second area; and

filling the bit line trench with a bit line metal material to form the bit line structure, the bit line structure and the gate-all-around structure being spaced by the support structures.

6. The method of claim 5, wherein the substrate further comprises a third isolation groove extending in the second direction, and the gate-all-around structure is divided into a first part and a second part by the third isolation groove in the first direction; the forming a stepped word line structure comprises:

forming a photoresist layer with a second opening on a surface of the second part, the second opening exposing an end, far away from the first part, of the second part; and

etching the second part for a plurality of times through the photoresist layer to form the stepped word line structure, wherein a size of the second opening in the first direction increases sequentially during etching for the plurality of times.

7. The method of claim 6, before forming the stepped word line structure, the method further comprises:

removing the first isolation layer located in the third isolation groove, and removing the medium layer and the first metal layer located on a side wall of the second part in the third isolation groove to form a fourth isolation groove extending in the second direction, the fourth isolation groove exposing the first metal layer on a side wall of the first part and the active column of the second part; and

forming a second connecting structure connecting the second part and the gate-all-around structure in the fourth isolation groove.

8. The method of claim 7, wherein the forming a second connecting structure comprises:

epitaxially growing the second connecting structure on the surface of the exposed active column of the second part, the second connecting structure being in contact with the first metal layer on the side wall of the first part.

9. The method of claim 8, after forming the second connecting structure, the method further comprises:

forming an insulating medium layer on a surface of the second connecting structure, a surface of the insulating medium layer being flush with a surface of the medium layer;

forming a third metal layer on the surface of the insulating medium layer, a surface of the third metal layer is flush with a surface of the first metal layer; and

filling a third isolation material on the surface of the third metal layer and between the third metal layers to form a third isolation layer, a surface of the third isolation layer is flush with the surface of the first isolation layer.

10. The method of claim 9, after forming the third isolation layer, the method further comprises:

forming a first metal wire connected to the capacitor structure, a second metal wire connected to the bit line structure, and a third metal wire connected to the stepped word line structure,

wherein the forming a first metal wire, a second metal wire, and a third metal wire comprises:

forming a barrier layer on surfaces of the stepped word line structure, the first isolation layer, the second isolation layer and the third isolation layer;

etching the barrier layer to form a first through hole exposing the second metal layer, a second through hole exposing the bit line structure, and a third through hole exposing the stepped word line structure; and

forming the first metal wire in the first through hole, forming the second metal wire in

the second through hole, and forming the third metal wire in the third through hole.

11. The method of claim 6, wherein the forming the substrate comprises:

providing a semiconductor substrate;

forming a stacked structure on the semiconductor substrate, the stacked structure comprising first semiconductor layers and second semiconductor layers stacked alternately;

etching the stacked structure to form the first isolation groove; and

removing the first semiconductor layers in the stacked structure.

12. The method of claim 11, after forming the first isolation groove, the method further comprises:

etching the stacked structure to form a fifth isolation groove extending in the second direction, the second semiconductor layers being divided into a plurality of active columns arranged in the first direction by the fifth isolation groove; and

forming an isolation structure in the fifth isolation groove.

13. The method of claim 12, before forming the first isolation layer, the method further comprises:

etching and removing part of the isolation structure and part of the first semiconductor layers to form a plurality of etched holes extending in the first direction, the etched holes exposing the active columns; and

filling the etched holes with a support material to form the support structures surrounding the active columns.

14. The method of claim 13, after forming the first isolation groove and before removing the first semiconductor layers in the stacked structure, the method further comprises:

filling the first isolation groove with a sacrificial material to form a sacrificial layer.

15. A semiconductor structure, comprising:

a substrate; wherein the substrate comprises a first area and a second area arranged in a second direction, and the second area comprises active columns arranged in an array along a first direction and a third direction; wherein the first direction, the second direction and the third direction are perpendicular to each other in pairs, and the first direction and the second direction are parallel to an upper surface of the substrate;

capacitor structures located in the first area, and gate-all-around structures located in the second area; wherein the gate-all-around structures surround surfaces of the active columns;

first connecting structures connecting the gate-all-around structures and the capacitor structures; and

support structures supporting the capacitor structures and the gate-all-around structures.

16. The semiconductor structure of claim 15, wherein the capacitor structures comprise a first metal layer, a dielectric layer, and a second metal layer;

the gate-all-around structures comprises the medium layer and the first metal layer.

17. The semiconductor structure of claim 16, further comprising: a bit line structure located in the second area and extending in the first direction.

18. The semiconductor structure of claim 17, further comprising: a second connecting structure and a stepped word line structure;

wherein the gate-all-around structure is connected to the stepped word line structure through the second connecting structure.

19. The semiconductor structure of claim 18, further comprising: a first metal wire, a second metal wire and a third metal wire;

wherein the first metal wire is located on a surface of the capacitor structure and is electrically connected to the capacitor structure;

the second metal wire is located on a surface of the bit line structure and is electrically connected to the bit line structure; and

the third metal wire is located on a surface of the stepped word line structure and is electrically connected to the stepped word line structure.