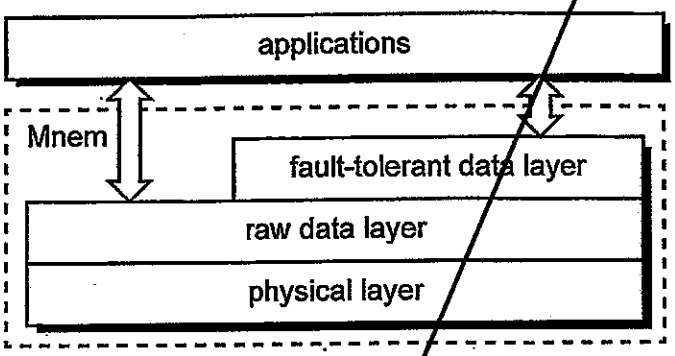

applications
Mnem
fault-tolerant data layer
raw data layer
physical layer

FIG. 1

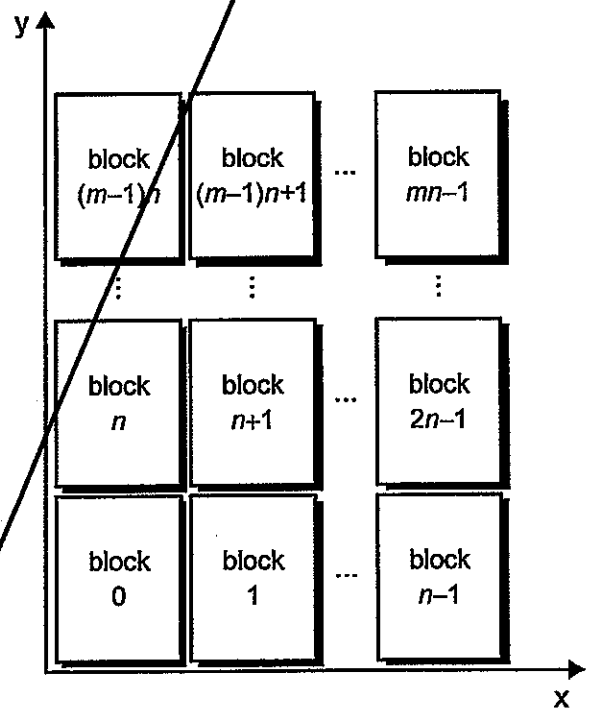

y
block (m–1)n
block (m–1)n+1
...
block mn–1
block n
block n+1
...
block 2n–1
block 0
block 1
...
block n–1
x

FIG. 2

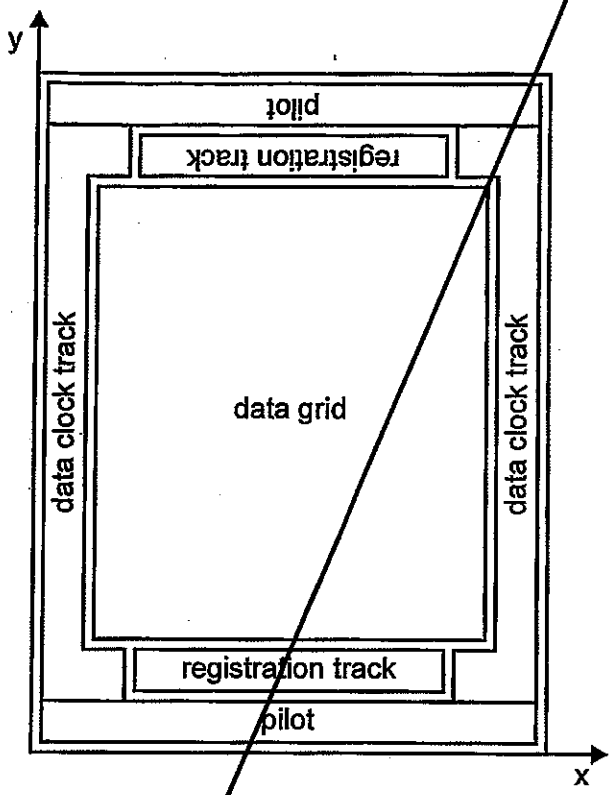

y
pilot
registration track
data clock track
data grid
data clock track
registration track
pilot
x

FIG. 3

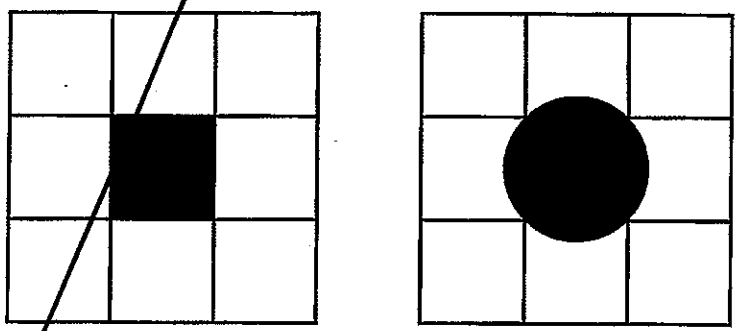


FIG. 4

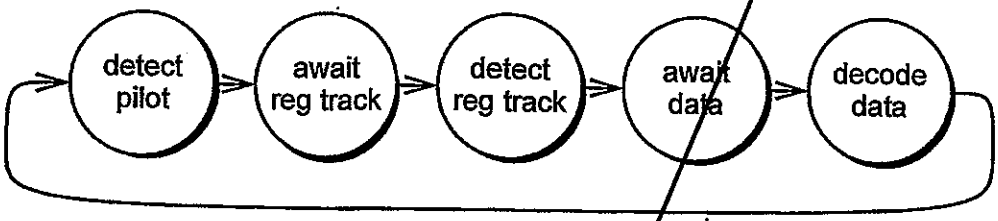

detect pilot
await reg track
detect reg track
await data
decode data

FIG. 5

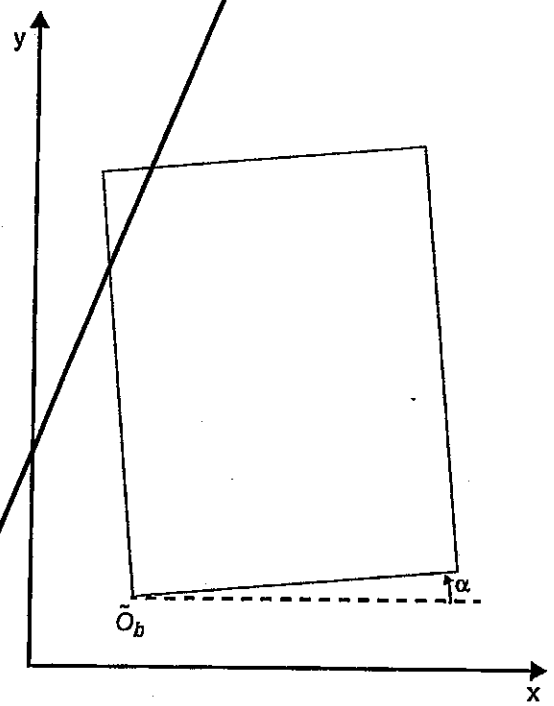

y
x
α
$\tilde{O}_b$

FIG. 6

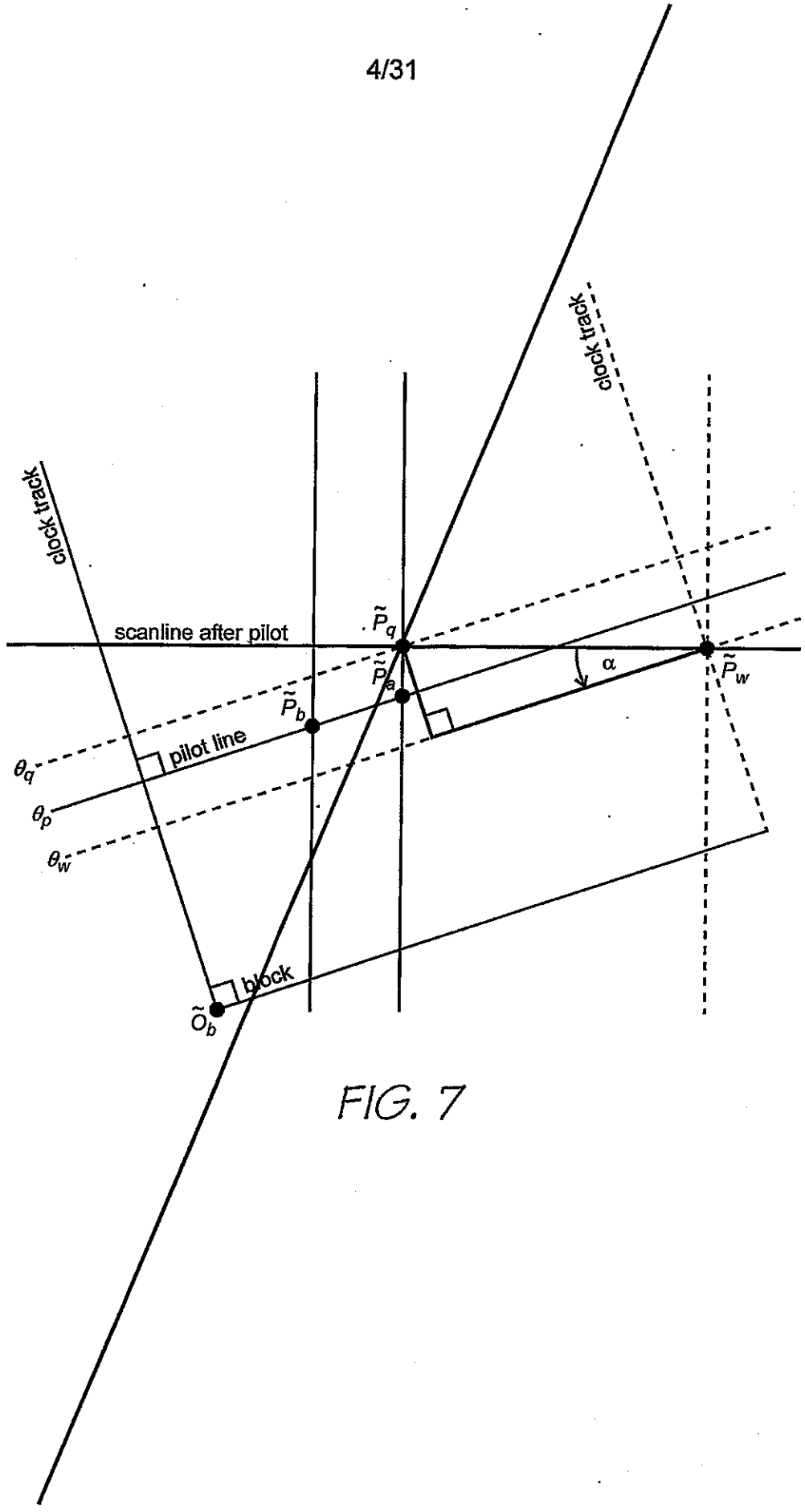

clock track
clock track
scanline after pilot
$\tilde{P}_q$
$\tilde{P}_a$
$\tilde{P}_b$
$\tilde{P}_w$
α
pilot line
θ_q
θ_p
θ_w
block
$\tilde{O}_b$

FIG. 7

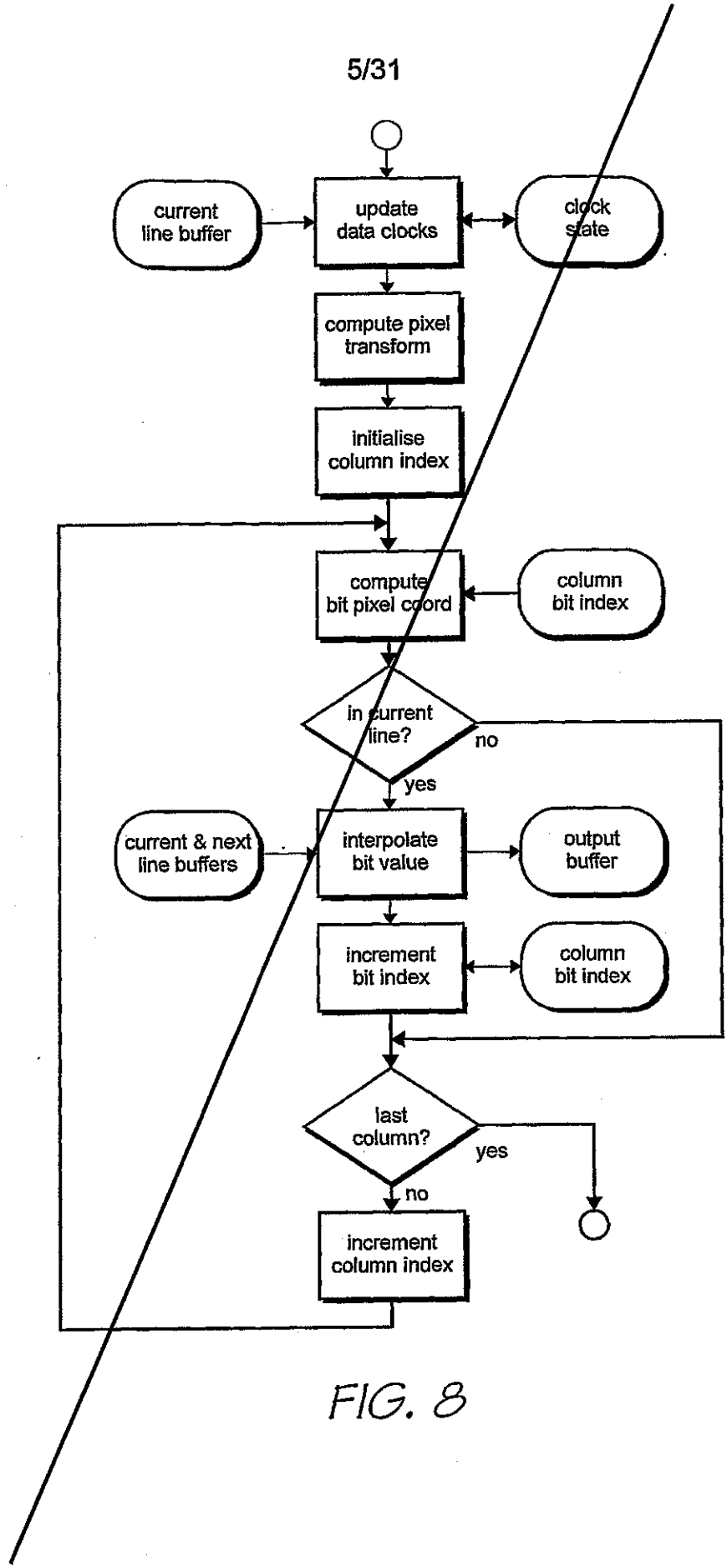

current line buffer
update data clocks
clock state
compute pixel transform
initialise column index
compute bit pixel coord
column bit index
in current line?
no
yes
current & next line buffers
interpolate bit value
output buffer
increment bit index
column bit index
last column?
yes
no
increment column index

FIG. 8

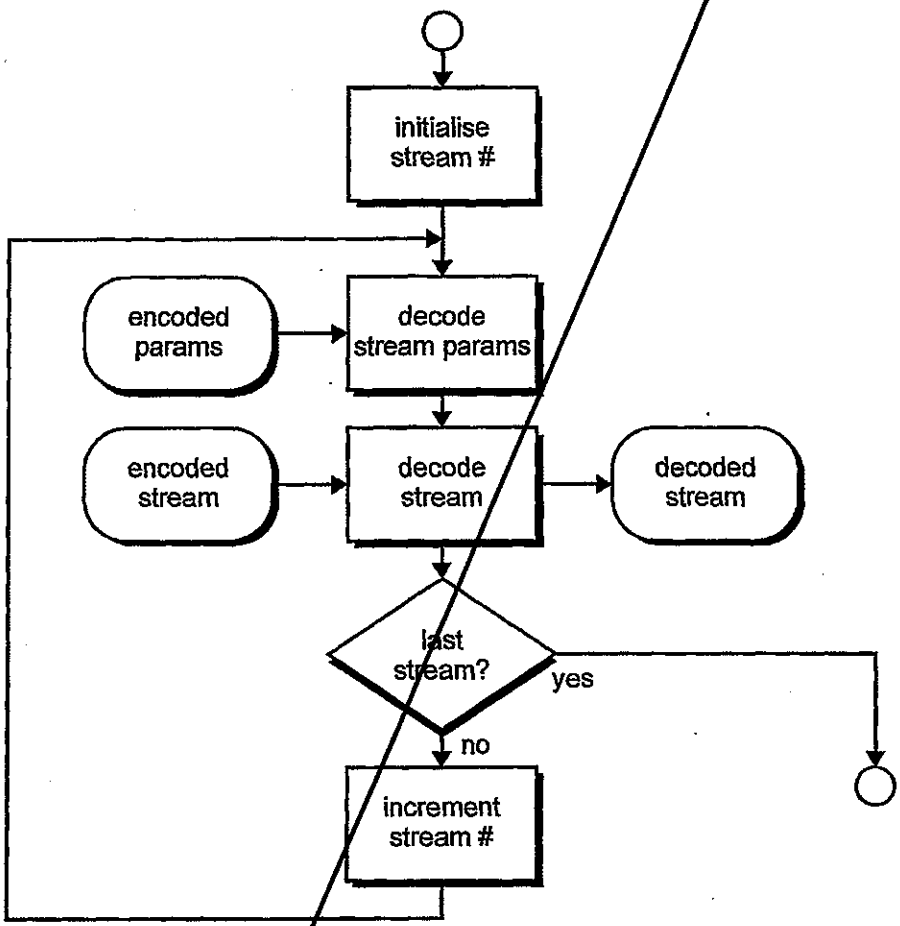

initialise stream #
encoded params
decode stream params
encoded stream
decode stream
decoded stream
last stream?
yes
no
increment stream #

FIG. 9

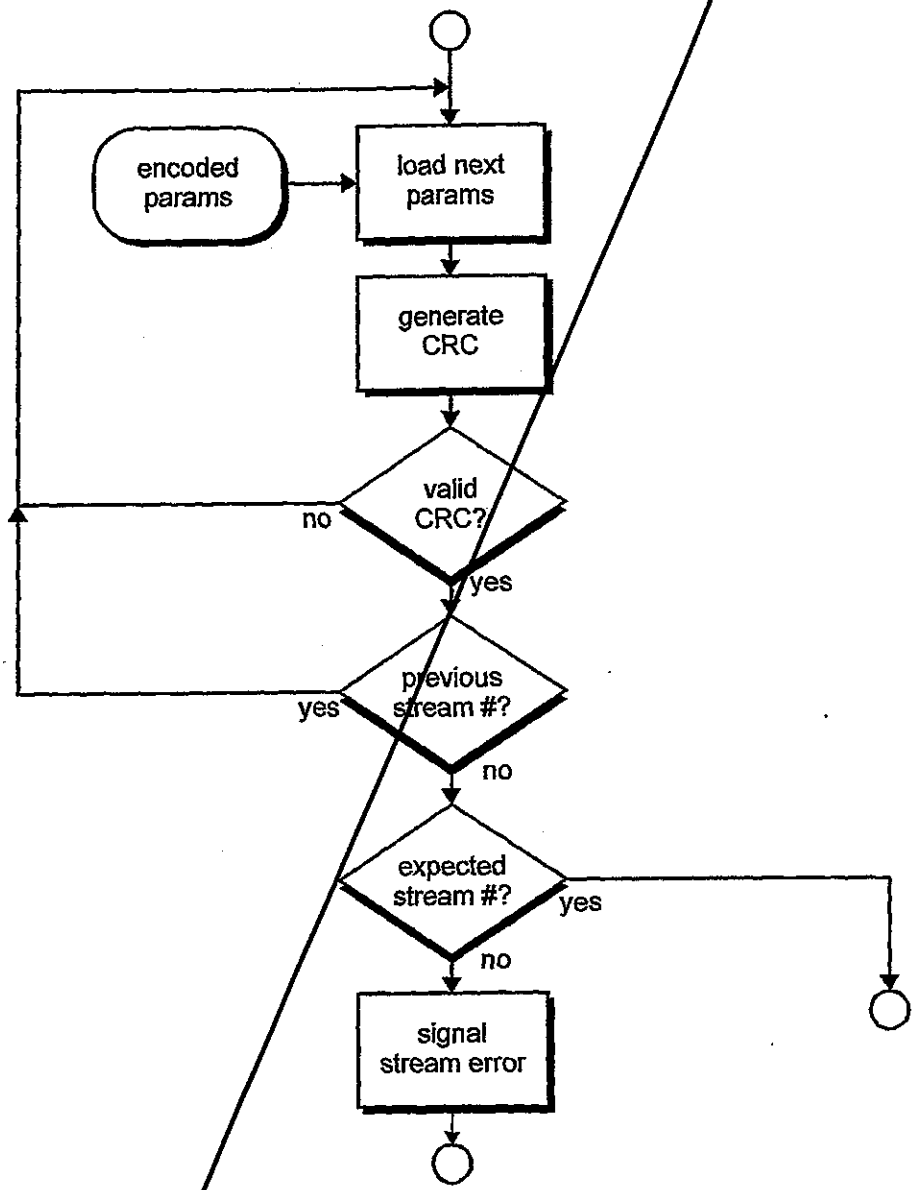

encoded params
load next params
generate CRC
valid CRC?
no
yes
previous stream #?
yes
no
expected stream #?
yes
no
signal stream error

FIG. 10

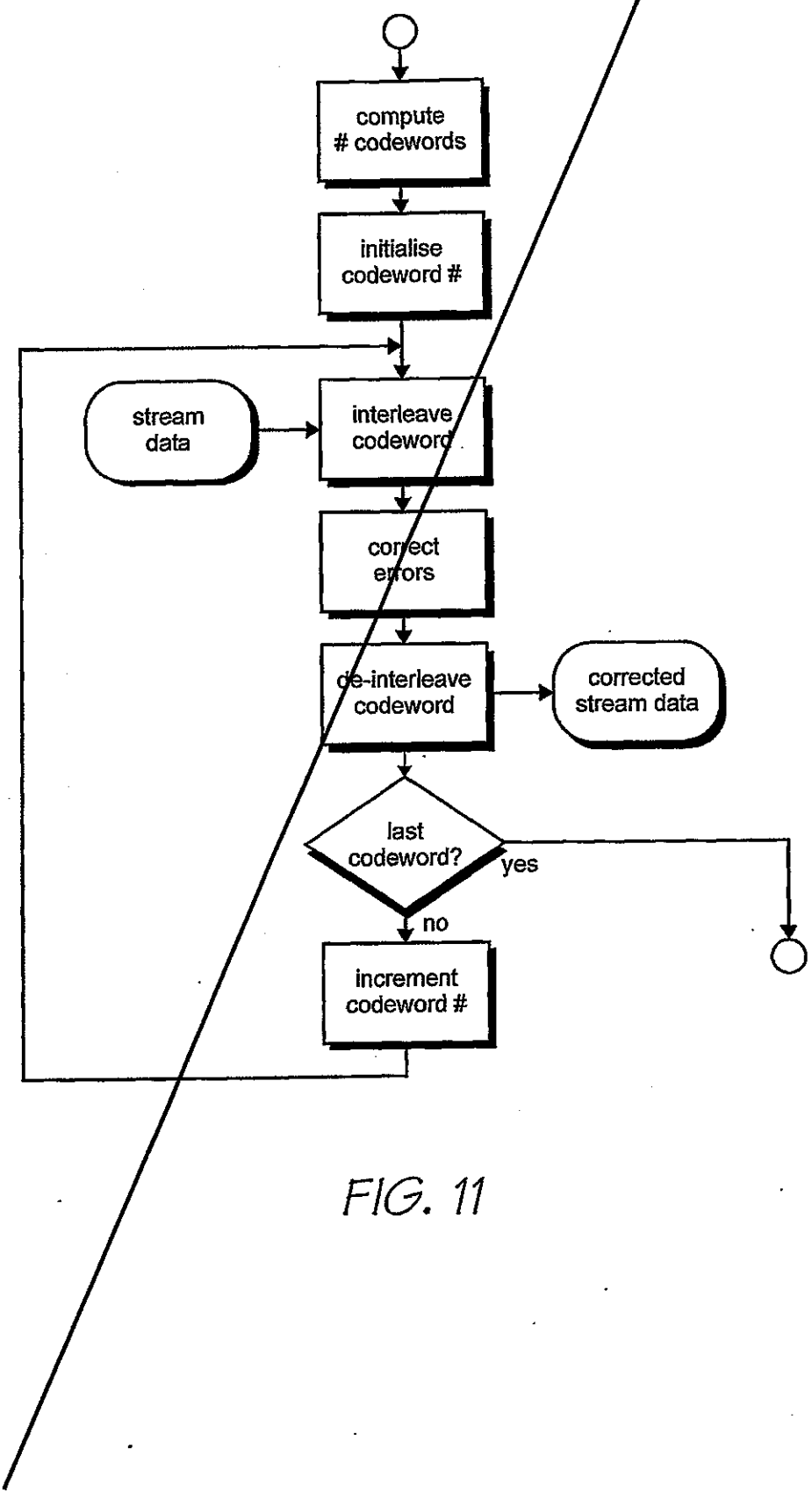

compute
codewords
initialise
codeword #
stream
data
interleave
codeword
correct
errors
de-interleave
codeword
corrected
stream data
last
codeword?
yes
no
increment
codeword #

FIG. 11

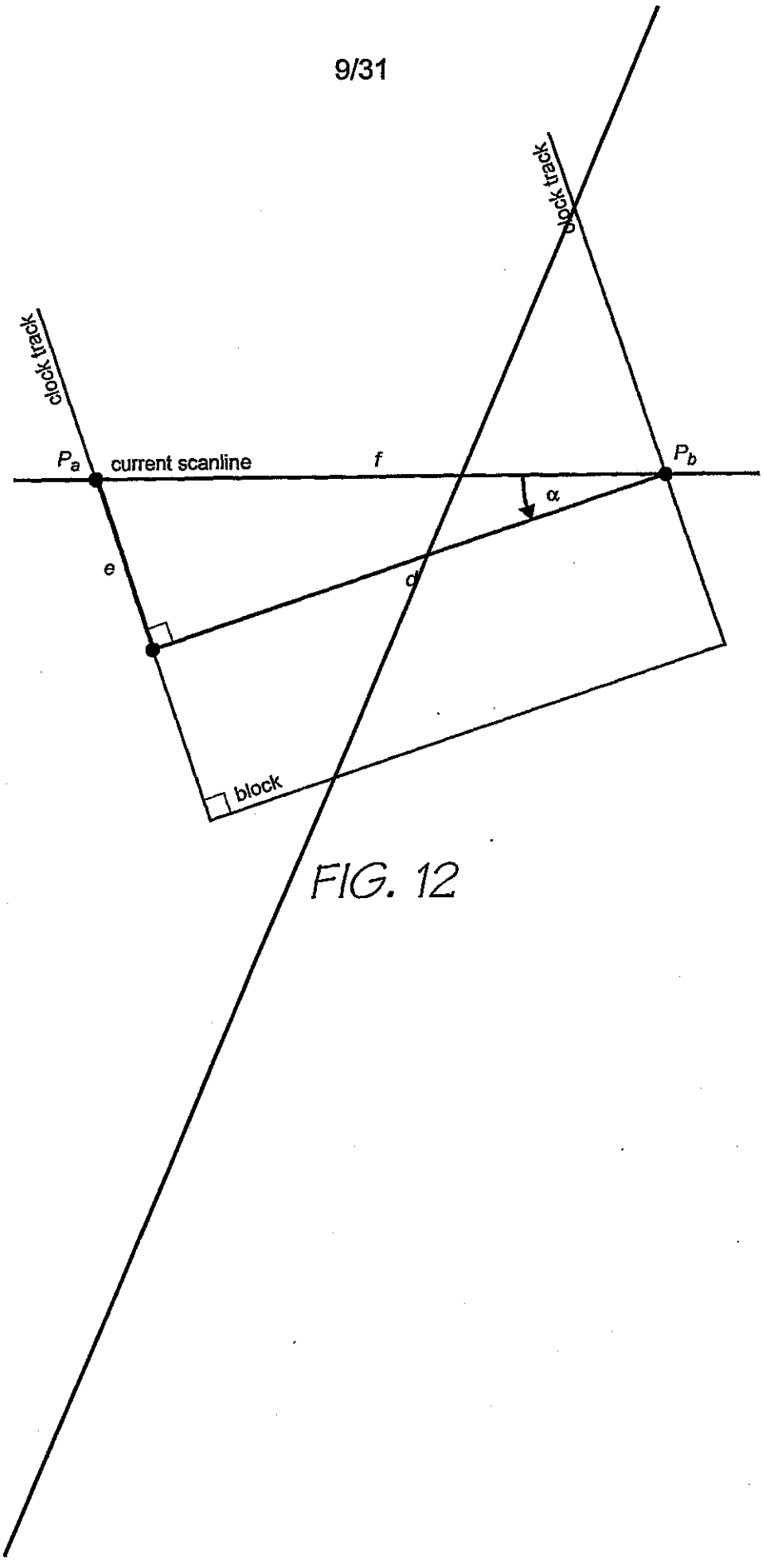


FIG. 12

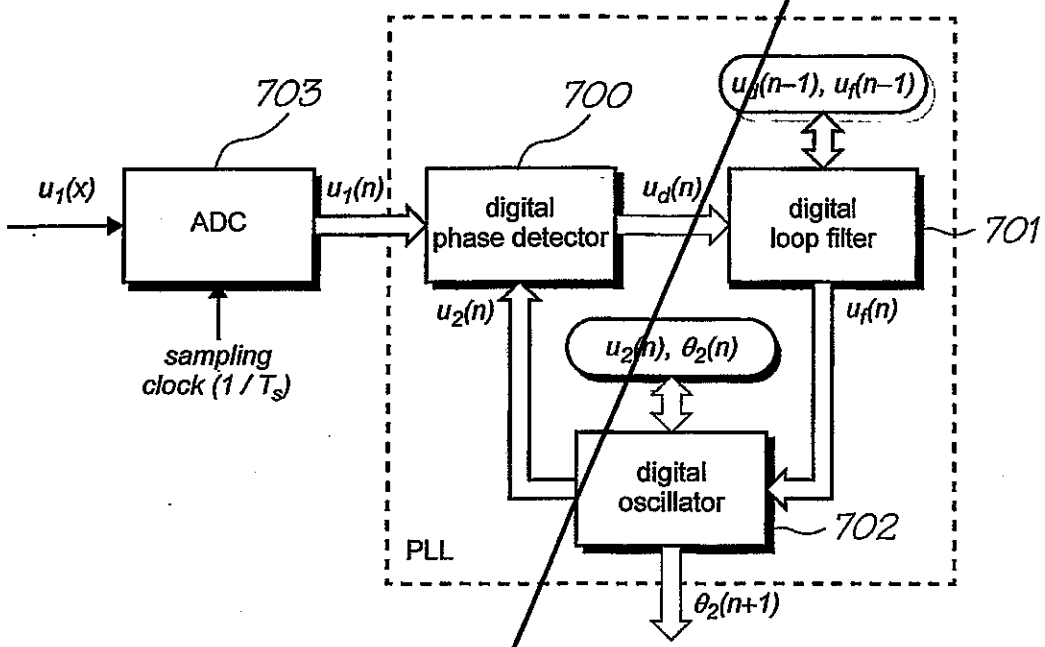

703
700
$u_d(n-1)$, $u_f(n-1)$
$u_1(x)$
ADC
$u_1(n)$
digital phase detector
$u_d(n)$
digital loop filter
701
$u_2(n)$
$u_f(n)$
$u_2(n)$, $\theta_2(n)$
sampling clock ($1 / T_s$)
digital oscillator
702
PLL
$\theta_2(n+1)$

FIG. 13

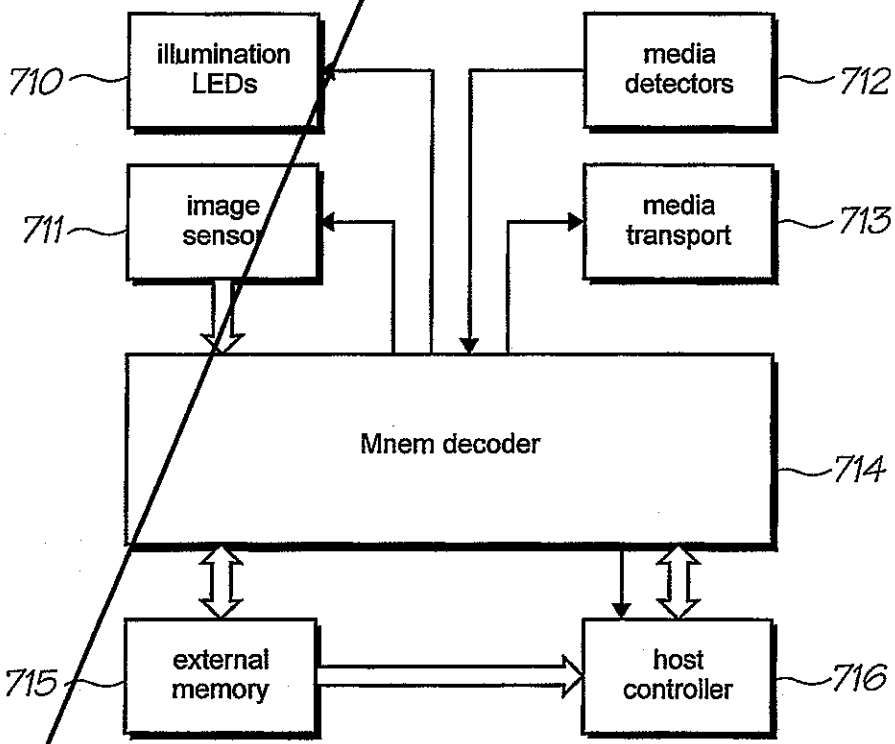

710
illumination LEDs
media detectors
712
711
image sensor
media transport
713
Mnem decoder
714
715
external memory
host controller
716

FIG. 14

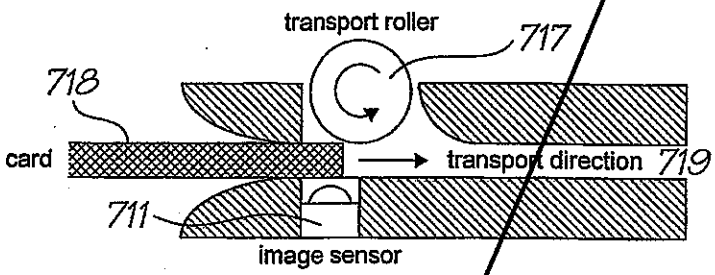

transport roller
717
718
card
transport direction
719
711
image sensor

FIG. 15

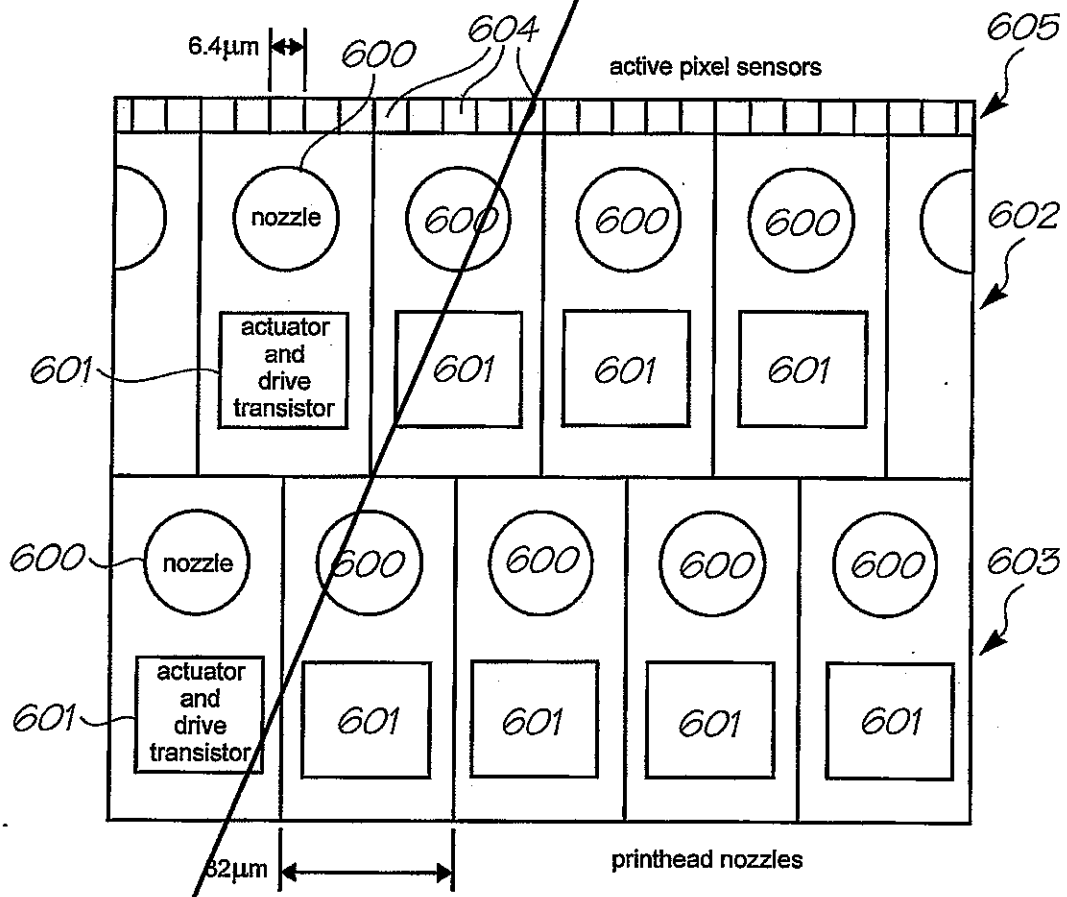

6.4µm
600
604
active pixel sensors
605
nozzle
602
actuator and drive transistor
601
603
32µm
printhead nozzles

FIG. 16

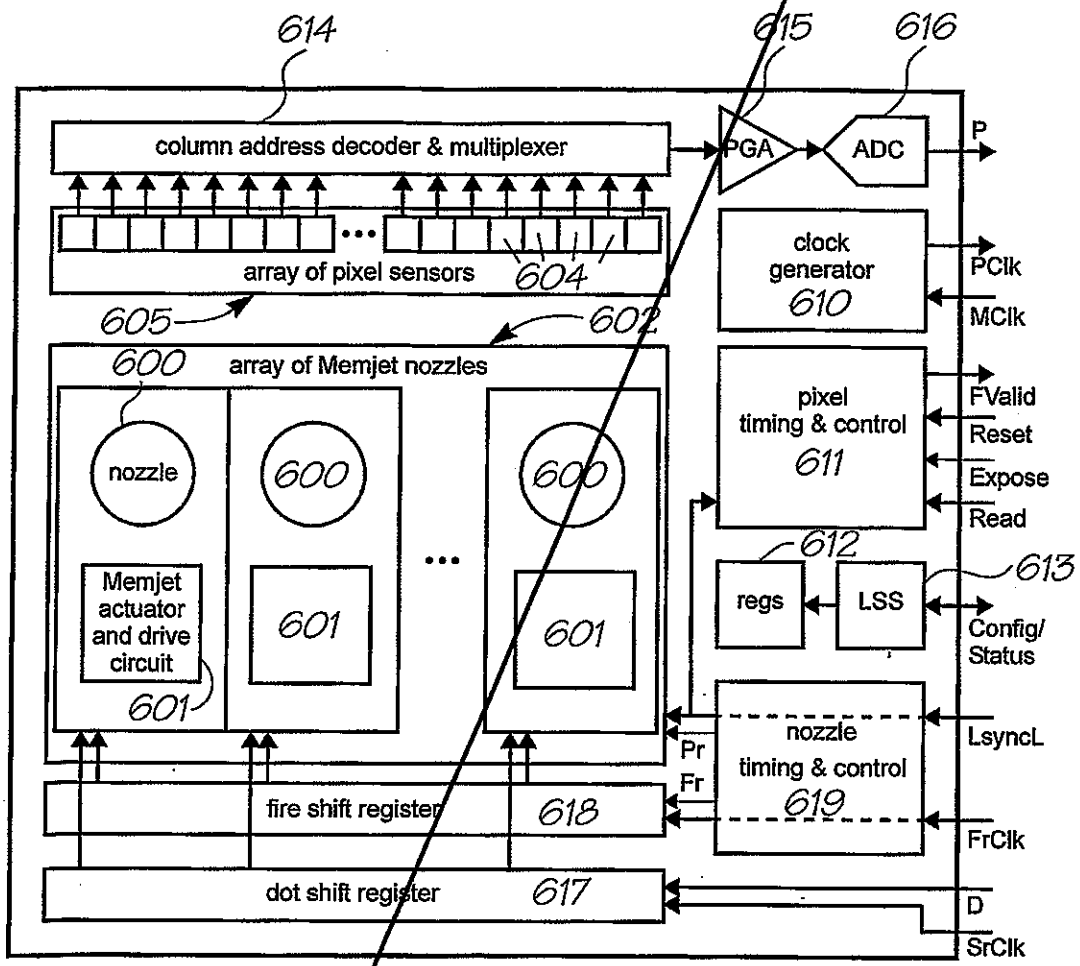

614
615
616
column address decoder & multiplexer
PGA
ADC
P
array of pixel sensors
604
clock generator
610
PClk
MClk
605
602
600
array of Memjet nozzles
nozzle
600
600
pixel timing & control
611
FValid
Reset
Expose
Read
612
613
regs
LSS
Config/ Status
Memjet actuator and drive circuit
601
601
601
Pr
Fr
nozzle timing & control
619
LsyncL
FrClk
fire shift register
618
dot shift register
617
D
SrClk

FIG. 17

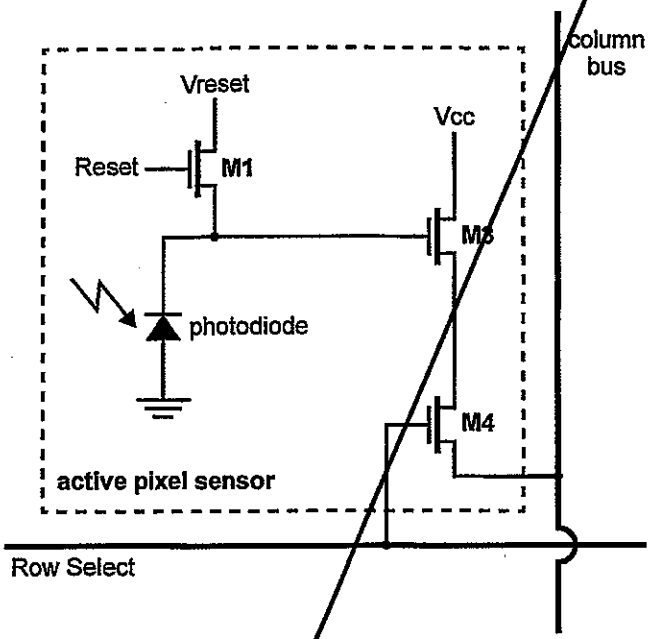

column bus
Vreset
Vcc
Reset
M1
M3
photodiode
M4
active pixel sensor
Row Select

FIG. 18

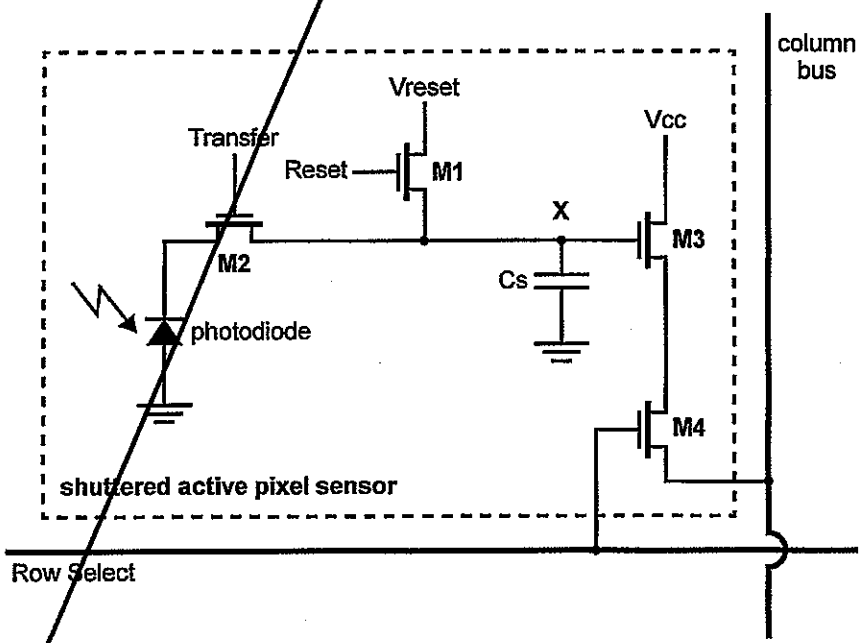

column bus
Vreset
Vcc
Transfer
Reset
M1
X
M3
M2
Cs
photodiode
M4
shuttered active pixel sensor
Row Select

FIG. 19

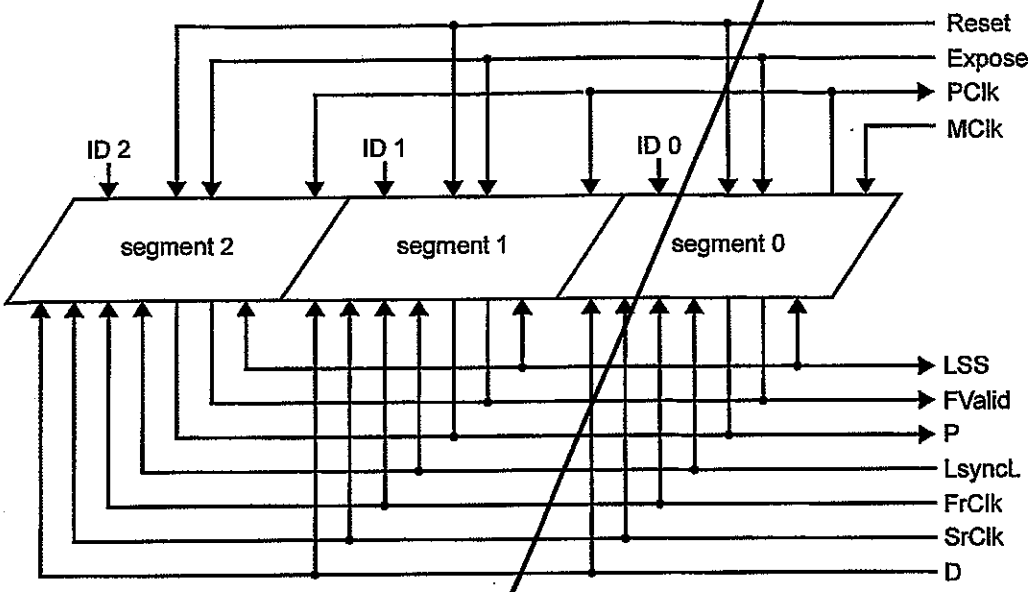

Reset
Expose
PClk
MClk
ID 2
ID 1
ID 0
segment 2
segment 1
segment 0
LSS
FValid
P
LsyncL
FrClk
SrClk
D

FIG. 20

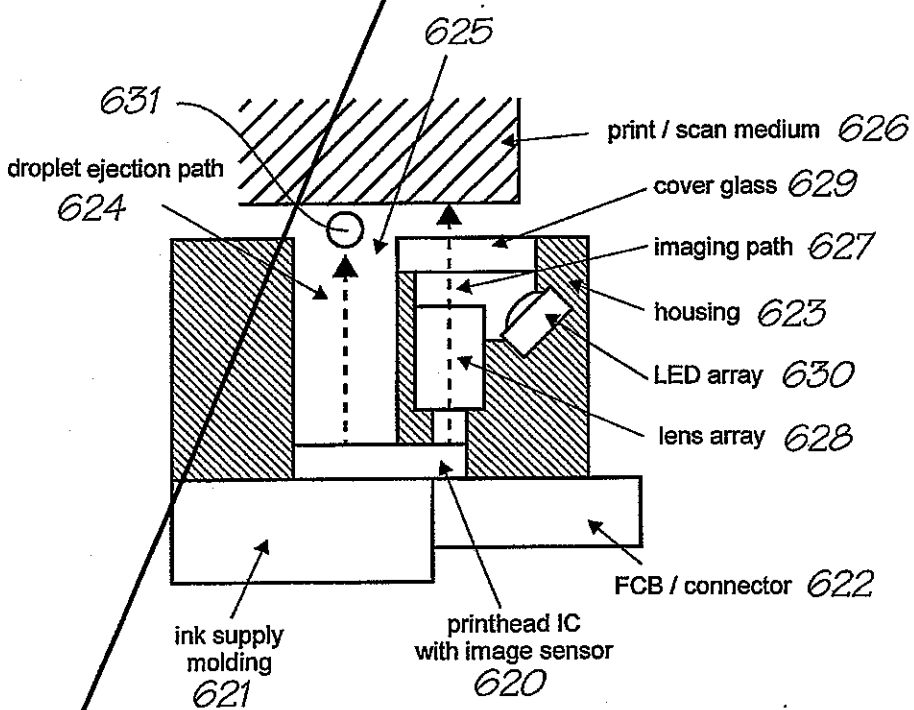

625
631
print / scan medium 626
droplet ejection path
624
cover glass 629
imaging path 627
housing 623
LED array 630
lens array 628
FCB / connector 622
ink supply
molding
621
printhead IC
with image sensor
620

FIG. 21

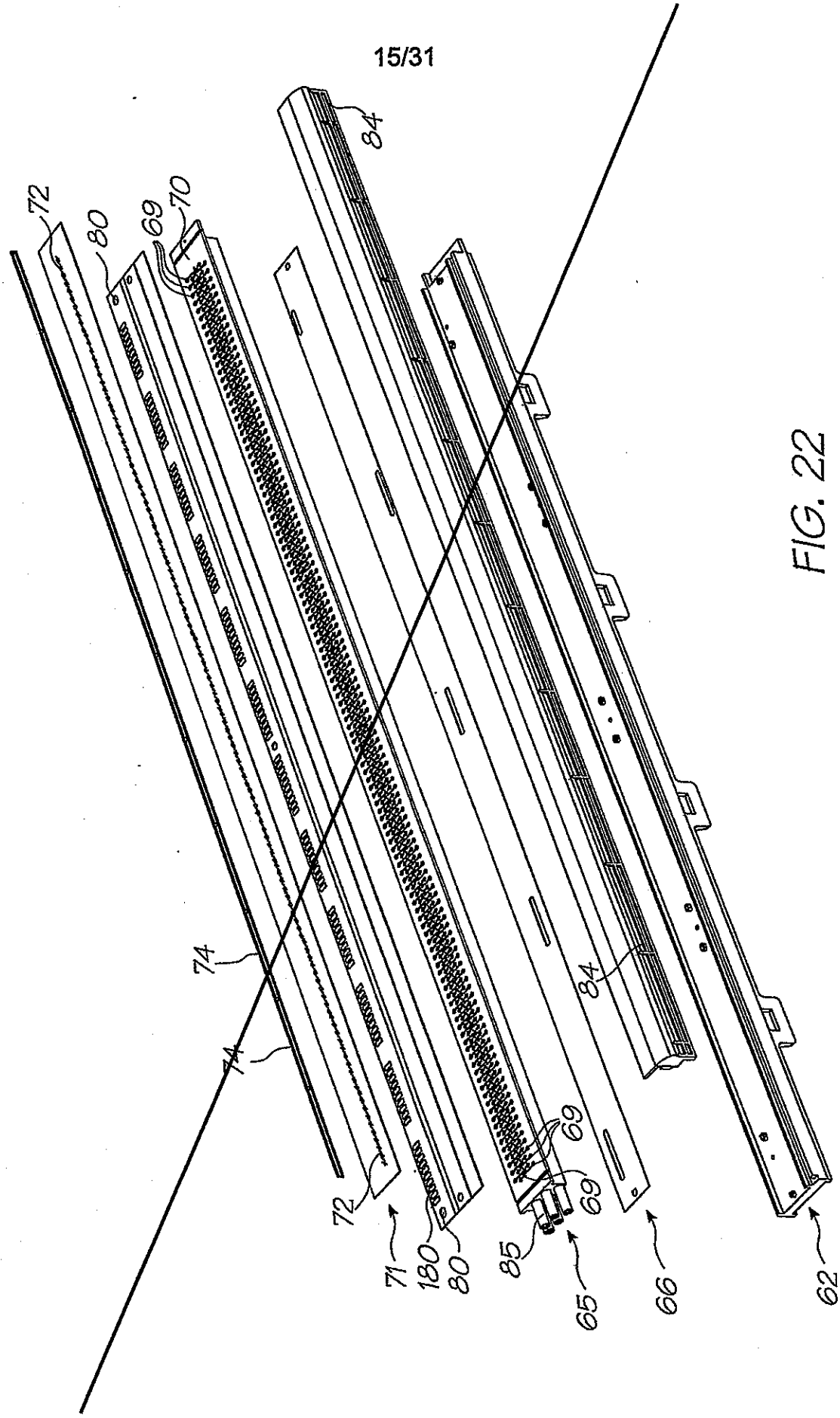


FIG. 22

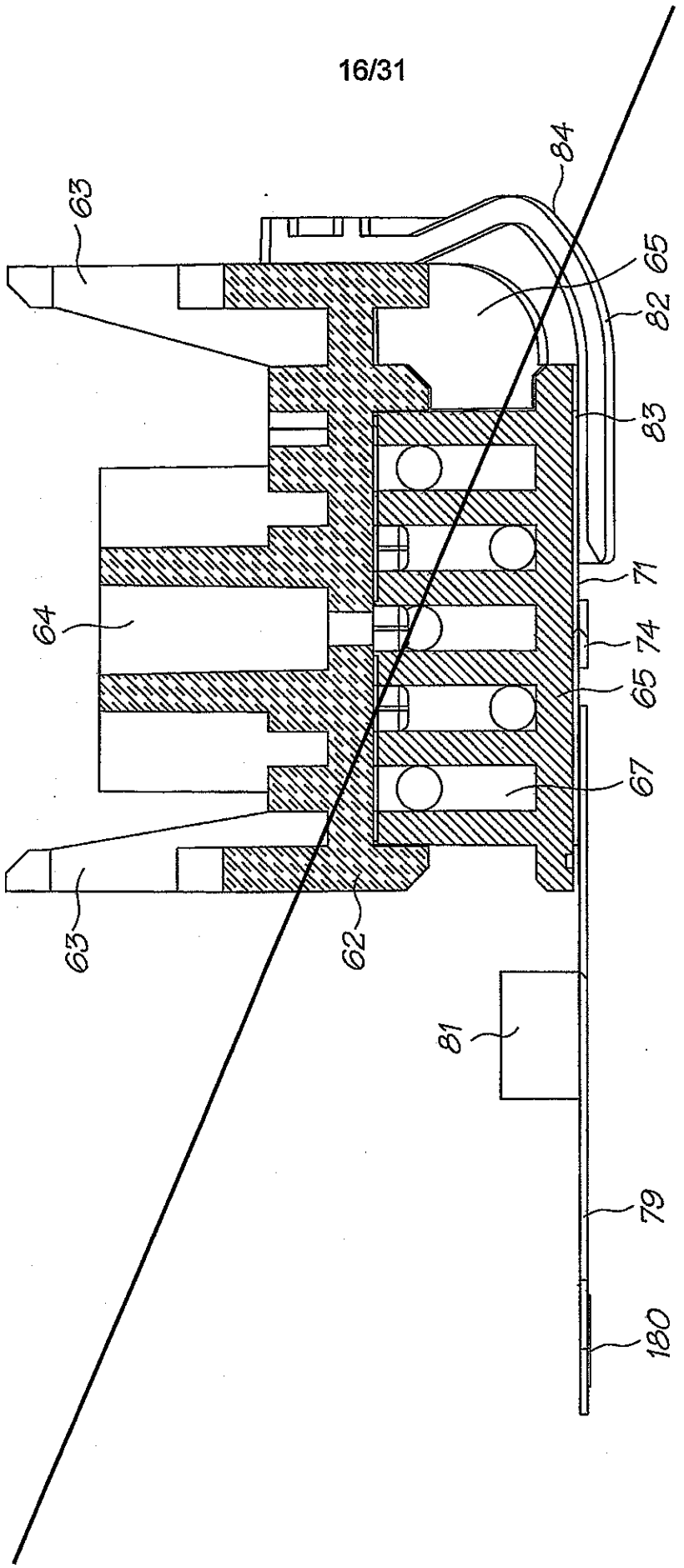


FIG. 23

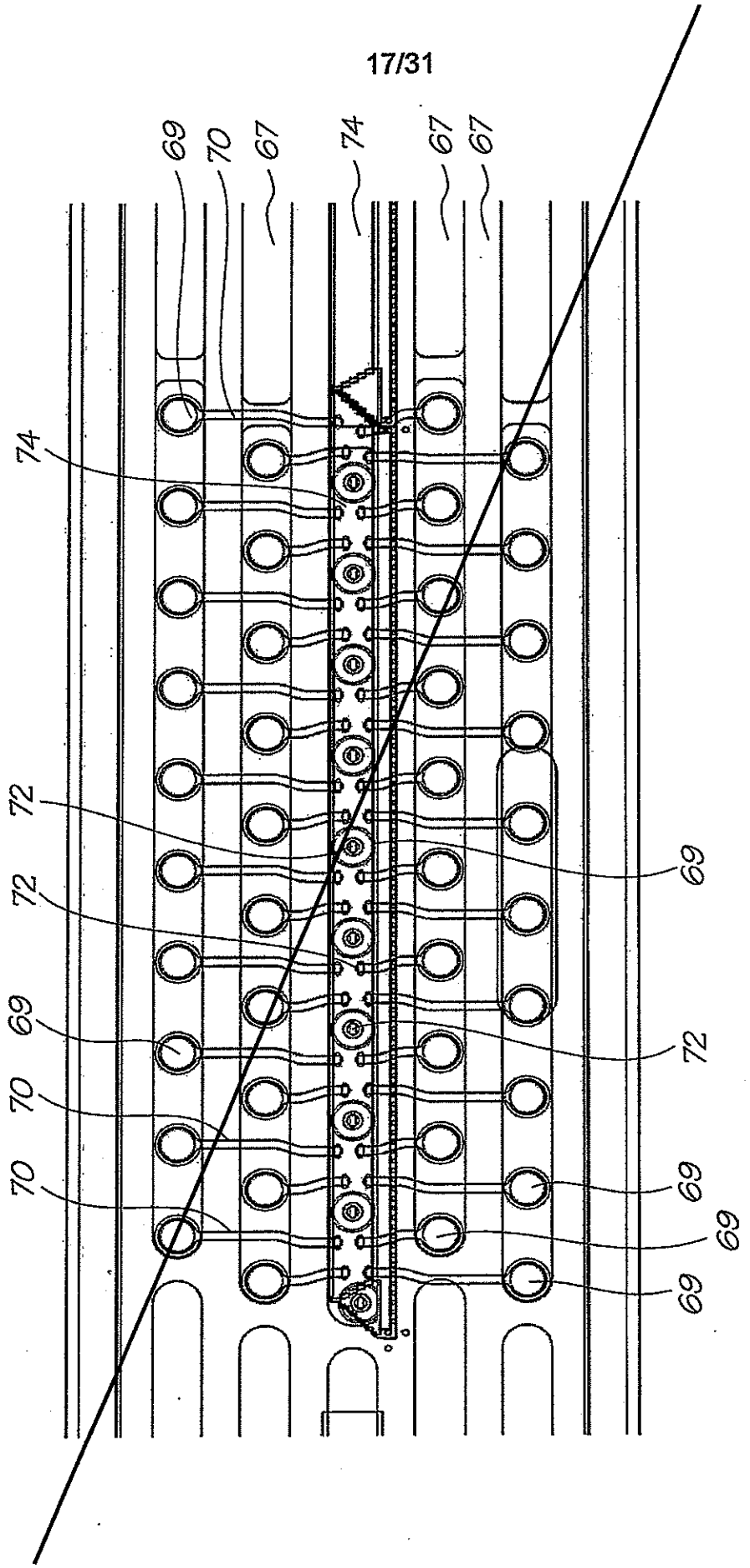


FIG. 24

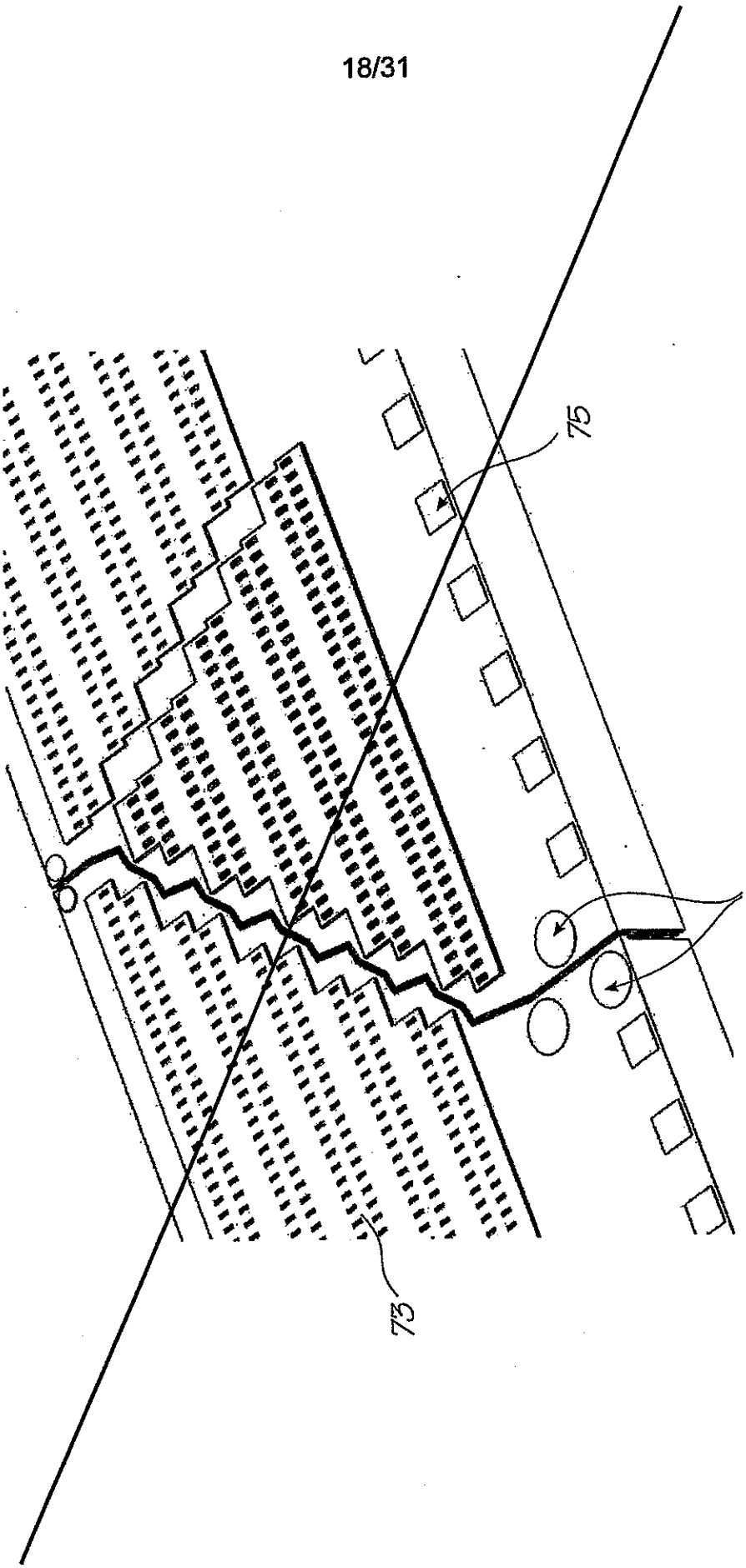


FIG. 25

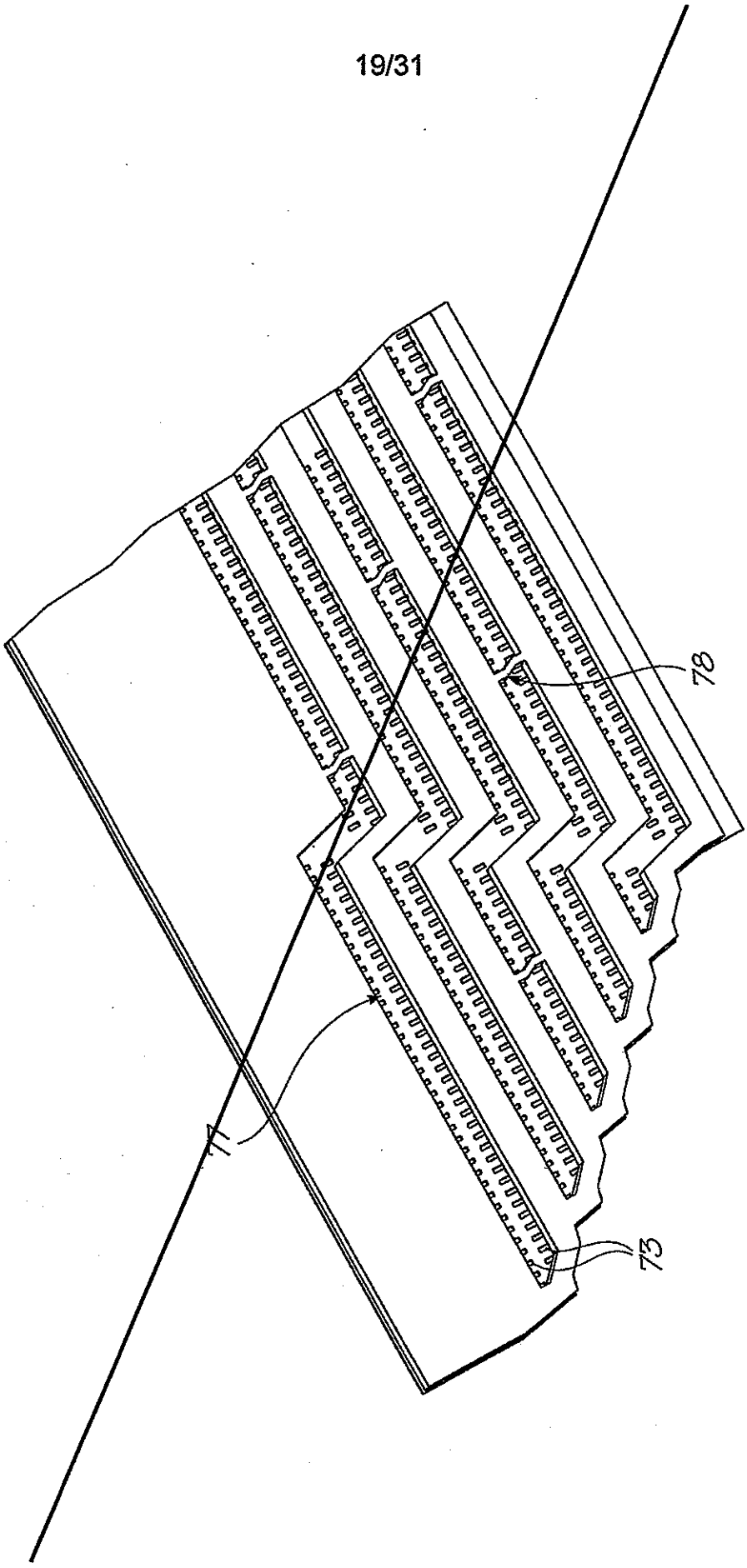


FIG. 26

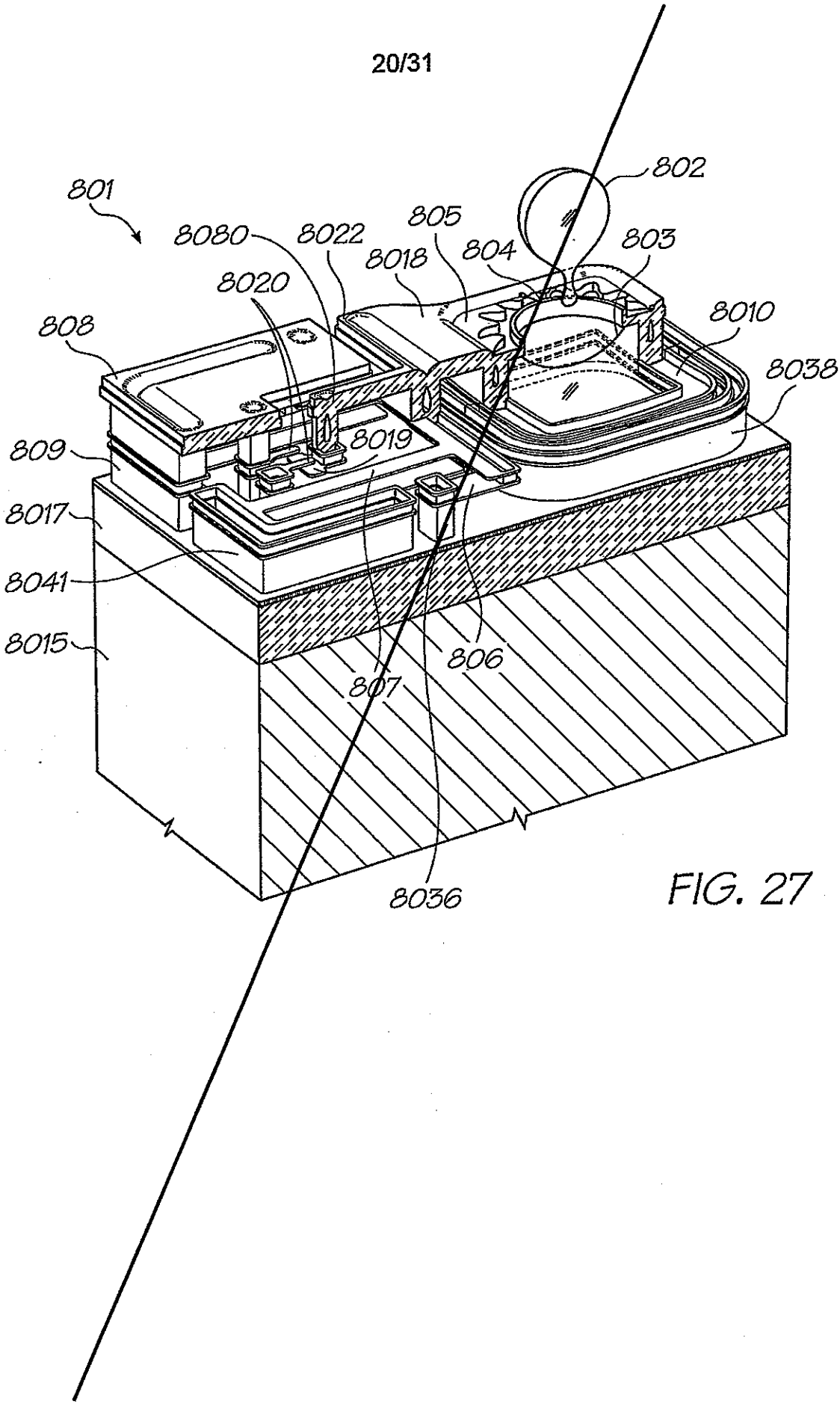

801
802
803
804
805
8080
8022
8018
8020
808
8010
8038
809
8019
8017
8041
8015
806
807
8036

FIG. 27

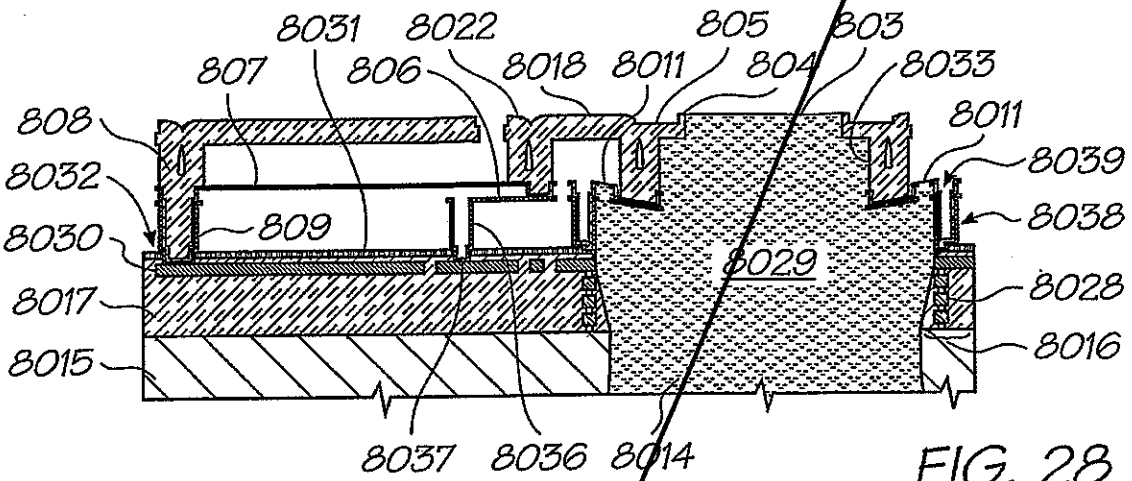


FIG. 28

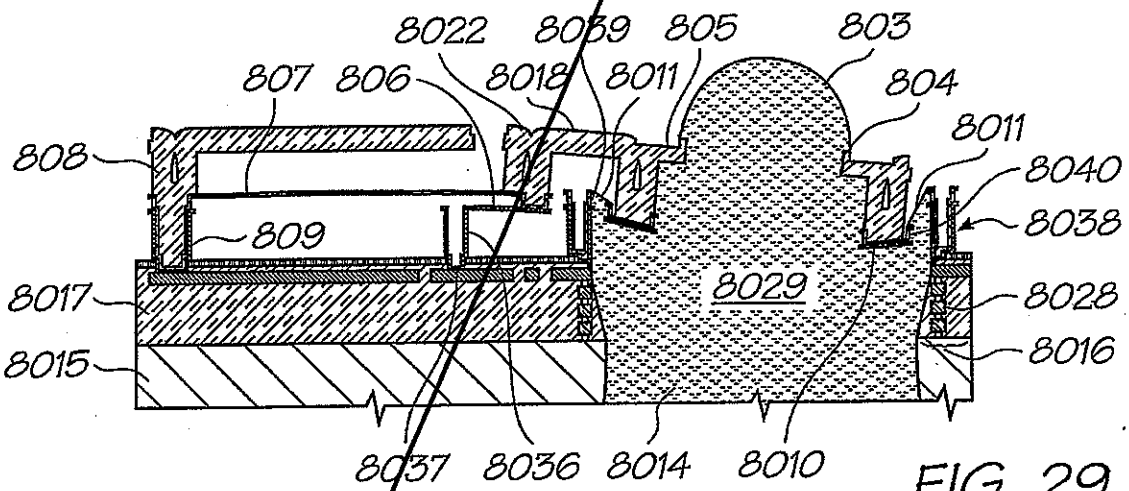


FIG. 29

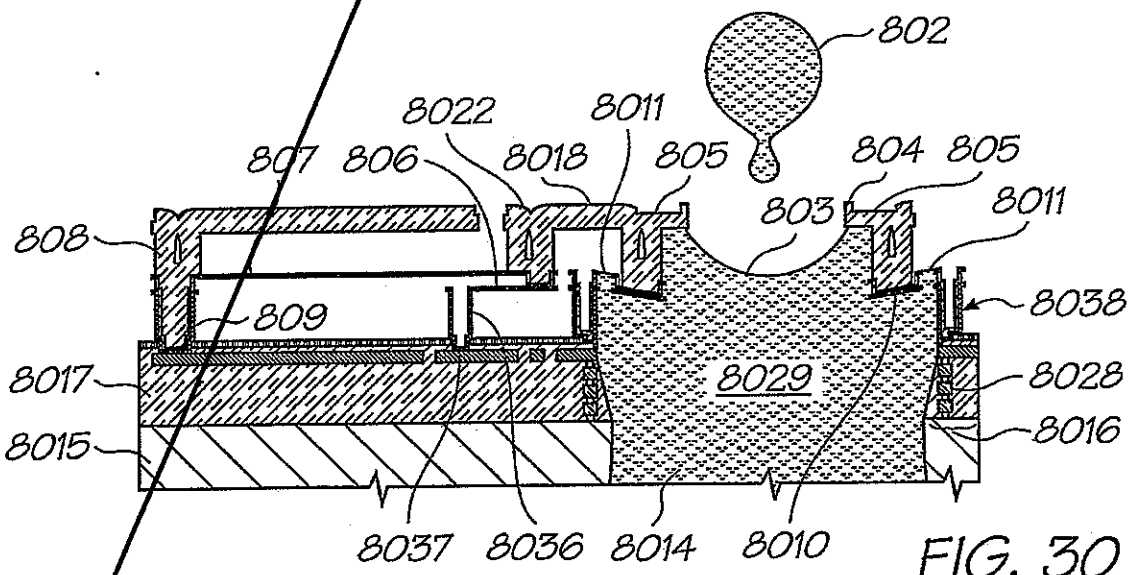


FIG. 30

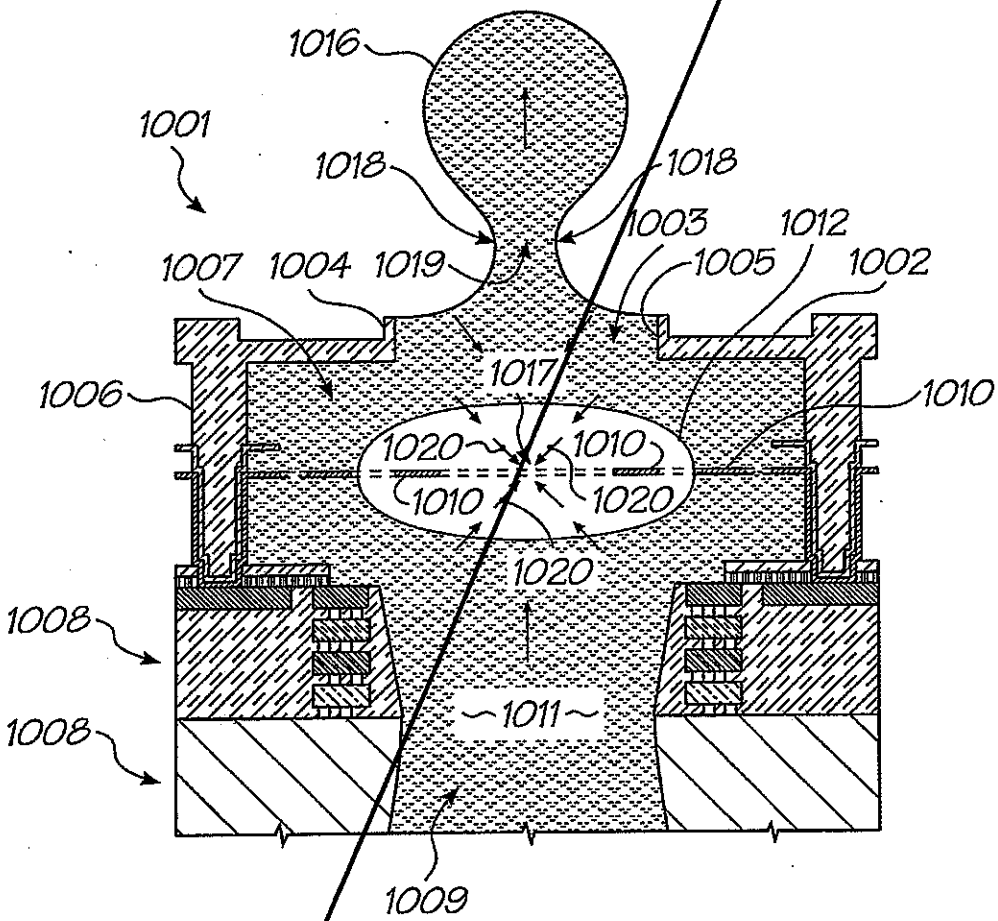

1016
1001
1018
1018
1003
1012
1007
1004
1019
1005
1002
1017
1006
1010
1020
1010
1010
1020
1020
1008
1011
1008
1009

FIG. 31

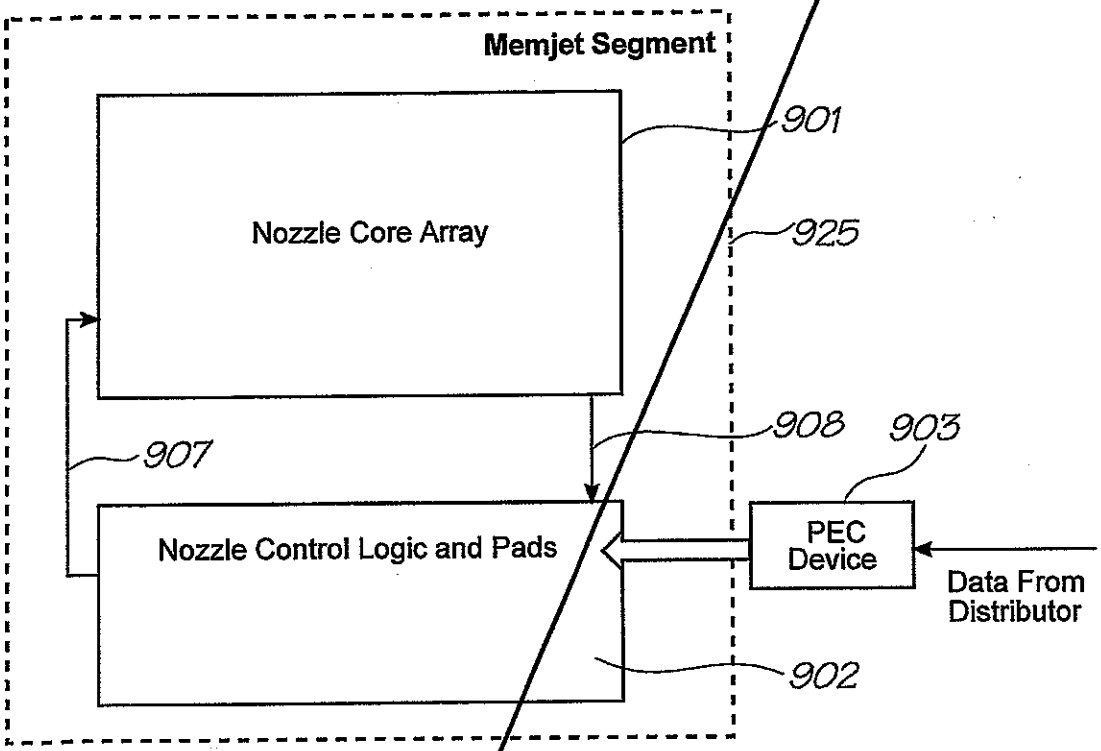

Memjet Segment
Nozzle Core Array
Nozzle Control Logic and Pads
PEC Device
Data From Distributor
901
925
908
903
907
902

FIG. 32

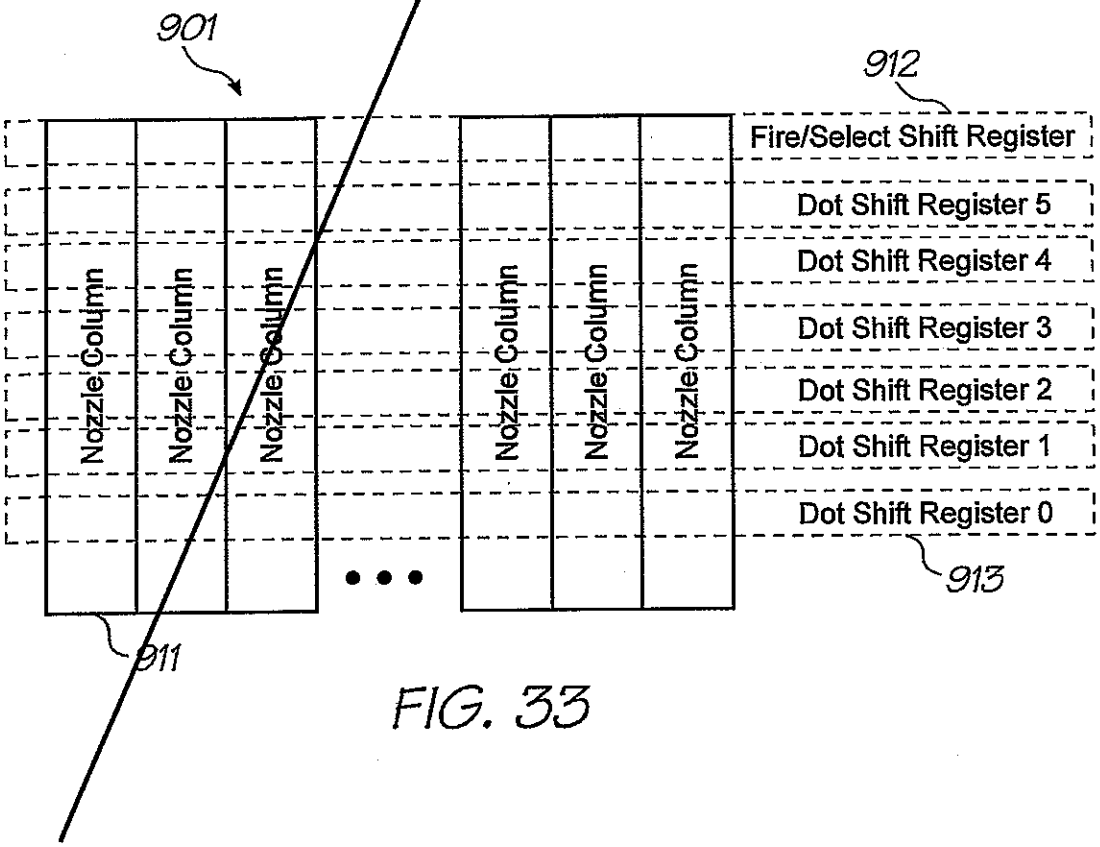

901
912
Fire/Select Shift Register
Dot Shift Register 5
Dot Shift Register 4
Dot Shift Register 3
Dot Shift Register 2
Dot Shift Register 1
Dot Shift Register 0
Nozzle Column
913
911

FIG. 33

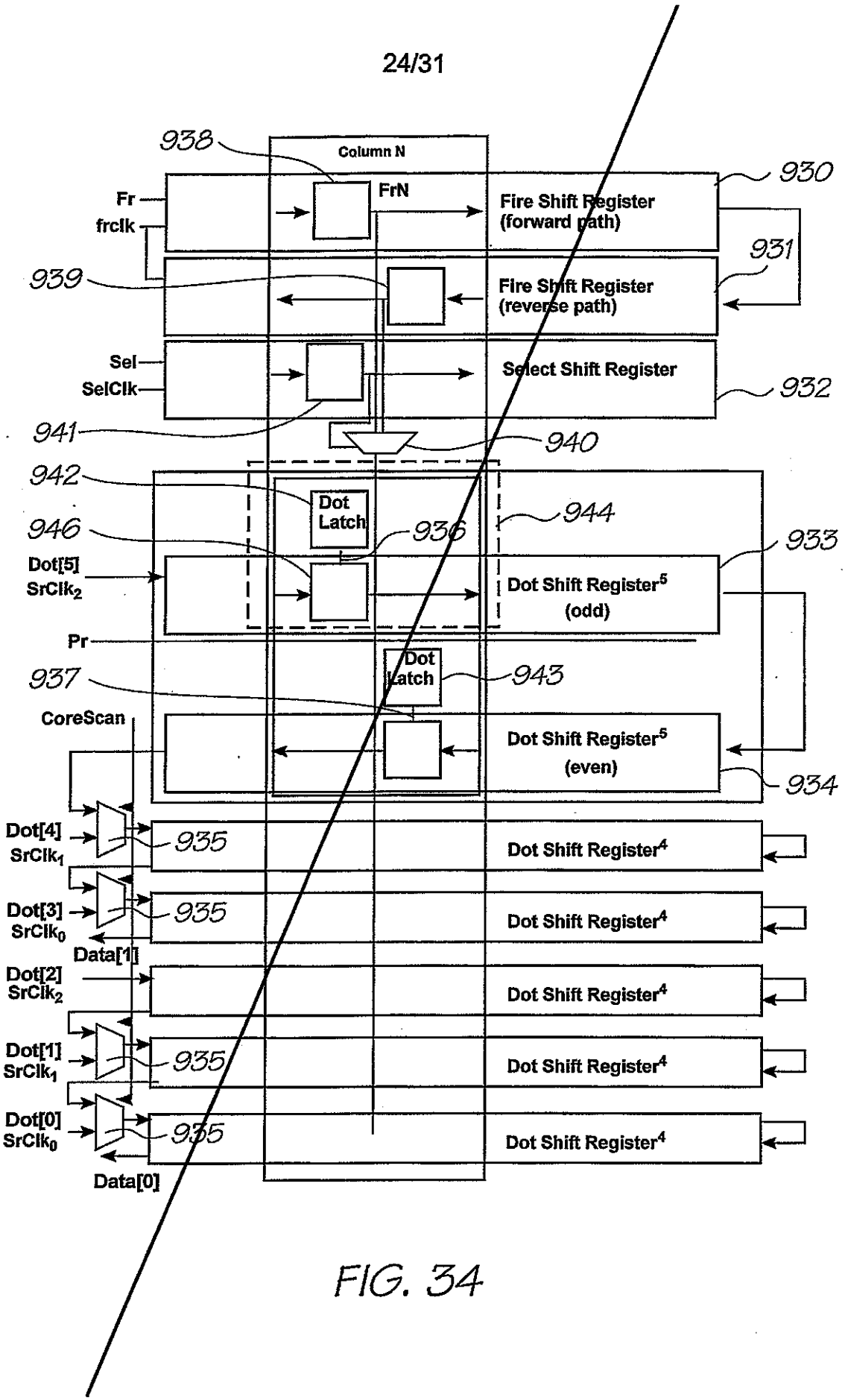

938
Column N
930
Fr
frclk
FrN
Fire Shift Register
(forward path)
931
939
Fire Shift Register
(reverse path)
Sel
SelClk
Select Shift Register
932
941
940
942
Dot
Latch
944
946
936
933
Dot[5]
SrClk2
Dot Shift Register5
(odd)
Pr
Dot
Latch
943
937
CoreScan
Dot Shift Register5
(even)
934
Dot[4]
SrClk1
935
Dot Shift Register4
Dot[3]
SrClk0
935
Dot Shift Register4
Data[1]
Dot[2]
SrClk2
Dot Shift Register4
Dot[1]
SrClk1
935
Dot Shift Register4
Dot[0]
SrClk0
935
Dot Shift Register4
Data[0]

FIG. 34

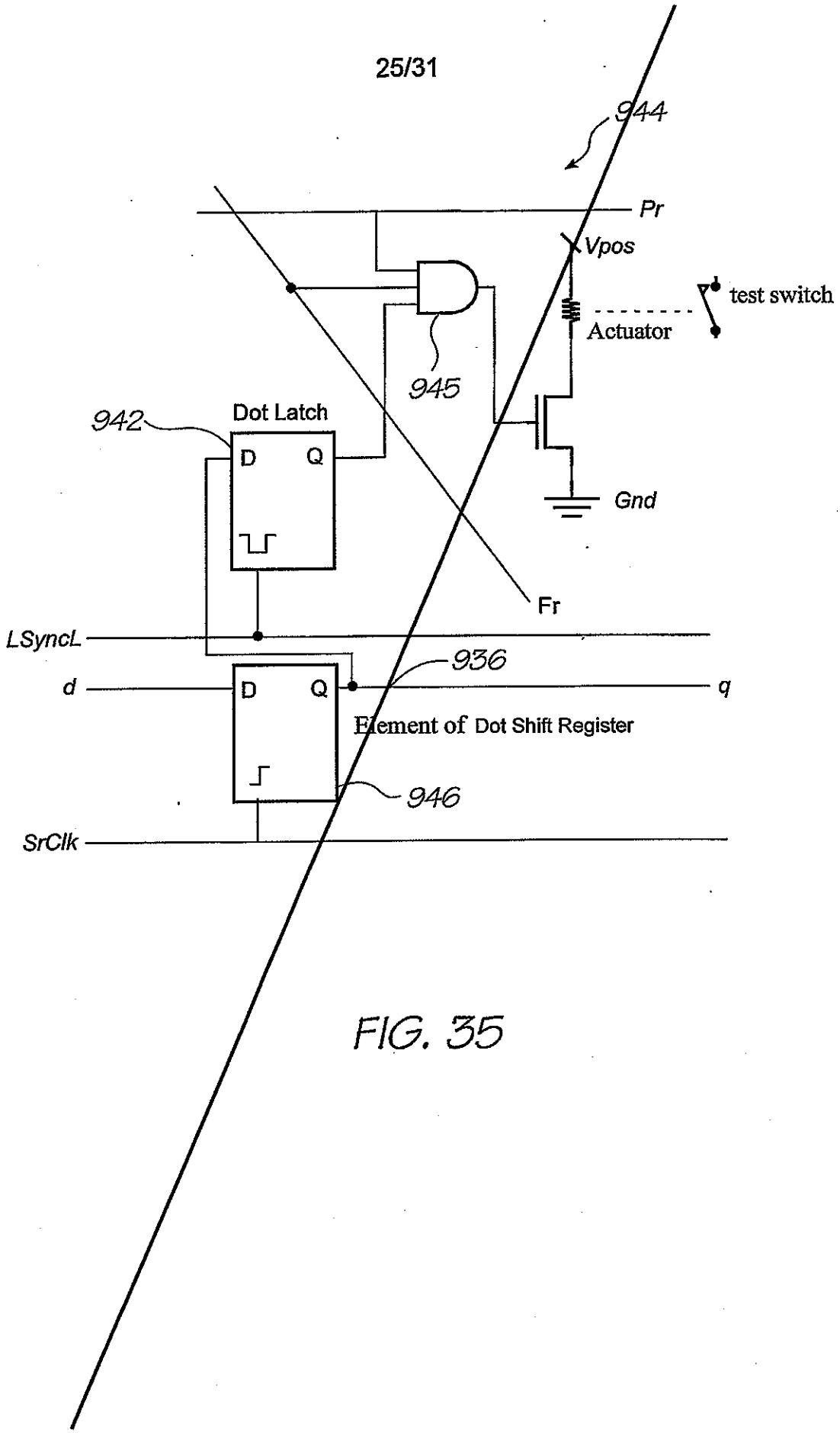

944
Pr
Vpos
test switch
Actuator
945
942
Dot Latch
D
Q
Gnd
Fr
LSyncL
936
d
D
Q
q
Element of Dot Shift Register
946
SrClk

FIG. 35

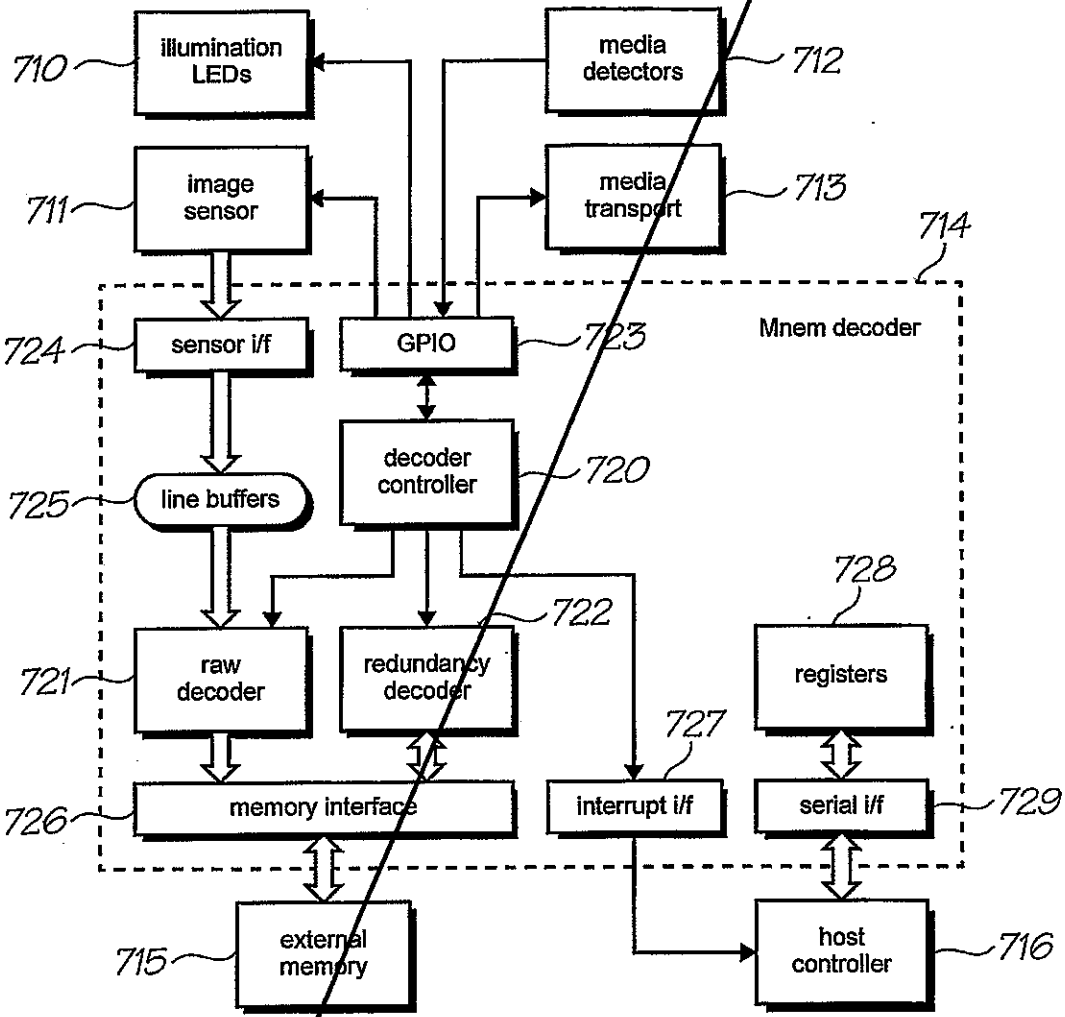

illumination LEDs
710
media detectors
712
image sensor
711
media transport
713
714
Mnem decoder
sensor i/f
724
GPIO
723
decoder controller
720
line buffers
725
728
722
raw decoder
721
redundancy decoder
registers
727
memory interface
726
interrupt i/f
serial i/f
729
external memory
715
host controller
716

FIG. 36

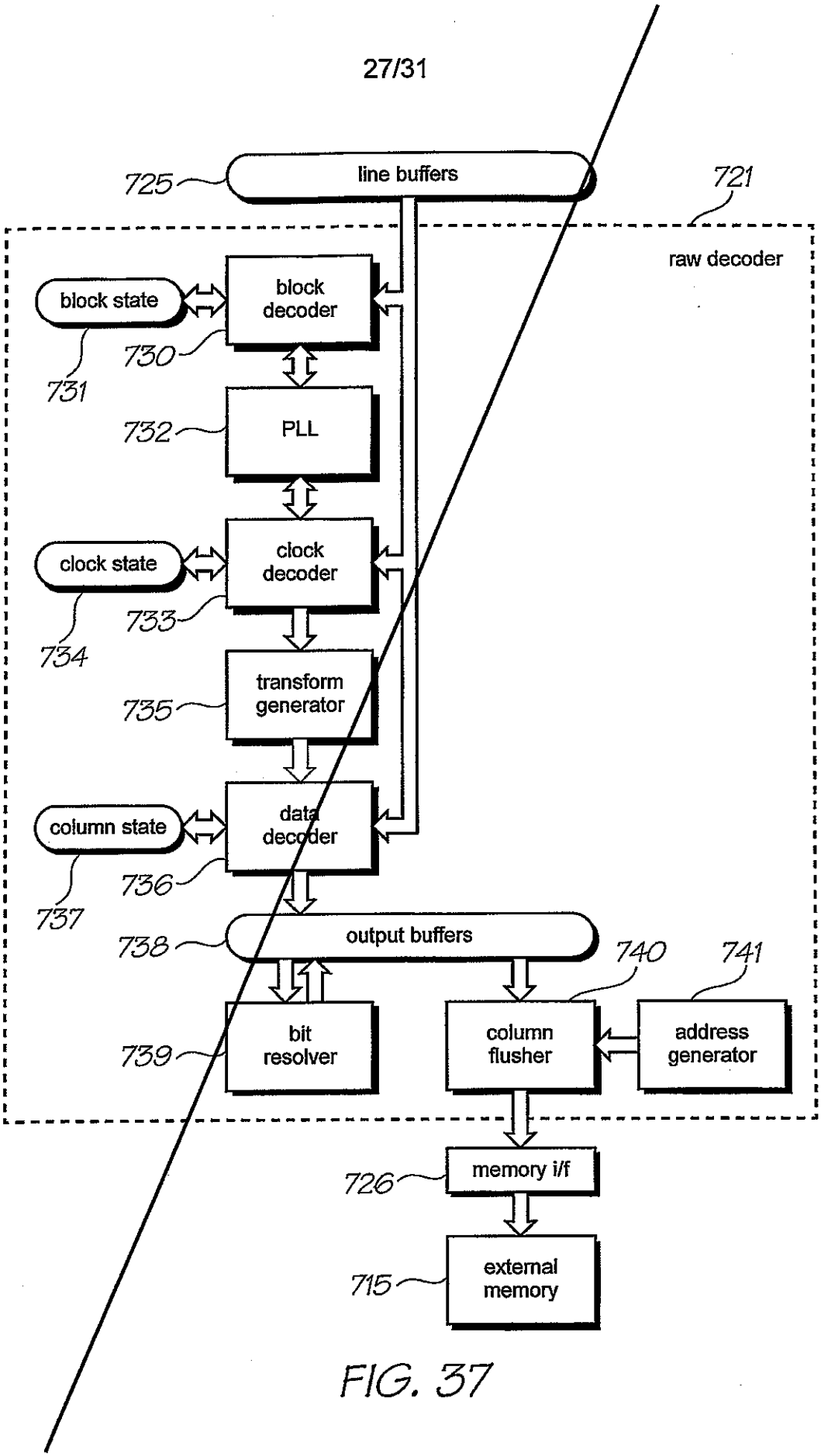

725
line buffers
721
raw decoder
block state
731
block decoder
730
732
PLL
clock state
734
clock decoder
733
transform generator
735
column state
737
data decoder
736
738
output buffers
740
741
bit resolver
739
column flusher
address generator
726
memory i/f
715
external memory

FIG. 37

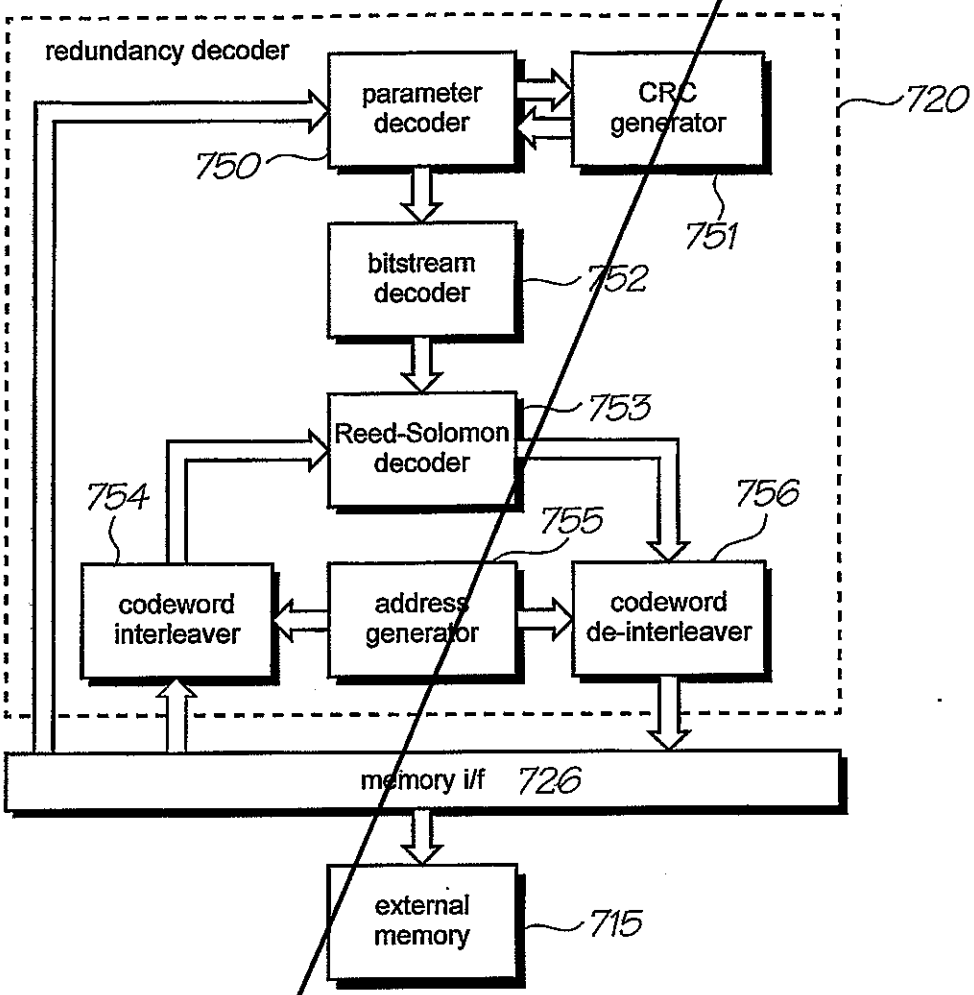

redundancy decoder
parameter decoder
CRC generator
720
750
751
bitstream decoder
752
753
Reed-Solomon decoder
754
755
756
codeword interleaver
address generator
codeword de-interleaver
memory i/f 726
external memory
715

FIG. 38

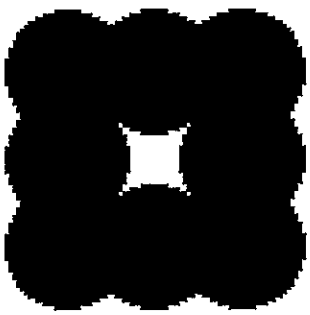


FIG. 39

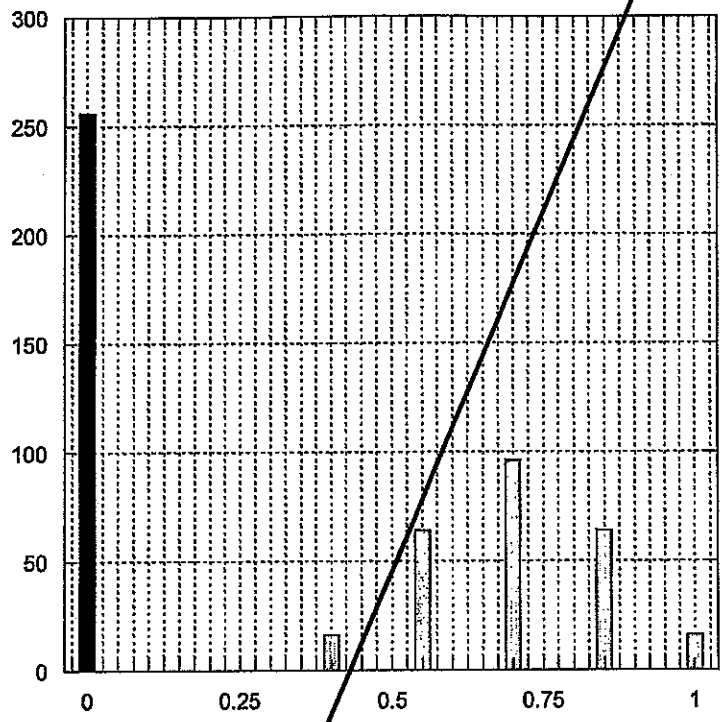


FIG. 40

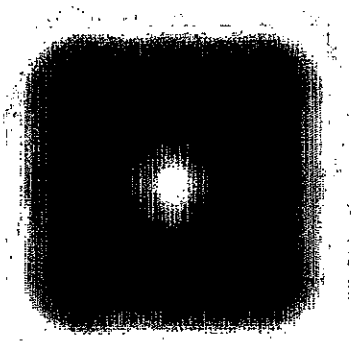


FIG. 41

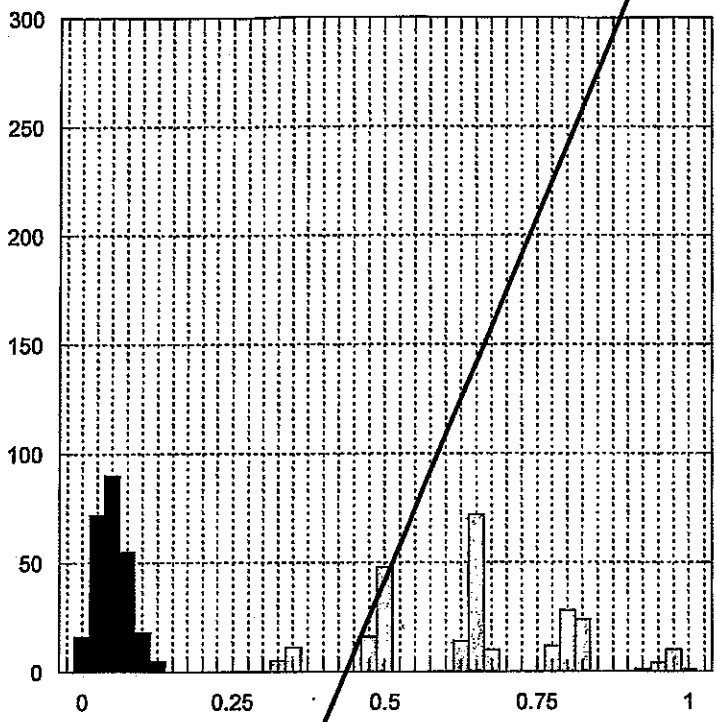


FIG. 42

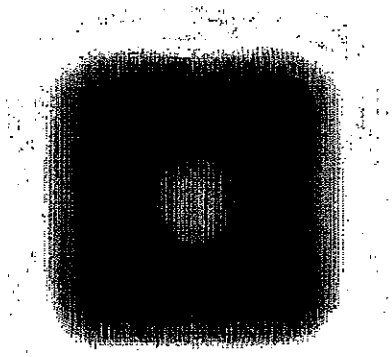


FIG. 43

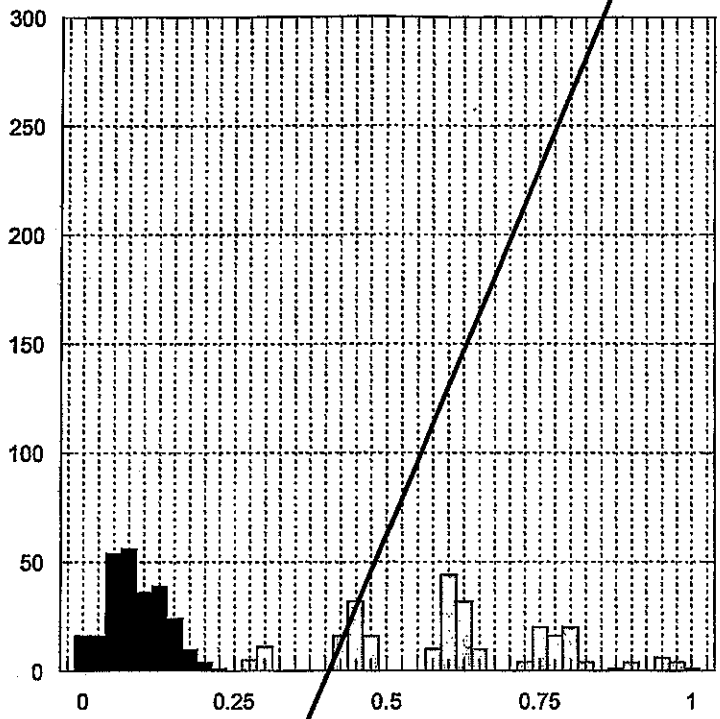


FIG. 44

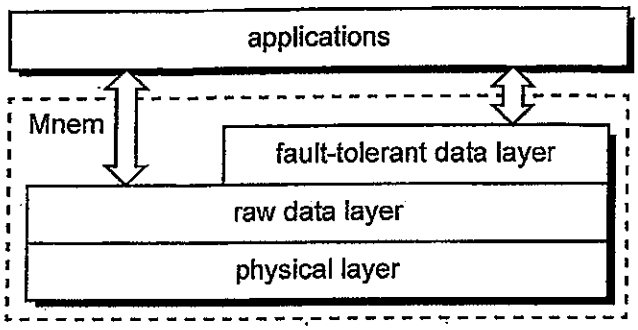

applications
Mnem
fault-tolerant data layer
raw data layer
physical layer

FIG. 1

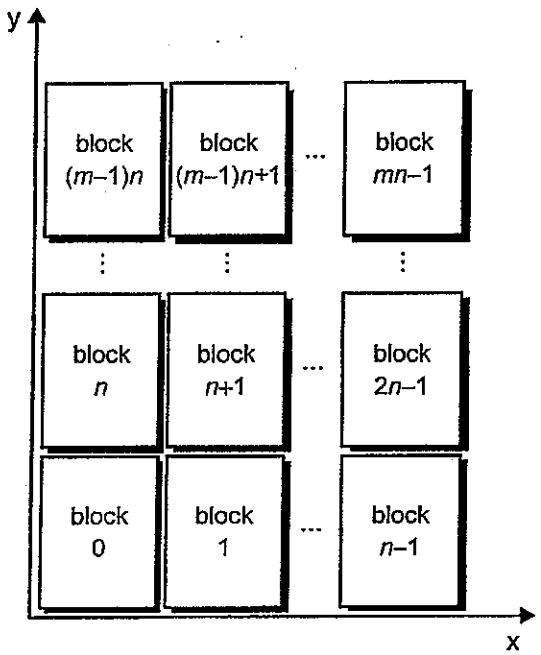

y
block (m–1)n
block (m–1)n+1
...
block mn–1
block n
block n+1
...
block 2n–1
block 0
block 1
...
block n–1
x

FIG. 2

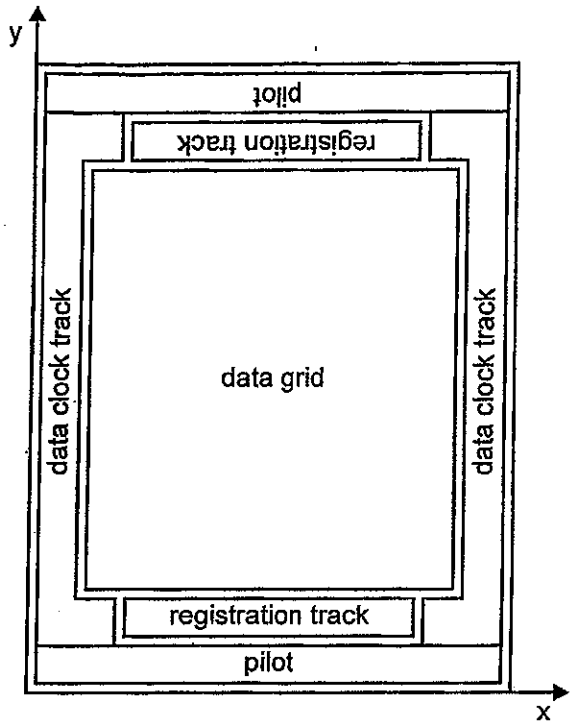

y
pilot
registration track
data clock track
data grid
data clock track
registration track
pilot
x

FIG. 3

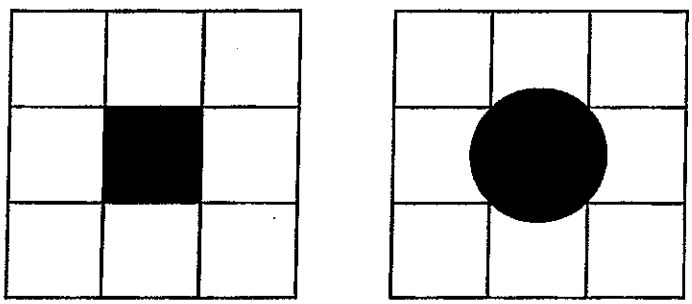


FIG. 4

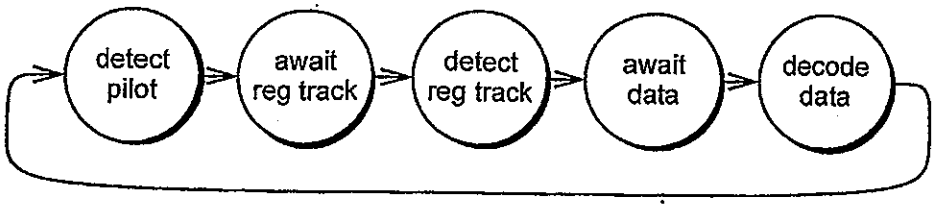

detect pilot
await reg track
detect reg track
await data
decode data

FIG. 5

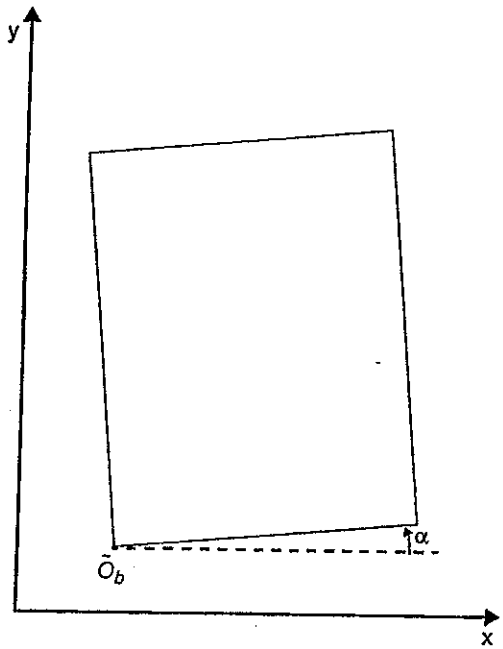

y
x
α
$\tilde{O}_b$

FIG. 6

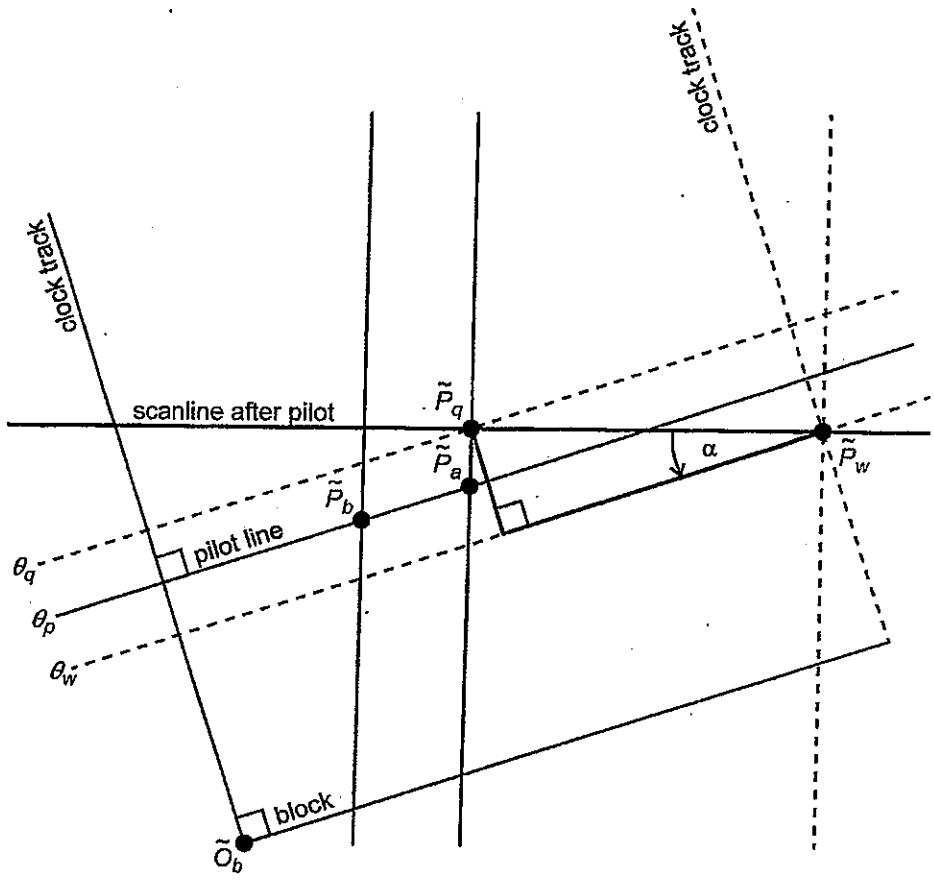

clock track
clock track
scanline after pilot
$\tilde{P}_q$
$\tilde{P}_a$
$\tilde{P}_b$
$\tilde{P}_w$
α
pilot line
θ_q
θ_p
θ_w
block
$\tilde{O}_b$

FIG. 7

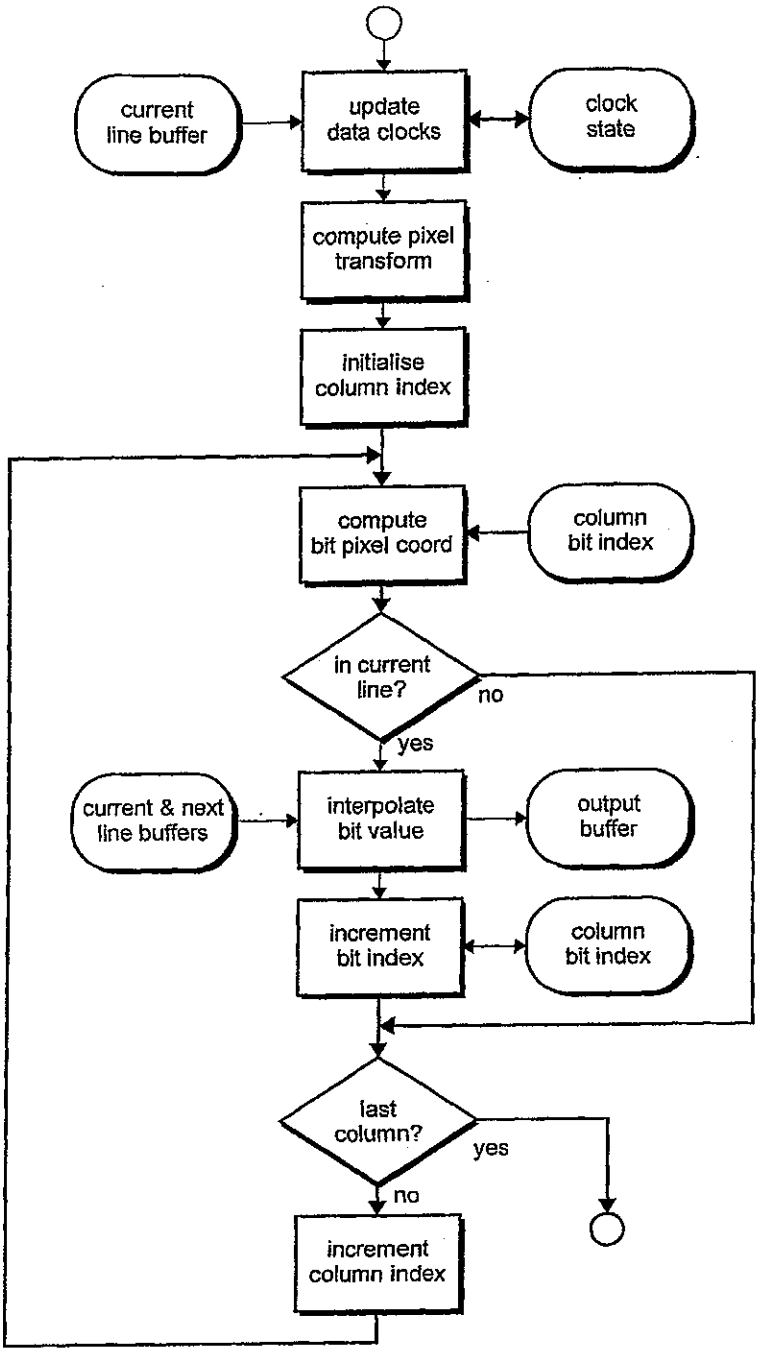

current line buffer
update data clocks
clock state
compute pixel transform
initialise column index
compute bit pixel coord
column bit index
in current line?
no
yes
current & next line buffers
interpolate bit value
output buffer
increment bit index
column bit index
last column?
yes
no
increment column index

FIG. 8

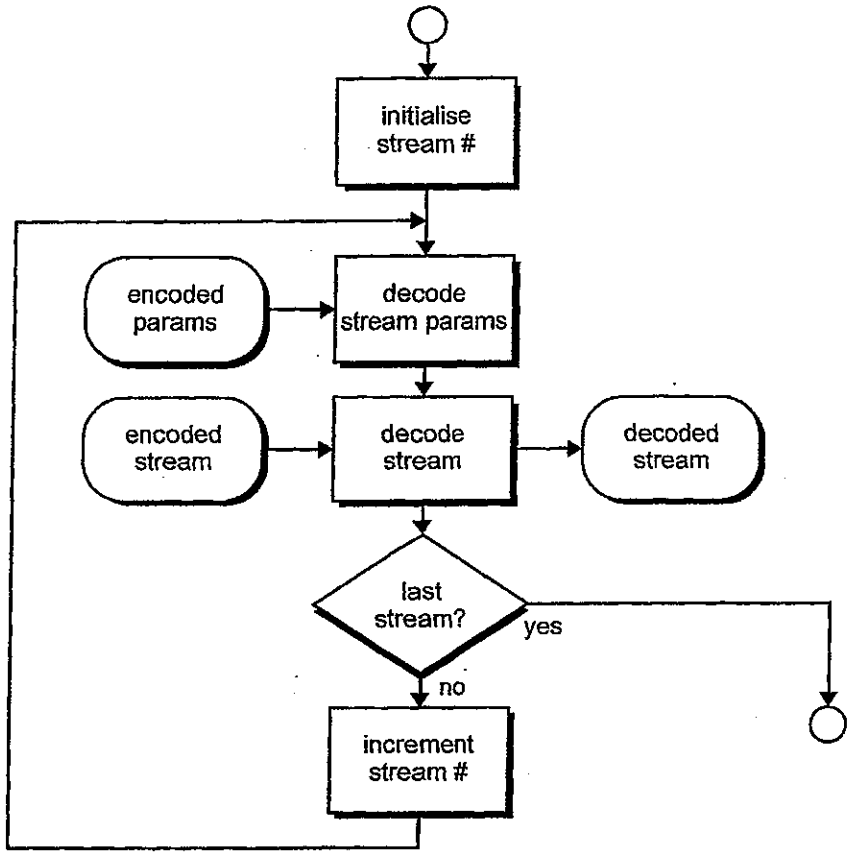

initialise stream #
encoded params
decode stream params
encoded stream
decode stream
decoded stream
last stream?
yes
no
increment stream #

FIG. 9

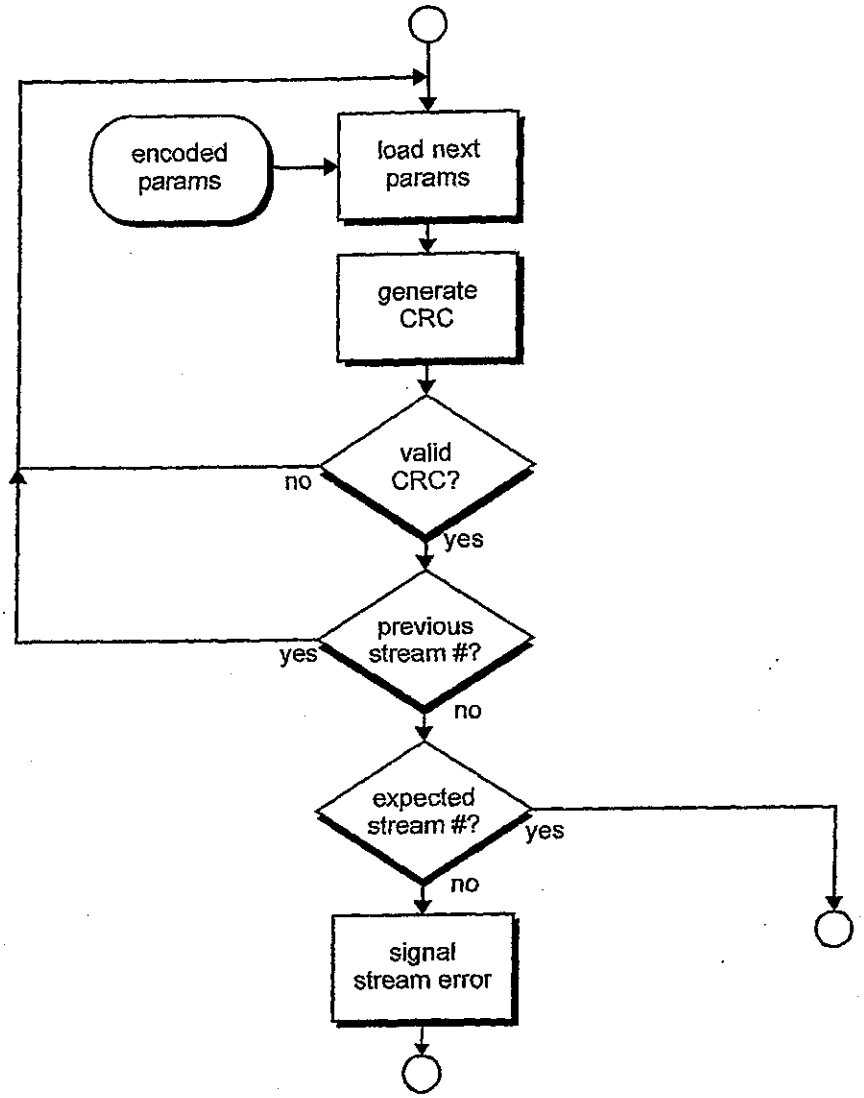

encoded params
load next params
generate CRC
valid CRC?
no
yes
previous stream #?
yes
no
expected stream #?
yes
no
signal stream error

FIG. 10

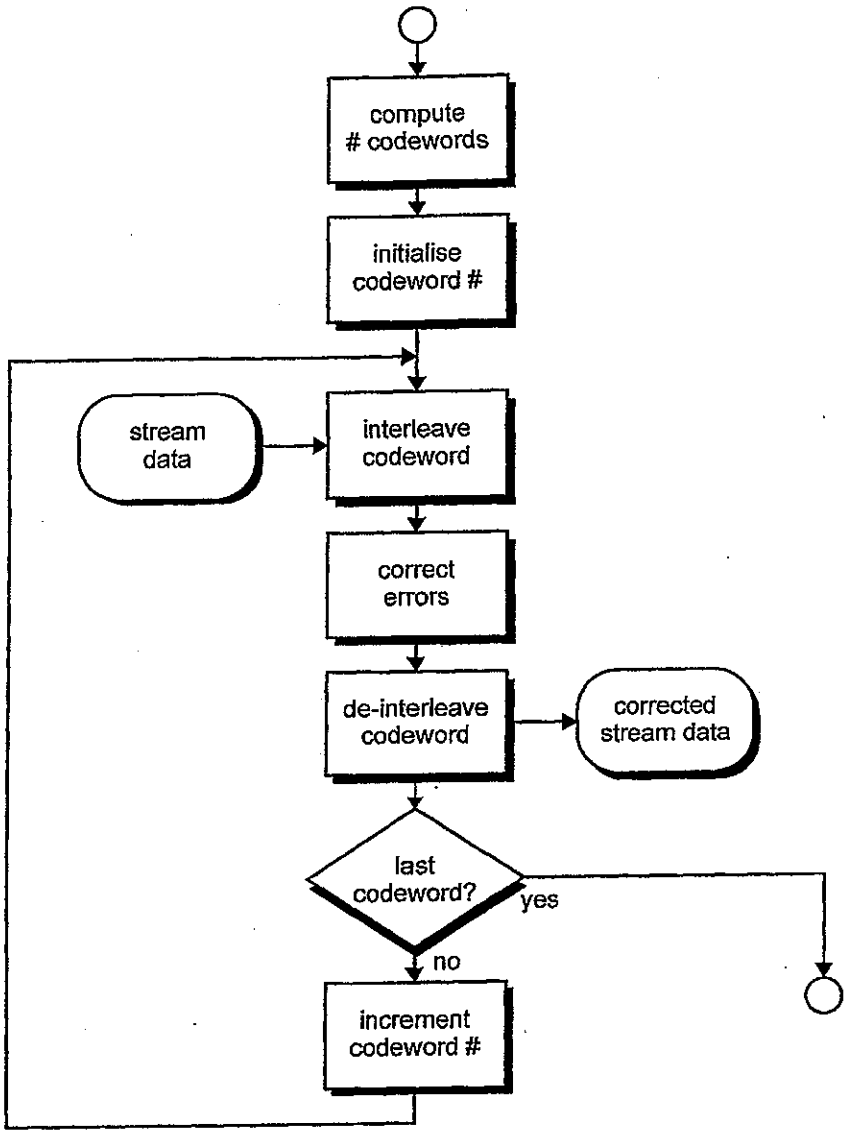

compute
codewords
initialise
codeword #
stream
data
interleave
codeword
correct
errors
de-interleave
codeword
corrected
stream data
last
codeword?
yes
no
increment
codeword #

FIG. 11

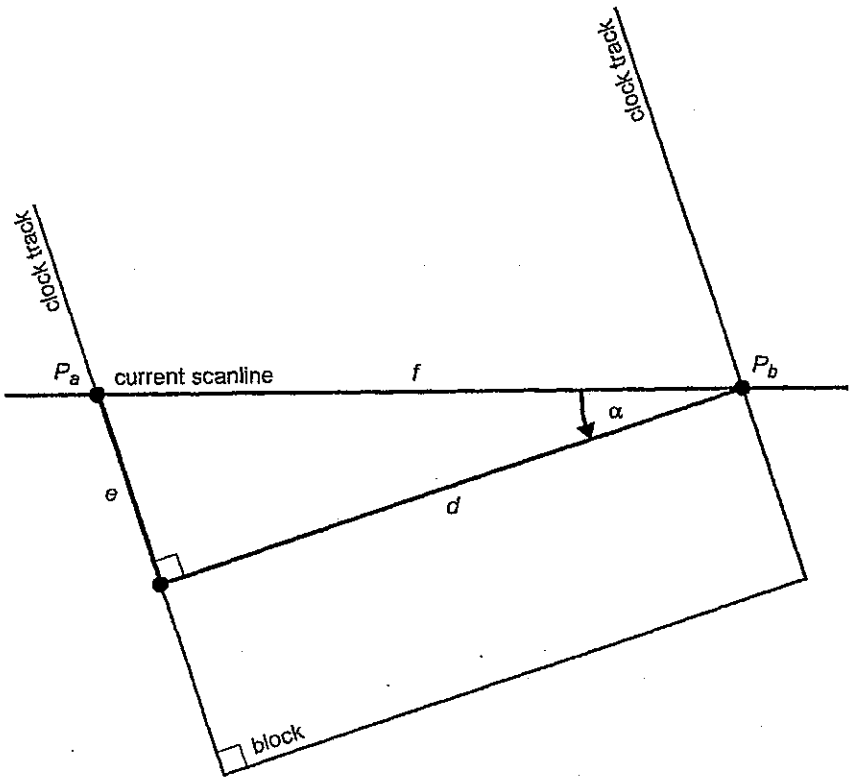


FIG. 12

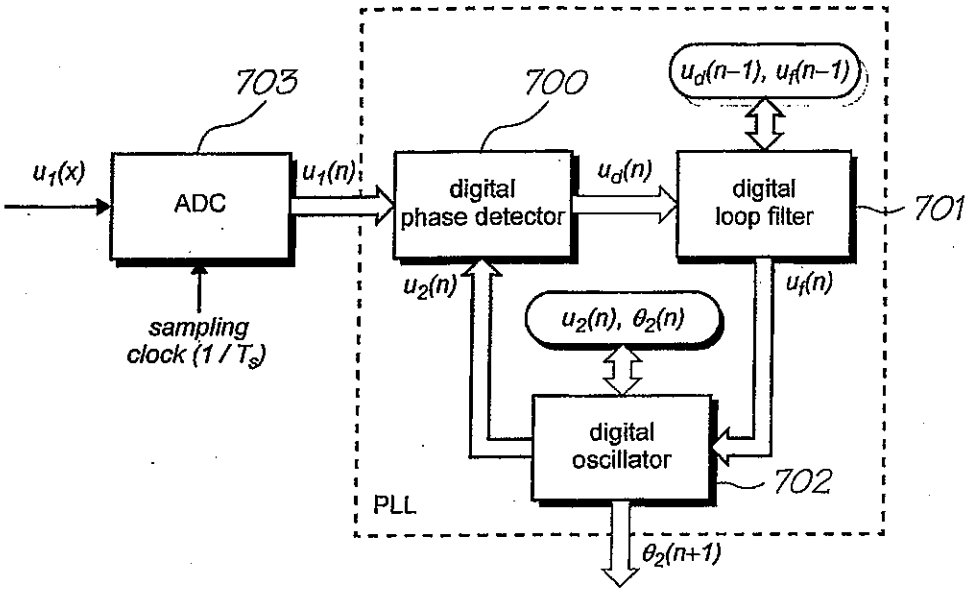

703
700
$u_d(n-1)$, $u_f(n-1)$
$u_1(x)$
ADC
$u_1(n)$
digital phase detector
$u_d(n)$
digital loop filter
701
$u_2(n)$
$u_f(n)$
$u_2(n)$, $\theta_2(n)$
sampling clock ($1 / T_s$)
digital oscillator
702
PLL
$\theta_2(n+1)$

FIG. 13

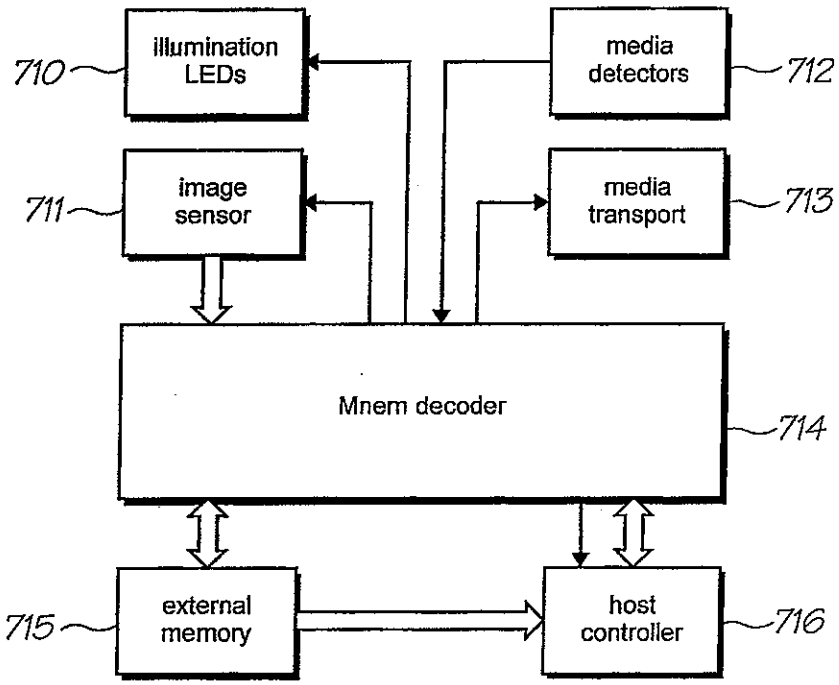

710
illumination LEDs
media detectors
712
711
image sensor
media transport
713
Mnem decoder
714
715
external memory
host controller
716

FIG. 14

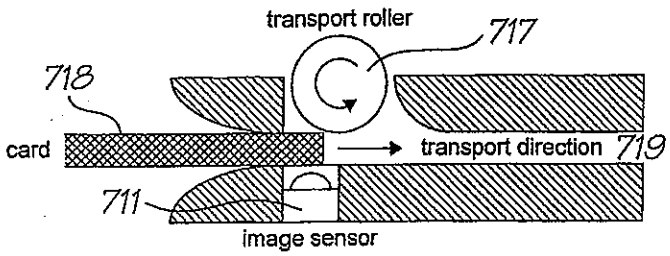

transport roller
717
718
card
transport direction
719
711
image sensor

FIG. 15

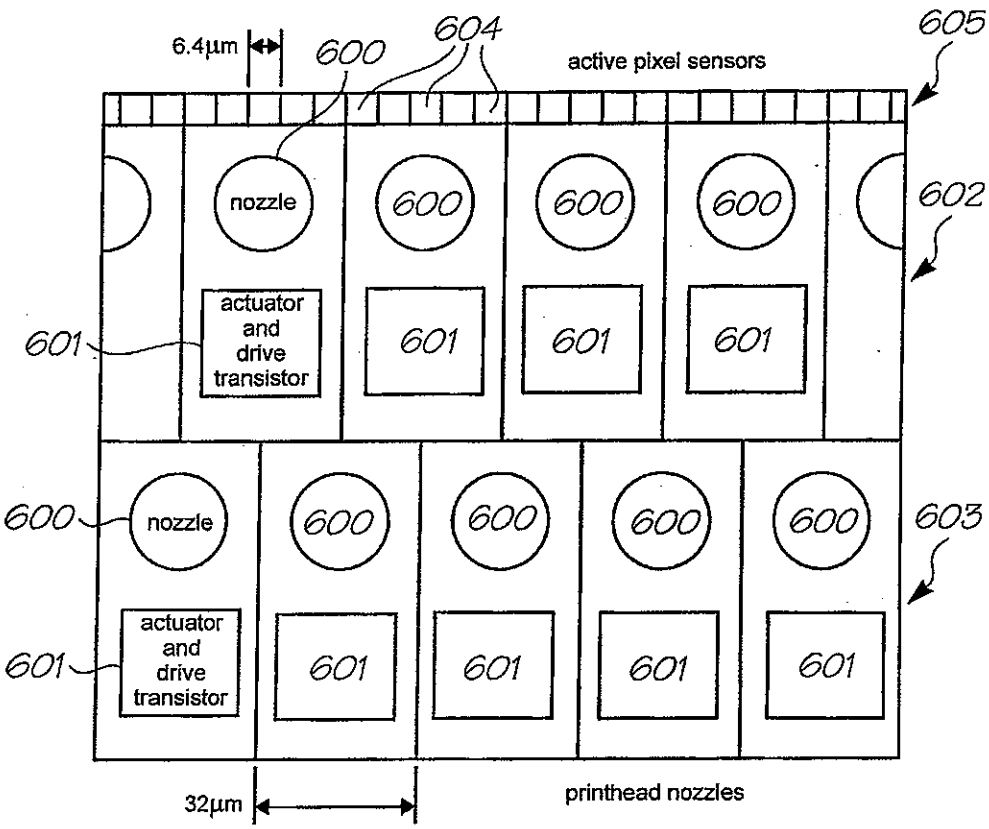

6.4µm
600
604
active pixel sensors
605
nozzle
602
actuator and drive transistor
601
603
32µm
printhead nozzles

FIG. 16

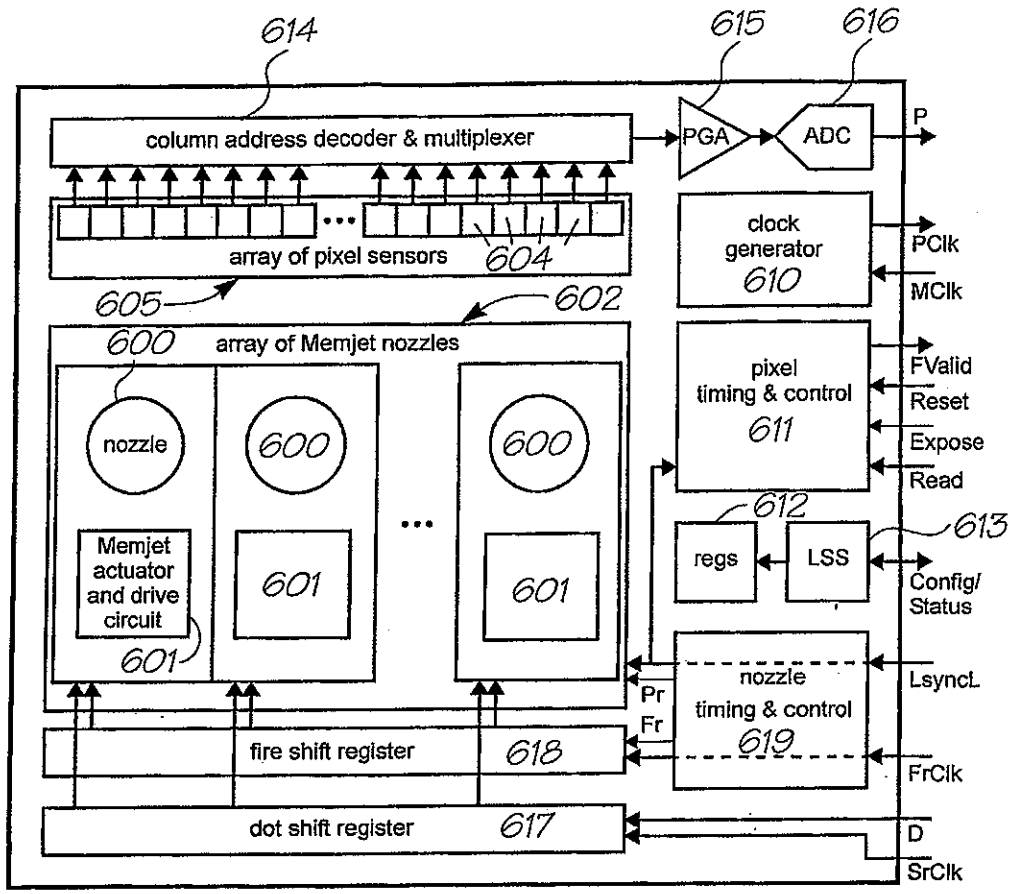

614
615
616
column address decoder & multiplexer
PGA
ADC
P
array of pixel sensors
604
clock generator
610
PClk
MClk
605
602
600
array of Memjet nozzles
nozzle
600
600
pixel timing & control
611
FValid
Reset
Expose
Read
612
613
regs
LSS
Config/ Status
Memjet actuator and drive circuit
601
601
601
nozzle timing & control
619
LsyncL
Pr
Fr
fire shift register
618
FrClk
dot shift register
617
D
SrClk

FIG. 17

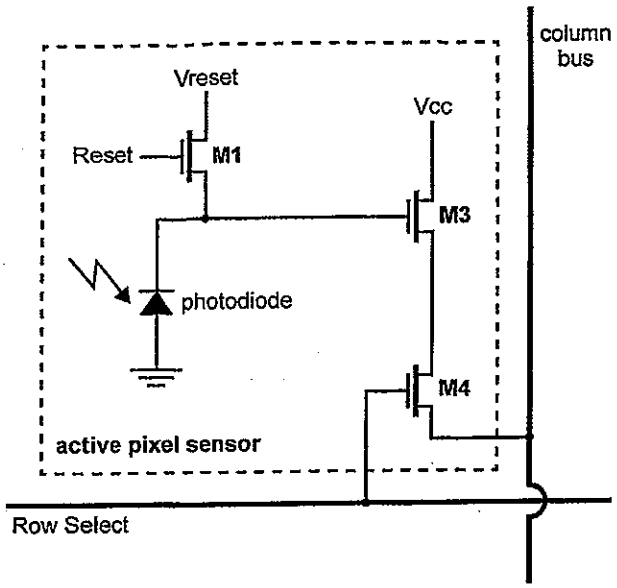

column bus
Vreset
Vcc
Reset
M1
M3
photodiode
M4
active pixel sensor
Row Select

FIG. 18

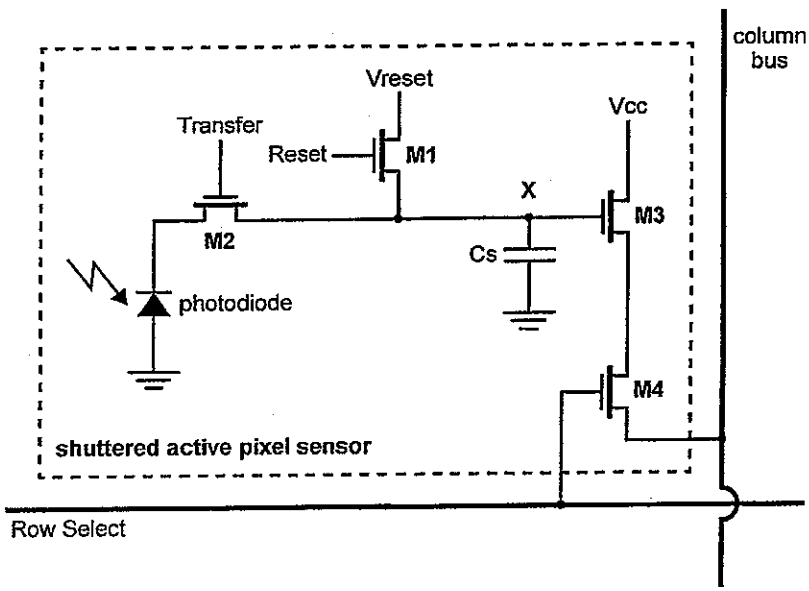

column bus
Vreset
Vcc
Transfer
Reset
M1
X
M3
M2
Cs
photodiode
M4
shuttered active pixel sensor
Row Select

FIG. 19

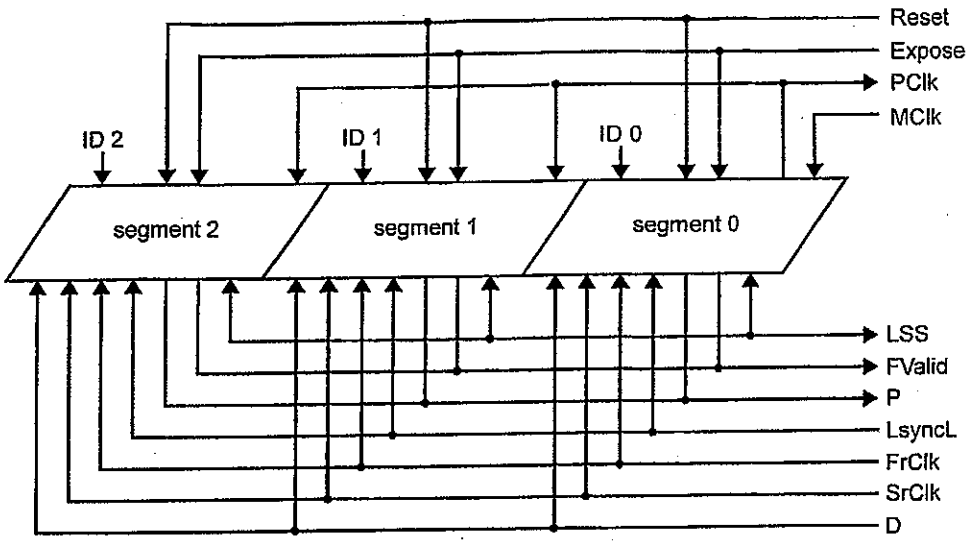

Reset
Expose
PClk
MClk
ID 2
ID 1
ID 0
segment 2
segment 1
segment 0
LSS
FValid
P
LsyncL
FrClk
SrClk
D

FIG. 20

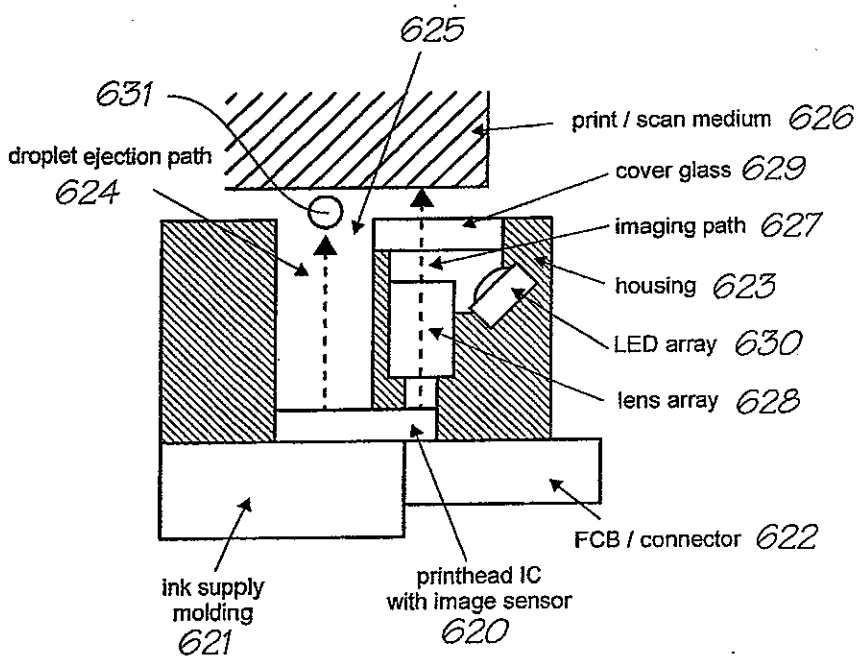

625
631
print / scan medium 626
droplet ejection path
624
cover glass 629
imaging path 627
housing 623
LED array 630
lens array 628
FCB / connector 622
ink supply
molding
621
printhead IC
with image sensor
620

FIG. 21

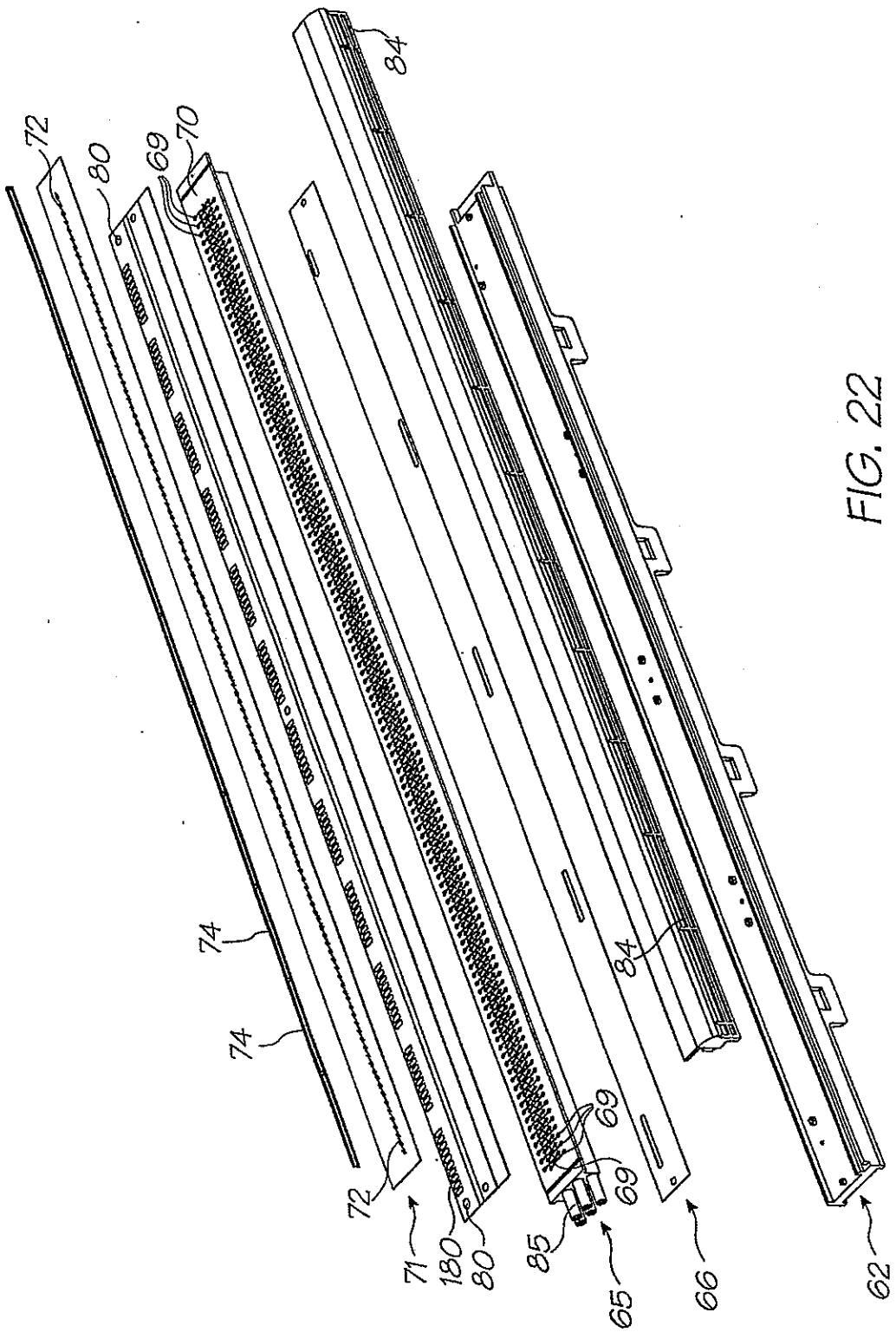


FIG. 22

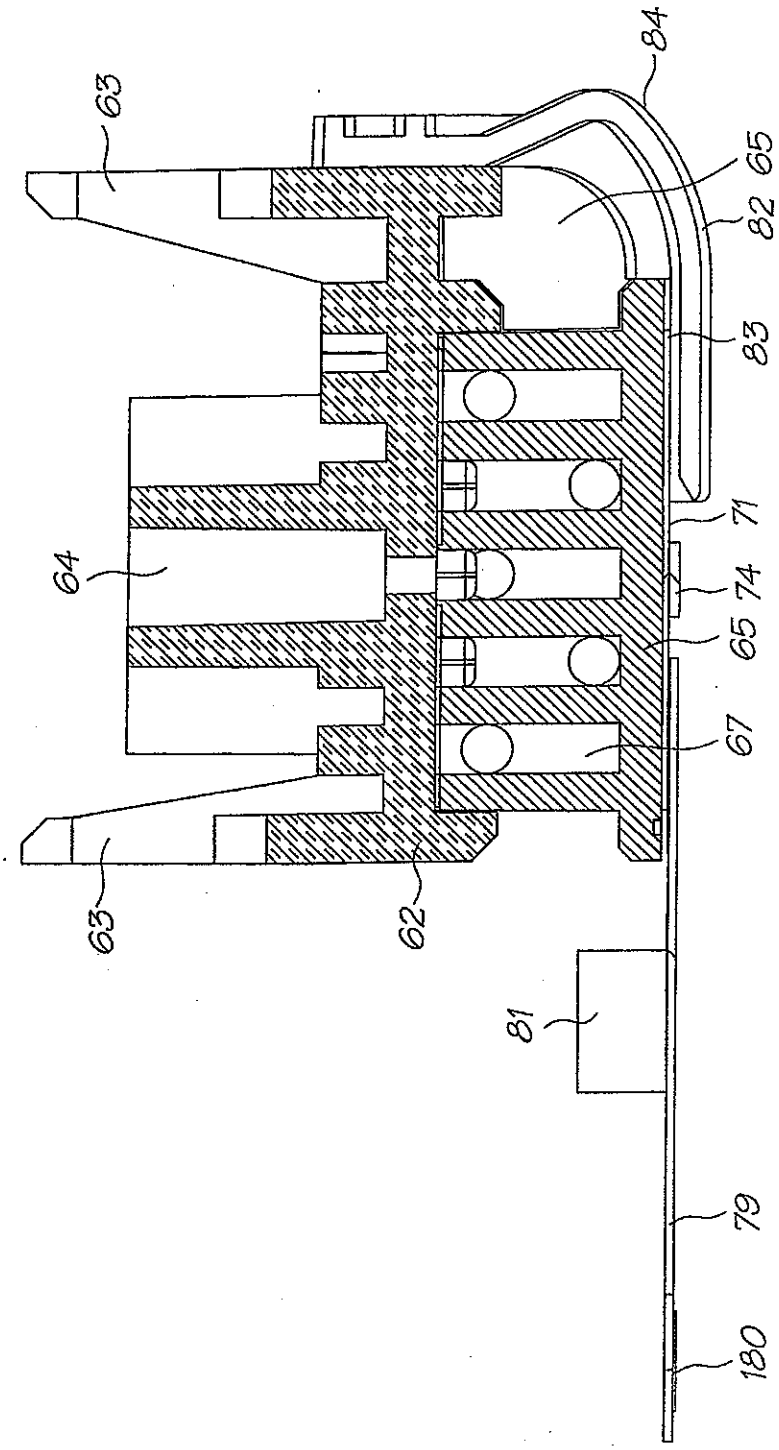


FIG. 23

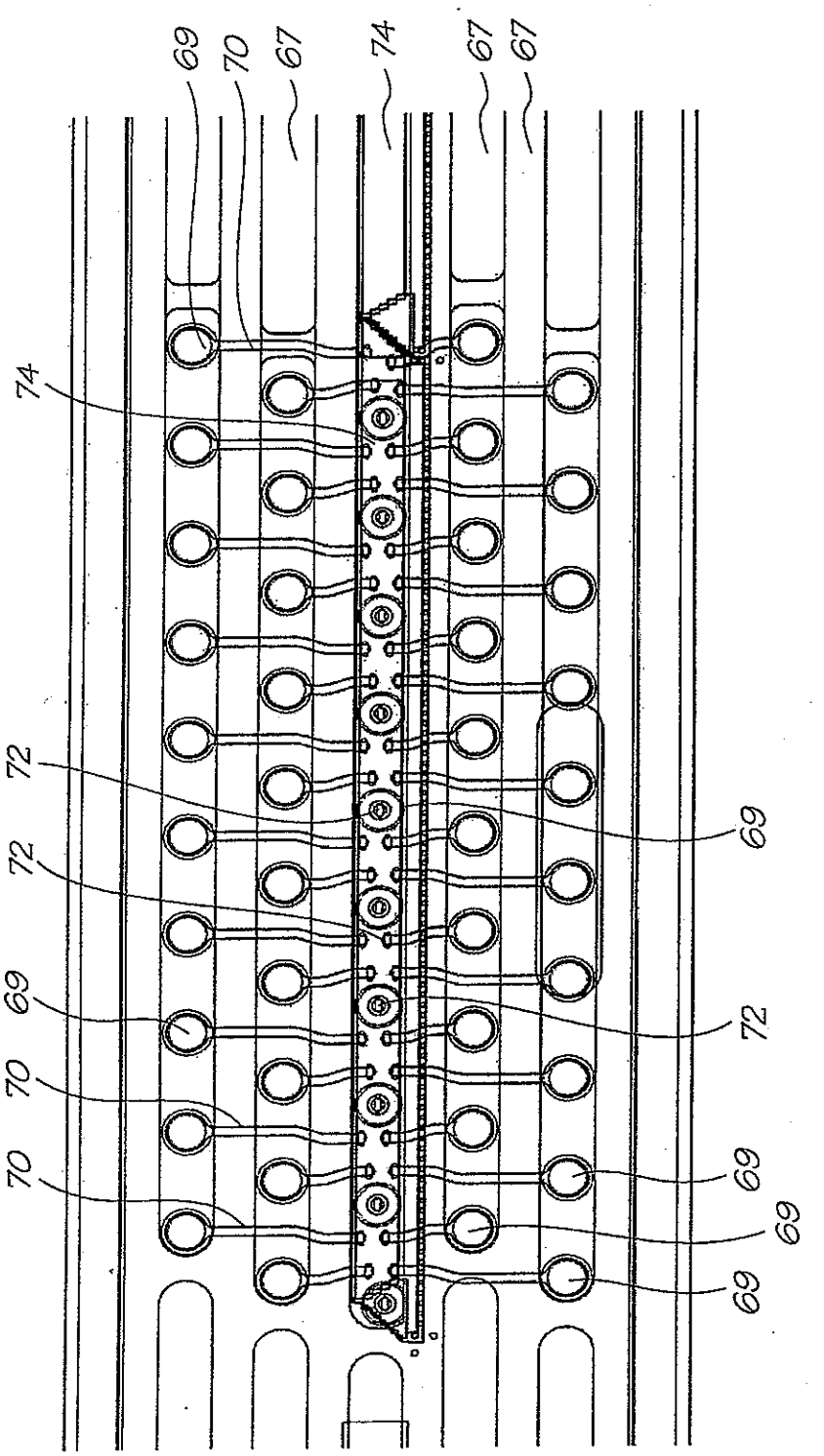


FIG. 24

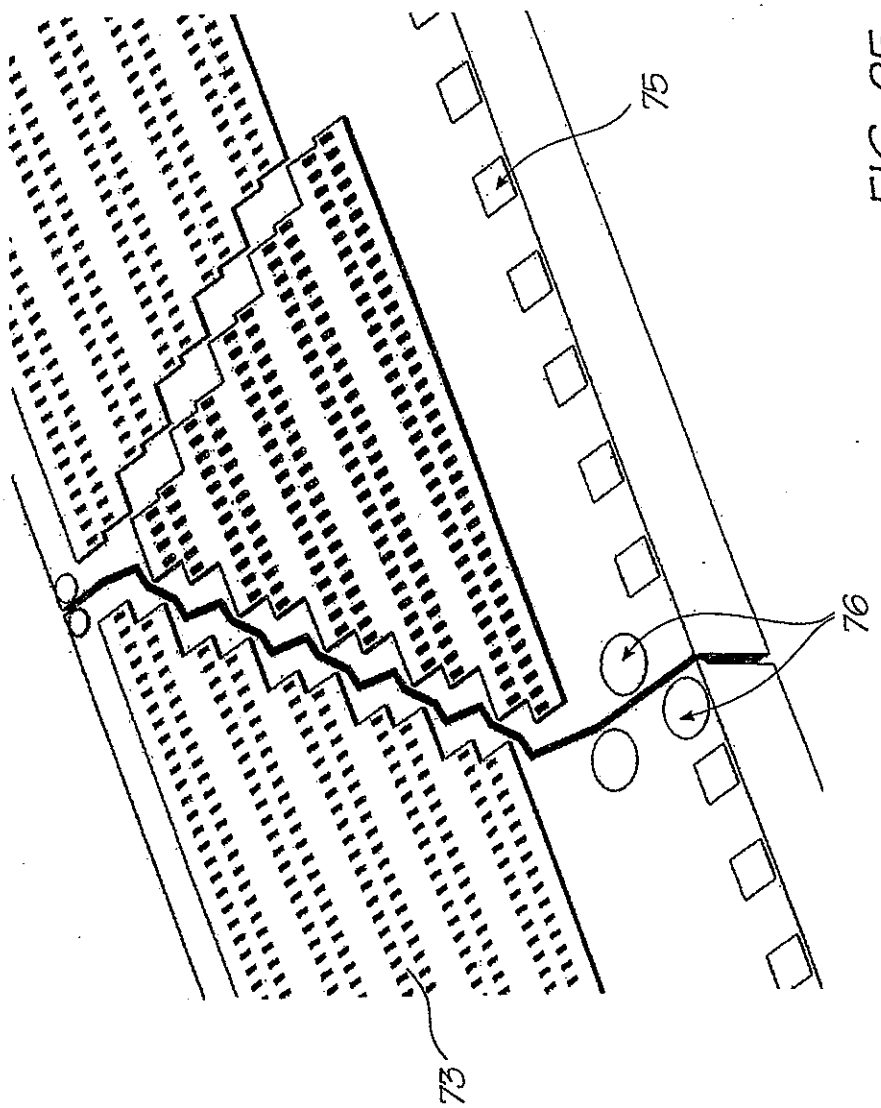


FIG. 25

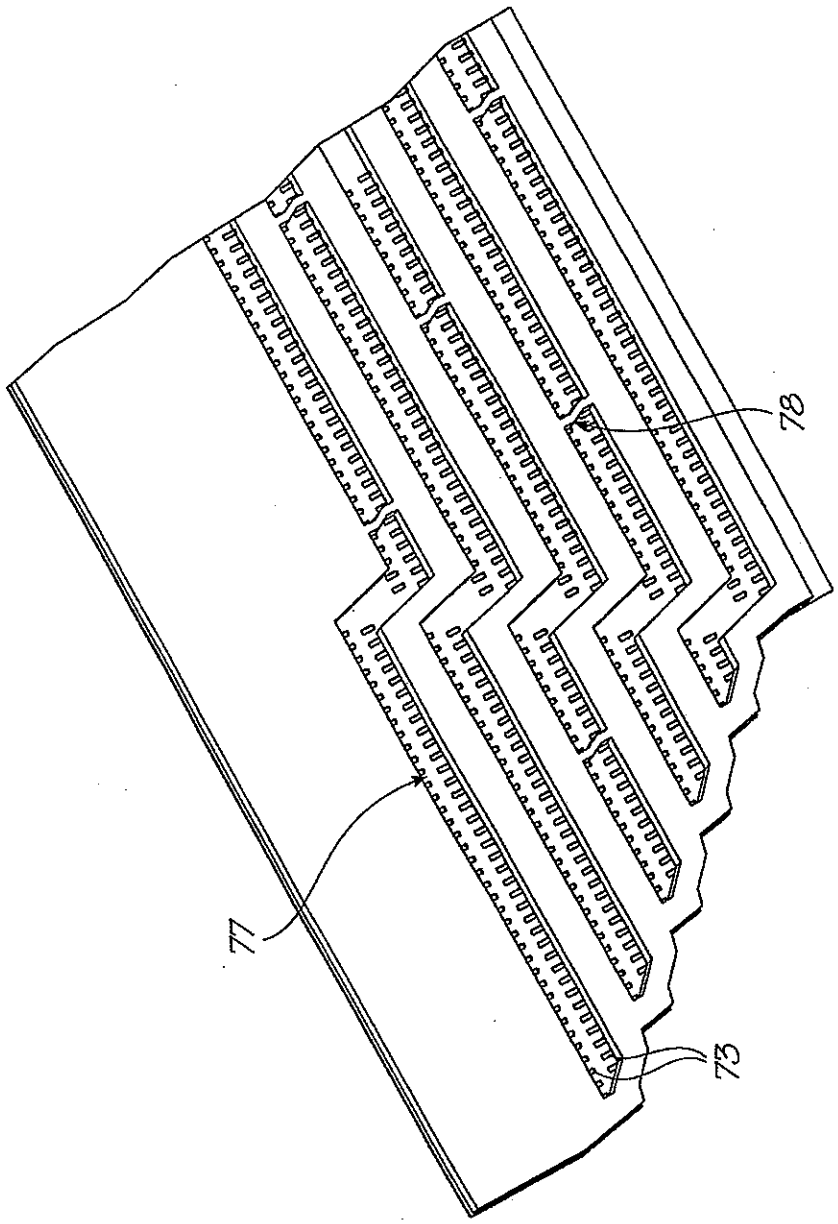


FIG. 26

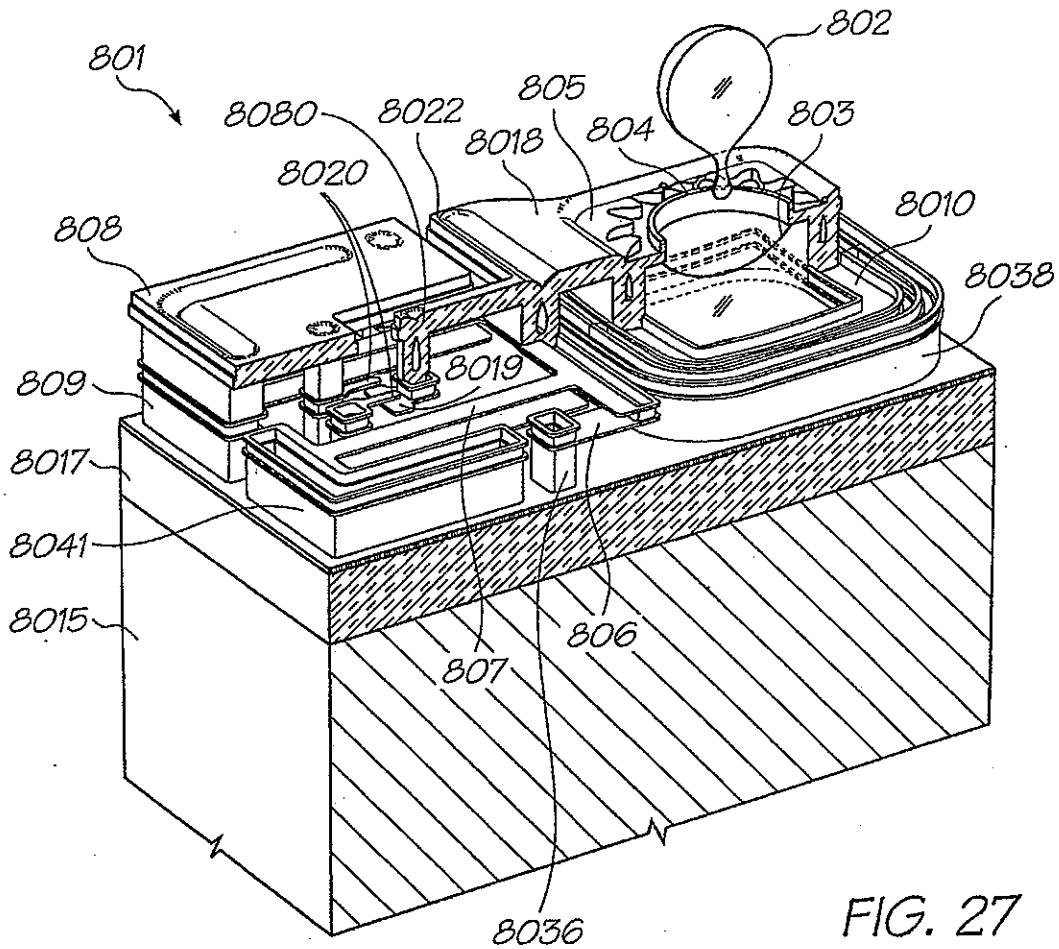

801
802
803
804
805
806
807
808
809
8010
8015
8017
8018
8019
8020
8022
8036
8038
8041
8080

FIG. 27

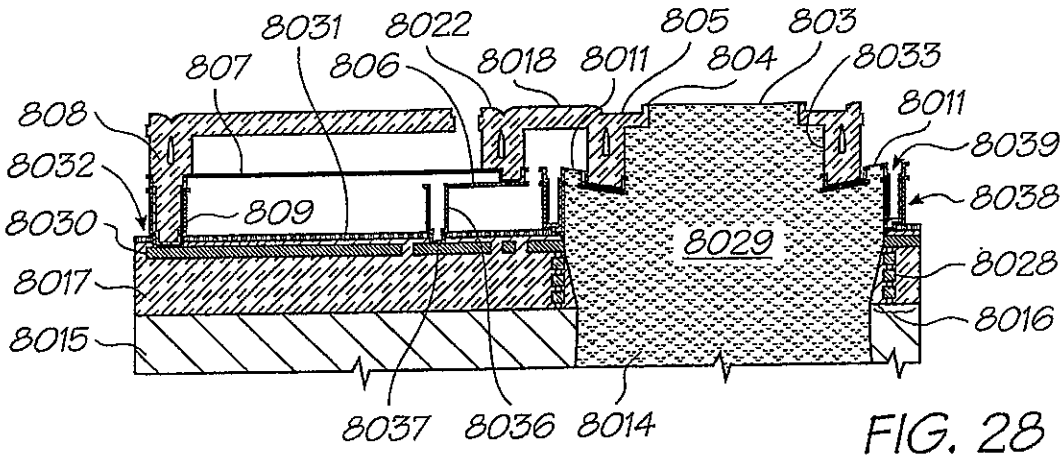


FIG. 28

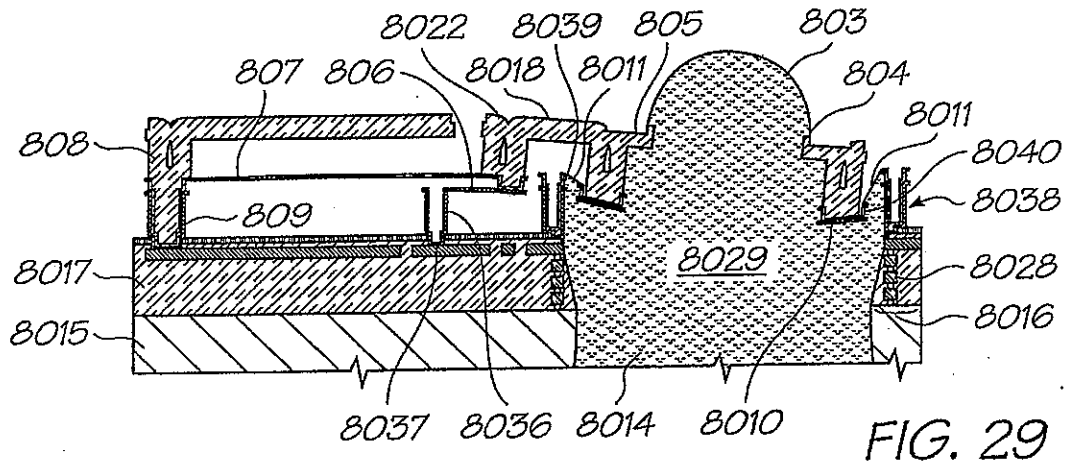


FIG. 29

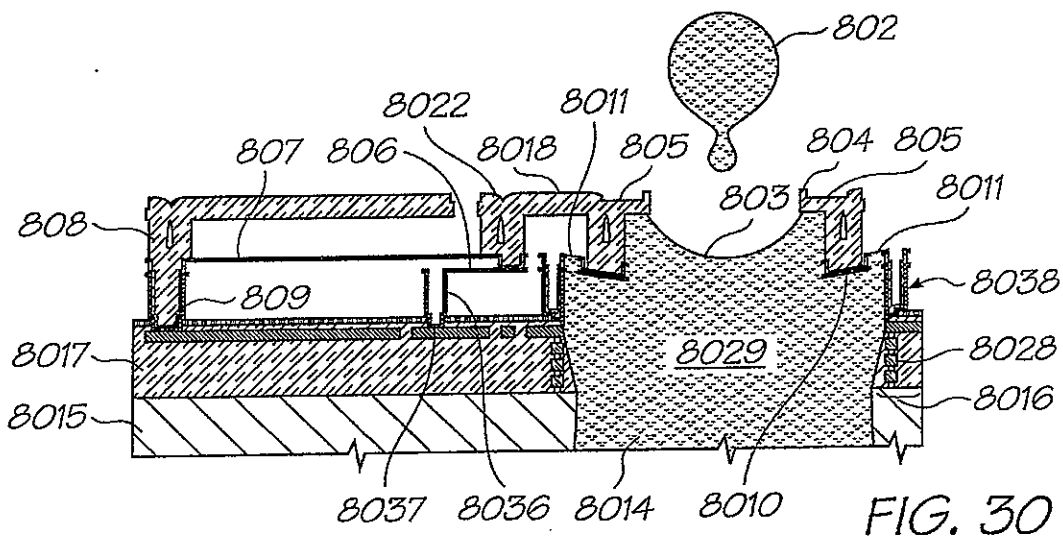


FIG. 30

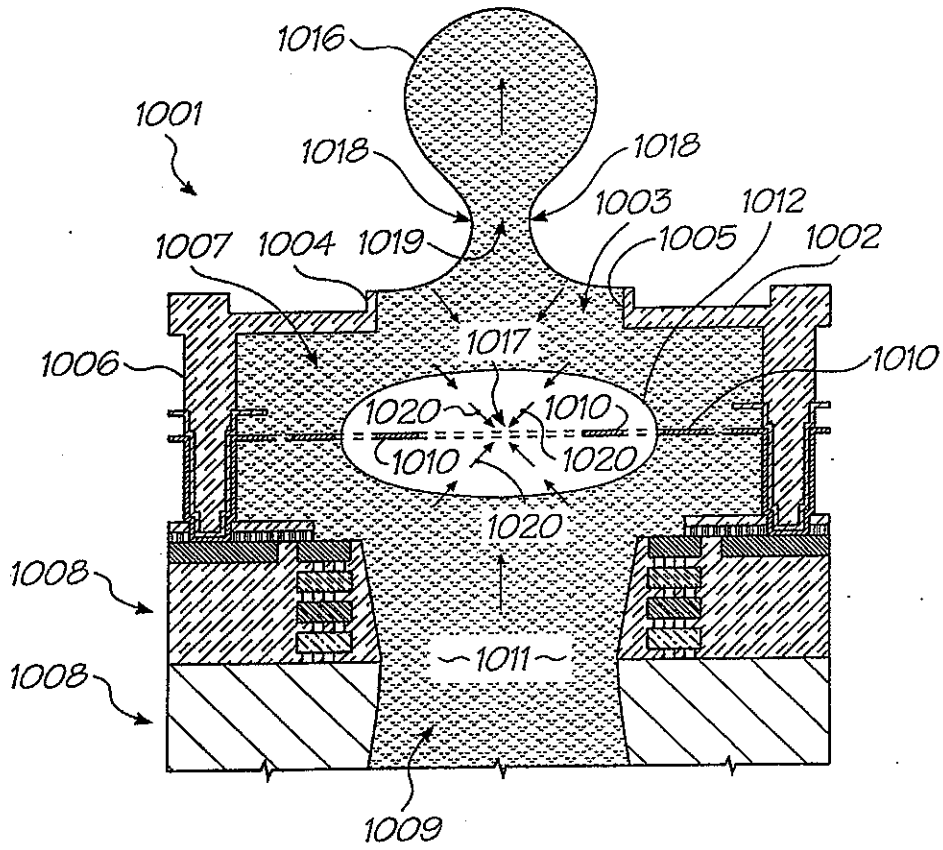

1016
1001
1018
1018
1003
1012
1007
1004
1019
1005
1002
1017
1006
1010
1020
1010
1010
1020
1020
1008
1011
1008
1009

FIG. 31

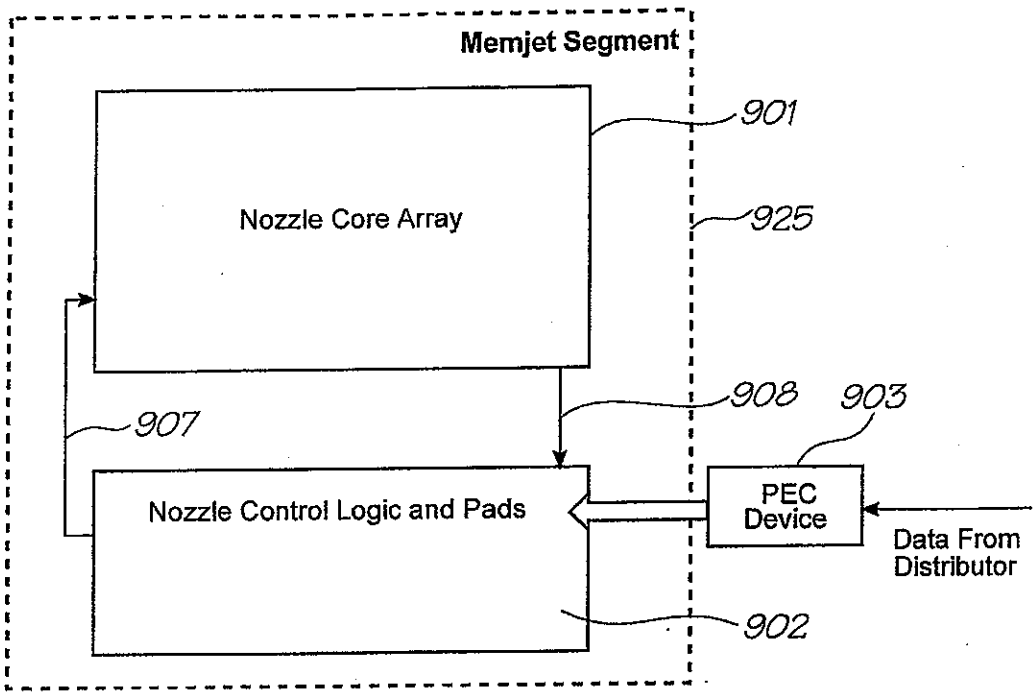

Memjet Segment
901
Nozzle Core Array
925
908
903
907
Nozzle Control Logic and Pads
PEC Device
Data From Distributor
902

FIG. 32

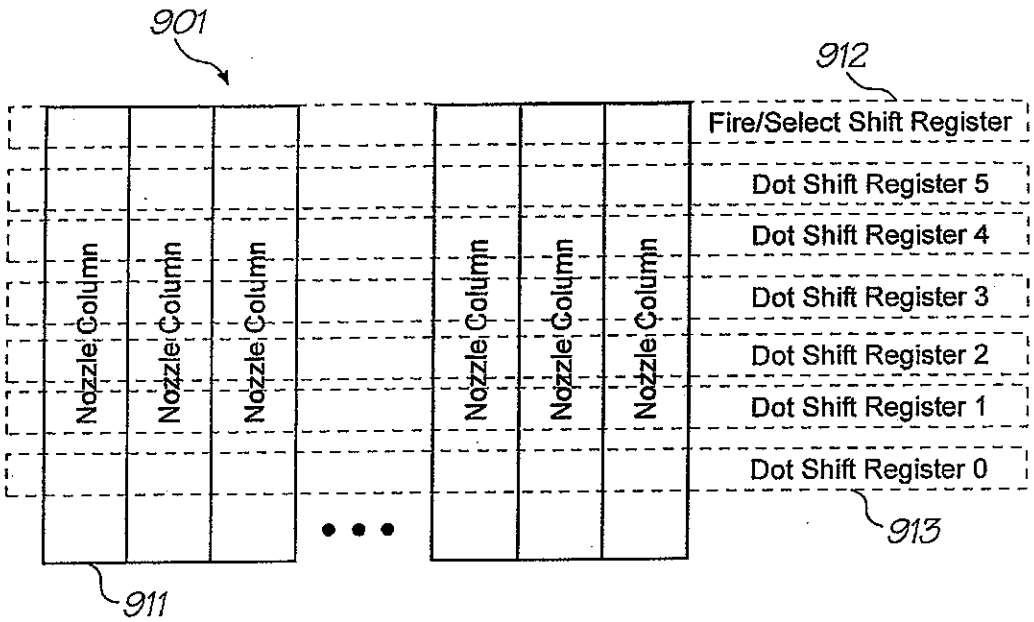

901
912
Fire/Select Shift Register
Dot Shift Register 5
Dot Shift Register 4
Dot Shift Register 3
Dot Shift Register 2
Dot Shift Register 1
Dot Shift Register 0
Nozzle Column
Nozzle Column
Nozzle Column
Nozzle Column
Nozzle Column
Nozzle Column
913
911

FIG. 33

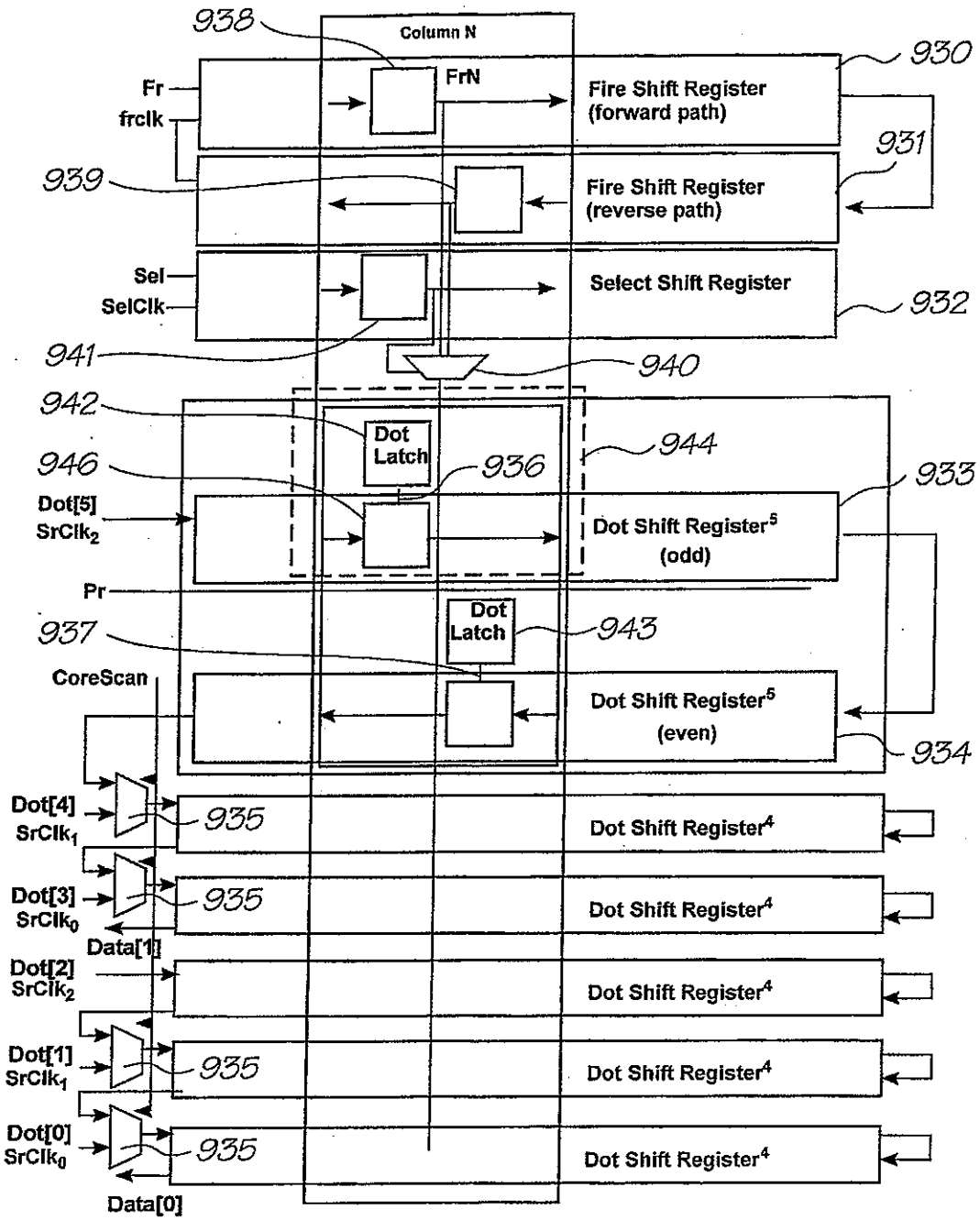

938
Column N
930
Fr
frclk
FrN
Fire Shift Register
(forward path)
931
939
Fire Shift Register
(reverse path)
Sel
SelClk
Select Shift Register
932
941
940
942
Dot
Latch
944
946
936
933
Dot[5]
SrClk2
Dot Shift Register5
(odd)
Pr
Dot
Latch
937
943
CoreScan
Dot Shift Register5
(even)
934
Dot[4]
SrClk1
935
Dot Shift Register4
Dot[3]
SrClk0
935
Dot Shift Register4
Data[1]
Dot[2]
SrClk2
Dot Shift Register4
Dot[1]
SrClk1
935
Dot Shift Register4
Dot[0]
SrClk0
935
Dot Shift Register4
Data[0]

FIG. 34

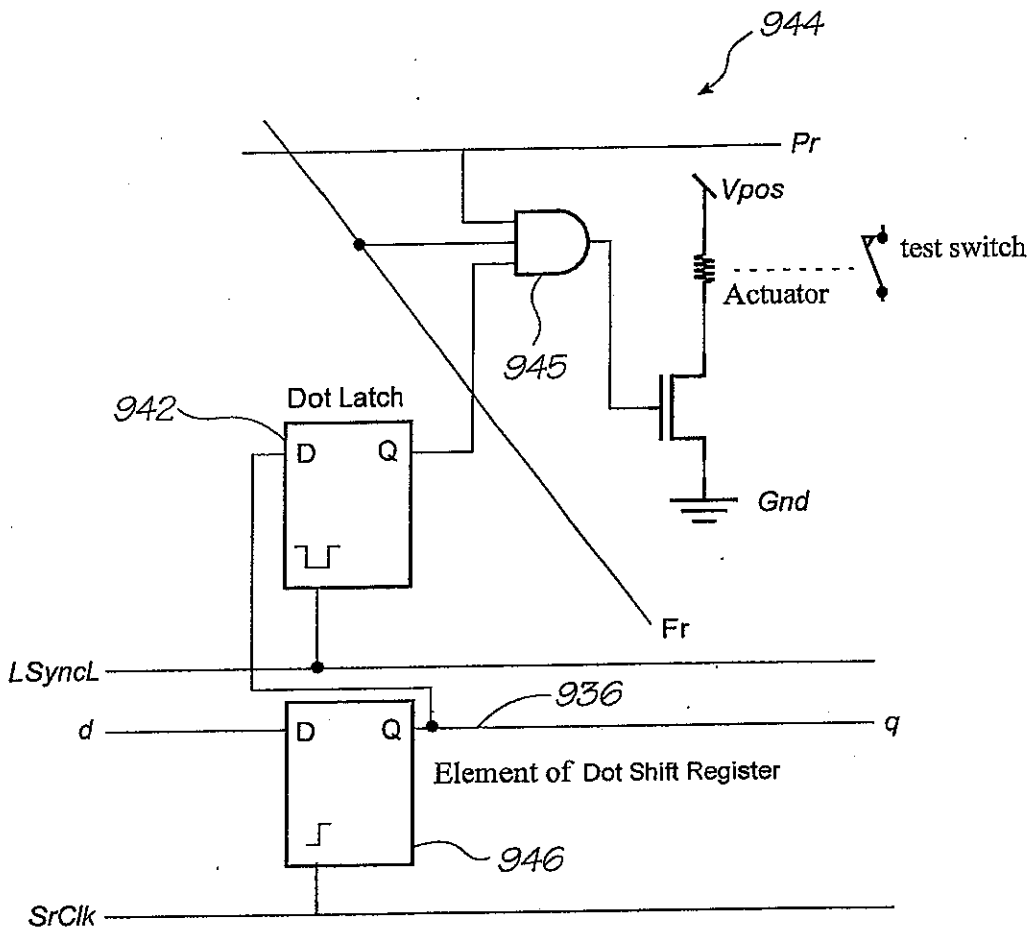

944
Pr
Vpos
test switch
Actuator
945
942
Dot Latch
D
Q
Gnd
Fr
LSyncL
936
d
D
Q
q
Element of Dot Shift Register
946
SrClk

FIG. 35

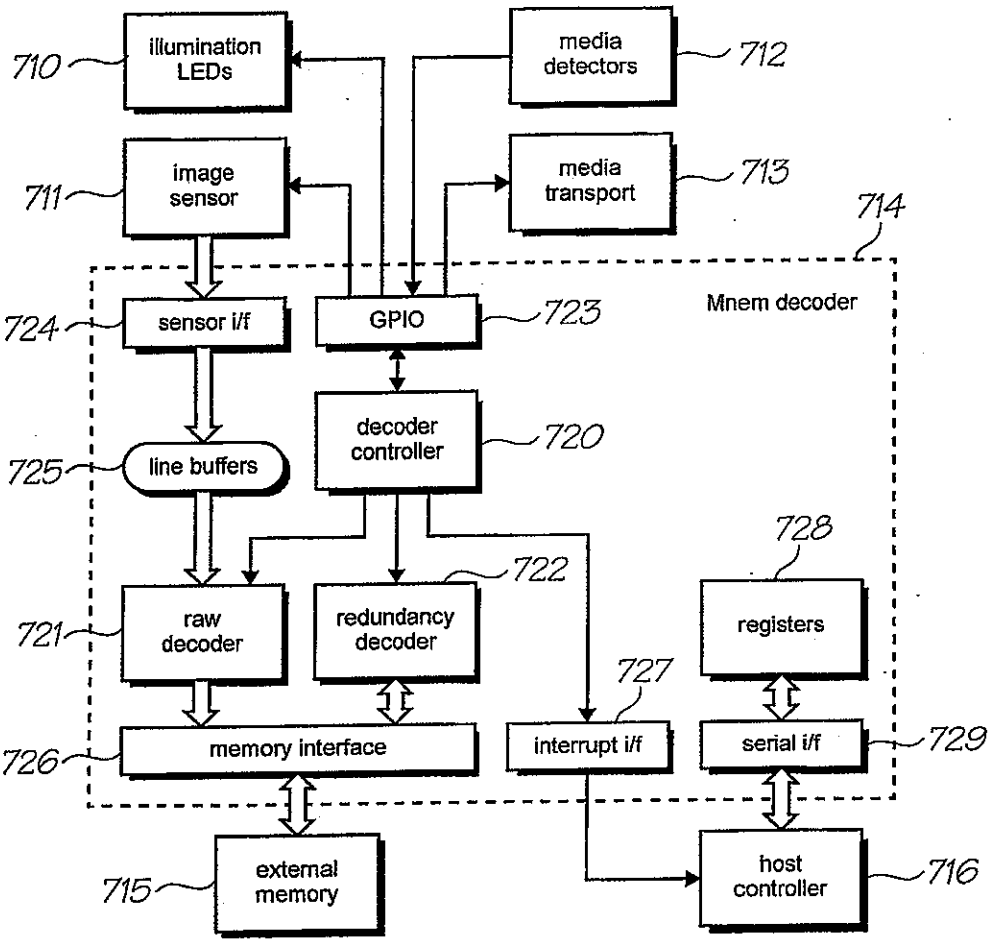

710
illumination LEDs
media detectors
712
711
image sensor
media transport
713
714
Mnem decoder
724
sensor i/f
GPIO
723
decoder controller
720
725
line buffers
728
722
raw decoder
redundancy decoder
registers
721
727
memory interface
interrupt i/f
serial i/f
729
726
external memory
715
host controller
716

FIG. 36

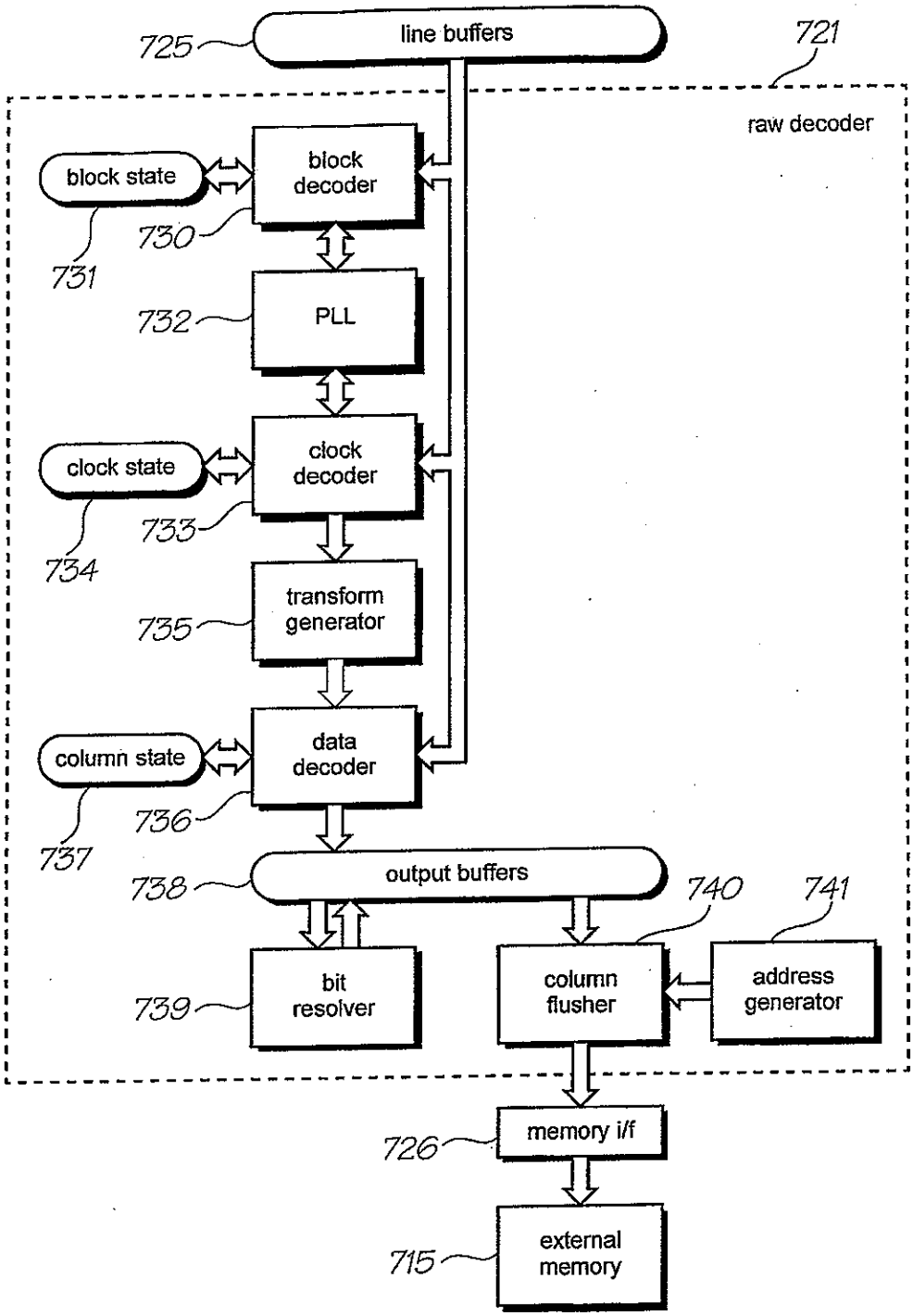

725
line buffers
721
raw decoder
block state
block decoder
730
731
732
PLL
clock state
clock decoder
733
734
transform generator
735
column state
data decoder
736
737
738
output buffers
740
741
bit resolver
739
column flusher
address generator
726
memory i/f
715
external memory

FIG. 37

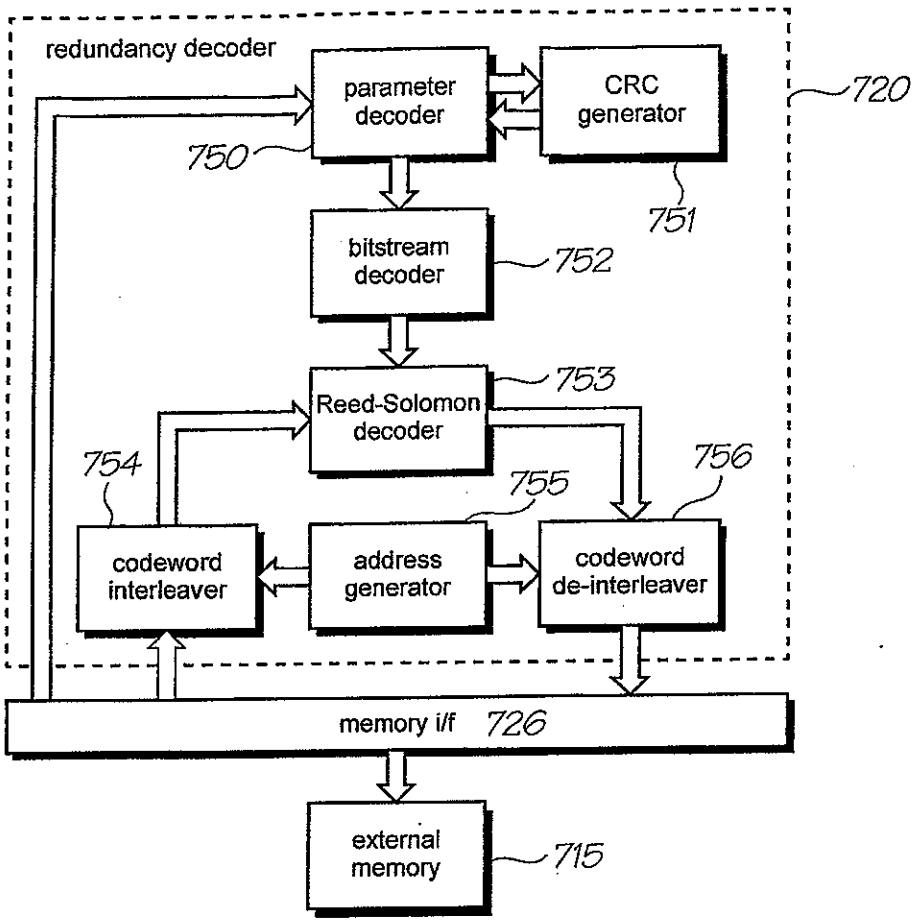

redundancy decoder
parameter decoder
CRC generator
720
750
751
bitstream decoder
752
Reed-Solomon decoder
753
754
755
756
codeword interleaver
address generator
codeword de-interleaver
memory i/f 726
external memory
715

FIG. 38

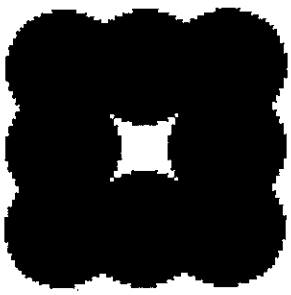


FIG. 39

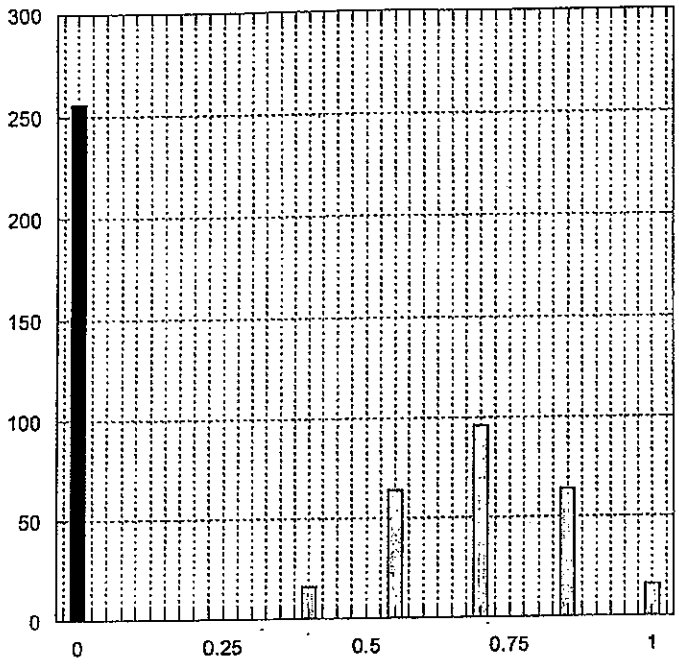


FIG. 40

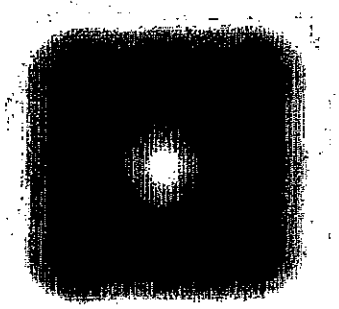


FIG. 41

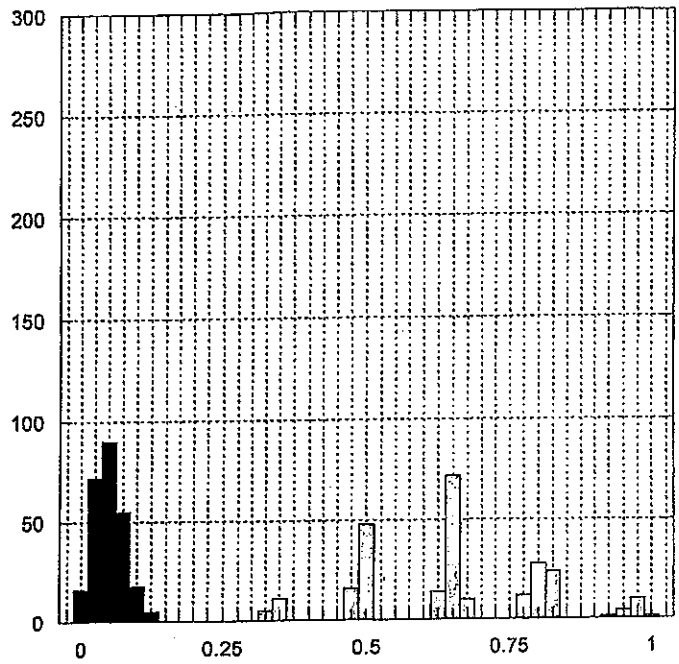


FIG. 42

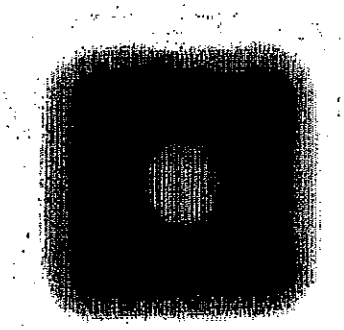


FIG. 43

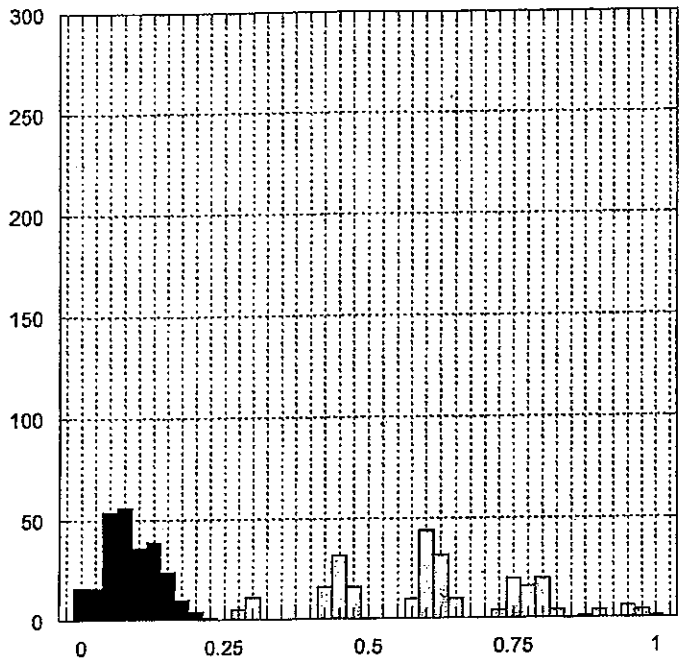


FIG. 44