CLAIMS

What is claimed is:

1. A microelectronic device, comprising:

a microelectronic substrate having an active surface and an opposing back surface;

a plurality of microelectronic integrated circuit components formed proximate the microelectronic substrate active surface;

a plurality of through-substrate vias extending through the microelectronic substrate from the microelectronic substrate active surface to a back surface of the microelectronic substrate;

a plurality of conductive routes between the plurality of first microelectronic integrated circuit component and the first through-substrate via;

at least one interconnection conductive trace on the microelectronic device back surface contacting at least one of the plurality of through-substrate vias and another of the plurality of through-substrate vias.

2. The microelectronic device of claim 1, wherein the plurality of through-substrate vias comprises a plurality of openings extending through the microelectronic substrate and a conductive material disposed within the plurality of openings.

3. The microelectronic device of claim 1, further including a dielectric layer proximate the microelectronic substrate active surface.

4. The microelectronic device of claim 3, wherein the plurality of conductive routes between the plurality of microelectronic integrated circuit components and the plurality of through-substrate via comprises:

a plurality of first conductive vias extending from the plurality of microelectronic integrated circuit components through the dielectric layer to an upper surface of the dielectric layer;

a plurality of second conductive vias extending through the dielectric layer from the dielectric layer upper surface to the first through-substrate via;

a plurality of conductive traces on the dielectric layer upper surface connecting the plurality of first conductive vias to a corresponding plurality of the second conductive vias.

5. A microelectronic device, comprising:

a microelectronic substrate having an active surface and an opposing back surface;

a first microelectronic integrated circuit component formed proximate the microelectronic substrate active surface;

a first through-substrate via extending through the microelectronic substrate from the microelectronic substrate active surface to a back surface of the microelectronic substrate;

a first conductive route between the first microelectronic integrated circuit component and the first through-substrate via;

a second microelectronic integrated circuit component formed proximate the microelectronic substrate active surface;

a second through-substrate via extending through the microelectronic substrate from the microelectronic substrate active surface to a back surface of the microelectronic substrate;

a second conductive route between the second microelectronic integrated circuit component and the second through-substrate via; and

an interconnection conductive trace on the microelectronic device back surface contacting the first through-substrate via and the second through-substrate via.

6. The microelectronic device of claim 5, wherein the first through-substrate via comprises an opening extending through the microelectronic substrate and a conductive material disposed within the opening.

7. The microelectronic device of claim 5, wherein the second through-substrate via comprises an opening extending through the microelectronic substrate and a conductive material disposed within the opening.

8. The microelectronic device of claim 5, further including a dielectric layer proximate the microelectronic substrate active surface.

9. The microelectronic device of claim 8, wherein the first conductive route between the first microelectronic integrated circuit component and the first through-substrate via comprises:

a first conductive via extending from the first microelectronic integrated circuit component through the dielectric layer to an upper surface of the dielectric layer;

a second conductive via extending through the dielectric layer from the dielectric layer upper surface to the first through-substrate via;

a conductive trace on the dielectric layer upper surface connecting the first conductive via to the second conductive via.

10. The microelectronic device of claim 8, wherein the second conductive route between the second microelectronic integrated circuit component and the second through-substrate via comprises:

a first conductive via extending from the second microelectronic integrated circuit component through the dielectric layer to an upper surface of the dielectric layer;

a second conductive via extending through the dielectric layer from the dielectric layer upper surface to the second through-substrate via;

a conductive trace on the dielectric layer upper surface connecting the first conductive via to the second conductive via.

11. A method, comprising:

forming a plurality of microelectronic integrated circuit components proximate an active surface of a microelectronic substrate;

forming a plurality of through-substrate vias extending through the microelectronic substrate from the microelectronic substrate active surface to a back surface of the microelectronic substrate;

forming a plurality of conductive routes between the plurality of microelectronic integrated circuit components and the plurality of through-substrate vias; and

forming at least one interconnection conductive trace on the microelectronic device back surface between at least one of the plurality of through-substrate vias to at least another of the plurality of through-substrate vias.

12. The method of claim 11, further comprising routing a critical signal from one of the plurality of microelectronic integrated circuit components to another of the plurality of microelectronic integrated circuit components through the at least one interconnection conductive trace.

13. The method of claim 12, wherein routing a critical signal from one of the plurality of microelectronic integrated circuit components to another of the plurality of microelectronic integrated circuit components through the at least one interconnection conductive trace comprises routing a timing sensitive signal from one of the plurality of microelectronic integrated circuit components to another of the plurality of microelectronic integrated circuit components through the at least one interconnection conductive trace.

14. The method of claim 13, wherein routing a timing sensitive signal from one of the plurality of microelectronic integrated circuit components to another of the plurality of

microelectronic integrated circuit components through the at least one interconnection conductive trace comprises routing a clock signal from one of the plurality of microelectronic integrated circuit components to another of the plurality of microelectronic integrated circuit components through the at least one interconnection conductive trace.

15. The method of claim 11, wherein forming a plurality of through-substrate vias comprises:

forming a plurality of openings extending through the microelectronic substrate from the microelectronic substrate active surface to the microelectronic substrate back surface; and

disposing a conductive material within the plurality of openings.

16. The method of claim 11, wherein forming a plurality of conductive routes comprises:

forming a dielectric layer on the microelectronic substrate active surface;

forming a plurality of first conductive vias from the plurality of microelectronic integrated circuit components through the dielectric layer to an upper surface of the dielectric layer;

forming a plurality of second conductive vias through the dielectric layer from the dielectric layer upper surface to the plurality of through-substrate vias;

forming a plurality of conductive traces on the dielectric layer upper surface to connect at least one of the plurality of first conductive vias to at least one of the plurality of second conductive vias.

17. A system, comprising:

a system substrate; and

a microelectronic device attached to the system substrate;

wherein the microelectronic device, comprises:

a microelectronic substrate having an active surface and an opposing back surface;

a plurality of microelectronic integrated circuit components formed proximate the microelectronic substrate active surface;

a plurality of through-substrate vias extending through the microelectronic substrate from the microelectronic substrate active surface to a back surface of the microelectronic substrate;

a plurality of conductive routes between the plurality of first microelectronic integrated circuit component and the first through-substrate via;

at least one interconnection conductive trace on the microelectronic device back surface contacting at least one of the plurality of through-substrate vias and another of the plurality of through-substrate vias.

18. The system of claim 17, wherein the plurality of through-substrate vias comprises a plurality of openings extending through the microelectronic substrate and a conductive material disposed within the plurality of openings.

19. The system of claim 17, further including a dielectric layer proximate the microelectronic substrate active surface.

20. The system of claim 19, wherein the plurality of conductive routes between the plurality of microelectronic integrated circuit components and the plurality of through-substrate via comprises:

a plurality of first conductive vias extending from the plurality of microelectronic integrated circuit components through the dielectric layer to an upper surface of the dielectric layer;

a plurality of second conductive vias extending through the dielectric layer from the dielectric layer upper surface to the first through-substrate via;

a plurality of conductive traces on the dielectric layer upper surface connecting the plurality of first conductive vias to a corresponding plurality of the second conductive vias.

CLAIMS

What is claimed is:

1. A microelectronic device, comprising:

a microelectronic substrate having an active surface and an opposing back surface;

a plurality of microelectronic integrated circuit components formed proximate the microelectronic substrate active surface;

a plurality of through-substrate vias extending through the microelectronic substrate from the microelectronic substrate active surface to a back surface of the microelectronic substrate;

a plurality of conductive routes between the plurality of first microelectronic integrated circuit component and the first through-substrate via;

at least one interconnection conductive trace on the microelectronic device back surface contacting at least one of the plurality of through-substrate vias and another of the plurality of through-substrate vias; and

a dielectric layer proximate the microelectronic substrate active surface,

wherein the plurality of conductive routes between the plurality of microelectronic integrated circuit components and the plurality of through-substrate via comprises:

a plurality of first conductive vias extending from the plurality of microelectronic integrated circuit components through the dielectric layer to an upper surface of the dielectric layer;

a plurality of second conductive vias extending through the dielectric layer from the dielectric layer upper surface to the first through-substrate via;

a plurality of conductive traces on the dielectric layer upper surface connecting the plurality of first conductive vias to a corresponding plurality of the second conductive vias.

2. A microelectronic device, comprising:

a microelectronic substrate having an active surface and an opposing back surface;

a first microelectronic integrated circuit component formed proximate the microelectronic substrate active surface;

a first through-substrate via extending through the microelectronic substrate from the microelectronic substrate active surface to a back surface of the microelectronic substrate;

a first conductive route between the first microelectronic integrated circuit component and the first through-substrate via;

a second microelectronic integrated circuit component formed proximate the microelectronic substrate active surface;

a second through-substrate via extending through the microelectronic substrate from the microelectronic substrate active surface to a back surface of the microelectronic substrate;

a second conductive route between the second microelectronic

integrated circuit component and the second through-substrate via;

an interconnection conductive trace on the microelectronic device back surface contacting the first through-substrate via and the second through-substrate via; and

a dielectric layer proximate the microelectronic substrate active surface,

wherein the first conductive route between the first microelectronic integrated circuit component and the first through-substrate via comprises:

a first conductive via extending from the first microelectronic integrated circuit component through the dielectric layer to an upper surface of the dielectric layer;

a second conductive via extending through the dielectric layer from the dielectric layer upper surface to the first through-substrate via;

a conductive trace on the dielectric layer upper surface connecting the first conductive via to the second conductive via.

3. A microelectronic device, comprising:

a microelectronic substrate having an active surface and an opposing back surface;

a first microelectronic integrated circuit component formed proximate the microelectronic substrate active surface;

a first through-substrate via extending through the microelectronic substrate from the microelectronic substrate active surface to a back surface of the microelectronic substrate;

a first conductive route between the first microelectronic integrated circuit component and the first through-substrate via;

a second microelectronic integrated circuit component formed proximate the microelectronic substrate active surface;

a second through-substrate via extending through the microelectronic substrate from the microelectronic substrate active surface to a back surface

of the microelectronic substrate;

a second conductive route between the second microelectronic integrated circuit component and the second through-substrate via;

an interconnection conductive trace on the microelectronic device back surface contacting the first through-substrate via and the second through-substrate via; and

a dielectric layer proximate the microelectronic substrate active surface,

wherein the second conductive route between the second microelectronic integrated circuit component and the second through-substrate via comprises:

a first conductive via extending from the second microelectronic integrated circuit component through the dielectric layer to an upper surface of the dielectric layer;

a second conductive via extending through the dielectric layer from the dielectric layer upper surface to the second through-substrate via;

a conductive trace on the dielectric layer upper surface connecting the first conductive via to the second conductive via.

4. A method for fabricating a microelectronic device, comprising:

forming a plurality of microelectronic integrated circuit components proximate an active surface of a microelectronic substrate;

forming a plurality of through-substrate vias extending through the microelectronic substrate from the microelectronic substrate active surface to a back surface of the microelectronic substrate;

forming a plurality of conductive routes between the plurality of microelectronic integrated circuit components and the plurality of through-substrate vias;

forming at least one interconnection conductive trace on the microelectronic device back surface between at least one of the plurality of through-substrate vias to at least another of the plurality of through-substrate vias; and

routing a critical signal from one of the plurality of microelectronic integrated

circuit components to another of the plurality of microelectronic integrated circuit components through the at least one interconnection conductive trace.

5. The method of claim 4, wherein routing a critical signal from one of the plurality of microelectronic integrated circuit components to another of the plurality of microelectronic integrated circuit components through the at least one interconnection conductive trace comprises routing a timing sensitive signal from one of the plurality of microelectronic integrated circuit components to another of the plurality of microelectronic integrated circuit components through the at least one interconnection conductive trace.

6. The method of claim 5, wherein routing a timing sensitive signal from one of the plurality of microelectronic integrated circuit components to another of the plurality of microelectronic integrated circuit components through the at least one interconnection conductive trace comprises routing a clock signal from one of the plurality of microelectronic integrated circuit components to another of the plurality of microelectronic integrated circuit components through the at least one interconnection conductive trace.

7. A method for fabricating a microelectronic device, comprising:

forming a plurality of microelectronic integrated circuit components proximate an active surface of a microelectronic substrate;

forming a plurality of through-substrate vias extending through the microelectronic substrate from the microelectronic substrate active surface to a back surface of the microelectronic substrate;

forming a plurality of conductive routes between the plurality of microelectronic integrated circuit components and the plurality of through-substrate vias;

forming at least one interconnection conductive trace on the microelectronic device back surface between at least one of the plurality of through-substrate vias to at least another of the plurality of through-substrate vias;

wherein forming a plurality of conductive routes comprises:

forming a dielectric layer on the microelectronic substrate active surface;

forming a plurality of first conductive vias from the plurality of microelectronic integrated circuit components through the dielectric layer to an upper surface of the dielectric layer;

forming a plurality of second conductive vias through the dielectric layer from the dielectric layer upper surface to the plurality of through-substrate vias;

forming a plurality of conductive traces on the dielectric layer upper surface to connect at least one of the plurality of first conductive vias to at least one of the plurality of second conductive vias.

8.A system for a microelectronic device, comprising:

a system substrate; and

a microelectronic device attached to the system substrate;

wherein the microelectronic device, comprises:

a microelectronic substrate having an active surface and an opposing back surface;

a plurality of microelectronic integrated circuit components formed proximate the microelectronic substrate active surface;

a plurality of through-substrate vias extending through the microelectronic substrate from the microelectronic substrate active surface to a back surface of the microelectronic substrate;

a plurality of conductive routes between the plurality of first microelectronic integrated circuit component and the first through-substrate via;

at least one interconnection conductive trace on the microelectronic device

back surface contacting at least one of the plurality of through-substrate vias and another of the plurality of through-substrate vias; and

a dielectric layer proximate the microelectronic substrate active surface,

wherein the plurality of conductive routes between the plurality of microelectronic integrated circuit components and the plurality of through-substrate via comprises:

a plurality of first conductive vias extending from the plurality of microelectronic integrated circuit components through the dielectric layer to an upper surface of the dielectric layer;

a plurality of second conductive vias extending through the dielectric layer from the dielectric layer upper surface to the first through-substrate via;

a plurality of conductive traces on the dielectric layer upper surface connecting the plurality of first conductive vias to a corresponding plurality of the second conductive vias.