the present disclosure. The following detailed description is, therefore, not to be taken in a limiting sense.

[0014] It is postulated that negative ions exist between gate stacks of memory cells and isolating dielectric due to contamination during the formation of the dielectric, e.g., silicon dioxide (SiO_2). These ions may be mobile, and may be absorbed onto or near the body of the memory cells, e.g., a semiconductor pillar in some memory cell structures, as a stable state after erasure or after long periods of data retention without access. Concentration of these superfluous ions, e.g., near an interface between a gate dielectric of an adjacent memory cell and its body, can influence the effective threshold voltage of that memory cell, which can result in errors in sensing its intended data value. Various embodiments seek to mitigate this phenomena by establishing a negative body potential prior to sensing that memory cell, e.g., immediately prior to sensing that memory cell, on a periodic basis, or during access operations on other memory cells.

[0015] Figure 1 is a simplified block diagram of a first apparatus, in the form of a memory (e.g., memory device) 100, in communication with a second apparatus, in the form of a processor 130, as part of a third apparatus, in the form of an electronic system, according to an embodiment. Some examples of electronic systems include personal computers, personal digital assistants (PDAs), digital cameras, digital media players, digital recorders, games, appliances, vehicles, wireless devices, mobile telephones, removable memory modules and the like. The processor 130, e.g., a controller external to the memory device 100, may represent a memory controller or other external host device.

[0016] Memory device 100 includes an array of memory cells 104 logically arranged in rows and columns. Memory cells of a logical row are typically connected to the same access line (commonly referred to as a word line) while memory cells of a logical column are typically selectively connected to the same data line (commonly referred to as a bit line). A single access line may be associated with more than one logical row of memory cells and a single data line may be associated with more than one logical column. Memory cells (not shown in Figure 1) of at least a portion of array of memory cells 104 are arranged in strings of series-connected memory cells.

embodiment, cache register 118 may be omitted, and the data are written directly into data register 120. Data are also output over input/output (I/O) pins [7:0] for an 8-bit device or input/output (I/O) pins [15:0] for a 16-bit device.

[0024] It will be appreciated by those skilled in the art that additional circuitry and signals can be provided, and that the memory device 100 of Figure 1 has been simplified. It should be recognized that the functionality of the various block components described with reference to Figure 1 may not necessarily be segregated to distinct components or component portions of an integrated circuit device. For example, a single component or component portion of an integrated circuit device could be adapted to perform the functionality of more than one block component of Figure 1. Alternatively, one or more components or component portions of an integrated circuit device could be combined to perform the functionality of a single block component of Figure 1.

[0025] Additionally, while specific I/O pins are described in accordance with popular conventions for receipt and output of the various signals, it is noted that other combinations or numbers of I/O pins may be used in the various embodiments.

[0026] Figure 2A is a schematic of a portion of an array of memory cells 200A as could be used in a memory of the type described with reference to Figure 1, e.g., as a portion of array of memory cells 104. Memory array 200A includes access lines, such as word lines (WL) 202_0 to 202_N, and a data line, such as bit line (BL) 204. The word lines 202 may be connected to global access lines (e.g., global word lines), not shown in Figure 2A, in a many-to-one relationship. For some embodiments, memory array 200A may be formed over a semiconductor that, for example, may be conductively doped to have a conductivity type, such as a p-type conductivity, e.g., to form a p-well, or an n-type conductivity, e.g., to form an n-well.

[0027] Memory array 200A might be arranged in rows (each corresponding to a word line 202) and columns (each corresponding to a bit line 204). Each column may include a string of series-connected memory cells, such as one of NAND strings 206_0 to 206_M. Each NAND string 206 might be connected (e.g., selectively connected) to a common source 216 and might include memory cells 208_0 to 208_N. The memory cells 208 may represent non-volatile memory cells for storage of data. The memory cells 208 of each NAND string 206 might be connected in series between a select gate 210 (e.g., a field-effect transistor), such as one of the select gates 210_0 to 210_M (e.g., that may be source select transistors,

commonly referred to as select gate source), and a select gate 212 (e.g., a field-effect transistor), such as one of the select gates 212_0 to 212_M (e.g., that may be drain select transistors, commonly referred to as select gate drain). Select gates 210_0 to 210_M might be commonly connected to a select line 214, such as a source select line or SGS, and select gates 212_0 to 212_M might be commonly connected to a select line 215, such as a drain select line or SGD. Although depicted as traditional field-effect transistors, the select gates 210 and 212 may utilize a structure similar to (e.g., the same as) the memory cells 208. The select gates 210 and 212 might represent a plurality of select gates connected in series, with each select gate in series configured to receive a same or independent control signal.

[0028] A source of each select gate 210 might be connected to common source (SRC) 216. The drain of each select gate 210 might be connected to a memory cell 208_0 of the corresponding NAND string 206. For example, the drain of select gate 210_0 might be connected to memory cell 208_0 of the corresponding NAND string 206_0. Therefore, each select gate 210 might be configured to selectively connect a corresponding NAND string 206 to common source 216. A control gate of each select gate 210 might be connected to select line 214.

[0029] The drain of each select gate 212 might be connected to the bit line 204 for the corresponding NAND string 206. For example, the drain of select gate 212_0 might be connected to the bit line 204_0 for the corresponding NAND string 206_0. The source of each select gate 212 might be connected to a memory cell 208_N of the corresponding NAND string 206. For example, the source of select gate 212_0 might be connected to memory cell 208_N of the corresponding NAND string 206_0. Therefore, each select gate 212 might be configured to selectively connect a corresponding NAND string 206 to the common bit line 204. A control gate of each select gate 212 might be connected to select line 215.

[0030] The memory array in Figure 2A might be a three-dimensional memory array, e.g., where NAND strings 206 may extend substantially perpendicular to a plane containing the common source 216 and to a plane containing a plurality of bit lines 204 that may be substantially parallel to the plane containing the common source 216.

[0031] Typical construction of memory cells 208 includes a data-storage structure 234 (e.g., a floating gate, charge trap, etc.) that can determine a data state of the memory cell (e.g., through changes in threshold voltage), and a control gate 236, as shown in Figure 2A. The data-storage structure 234 may include both conductive and dielectric structures while the control gate 236 is generally formed of one or more conductive materials. In some cases,

NAND memory array 200B may incorporate vertical structures which may include semiconductor pillars where a portion of a pillar may act as a body (e.g., channel) region of the memory cells of NAND strings 206. The NAND strings 206 may be each selectively connected to a bit line 204_0-204_M by a select transistor 212 (e.g., that may be drain select transistors, commonly referred to as select gate drain) and to a common source 216 by a select transistor 210 (e.g., that may be source select transistors, commonly referred to as select gate source). Multiple NAND strings 206 might be selectively connected to the same bit line 204. Subsets of NAND strings 206 can be connected to their respective bit lines 204 by biasing the select lines 215_0-215_L to selectively activate particular select transistors 212 each between a NAND string 206 and a bit line 204. The select transistors 210 can be activated by biasing the select line 214. Each word line 202 may be connected to multiple rows of memory cells of the memory array 200B. Rows of memory cells that are commonly connected to each other by a particular word line 202 may collectively be referred to as tiers.

[0034] Figure 2C is a further schematic of a portion of an array of memory cells 200C as could be used in a memory of the type described with reference to Figures 1, e.g., as a portion of array of memory cells 104. Like numbered elements in Figure 2C correspond to the description as provided with respect to Figure 2A. Array of memory cells 200C may include NAND strings 206, word lines 202, bit lines 204, source select lines 214, drain select lines 215 and common source 216 as depicted in Figure 2A. The array of memory cells 200A may be a portion of the array of memory cells 200C, for example. Figure 2C depicts groupings of NAND strings 206 into blocks of memory cells 250, e.g., blocks of memory cells 250_0, 250_1, 250_2 and 250_3. Blocks of memory cells 250 may be groupings of memory cells 208 that may be erased together in a single erase operation, sometimes referred to as erase blocks.

[0035] Figures 3A-3B are cross-sectional views of strings of series-connected memory cells as could be used in a memory of the type described with reference to Figure 1. Three-dimensional memory arrays are typically fabricated by forming alternating layers of conductors and dielectrics, forming holes in these layers, forming additional materials on sidewalls of the holes to define gate stacks for memory cells and other gates, and subsequently filling the holes with a semiconductor material to define a pillar to act as bodies of the memory cells and select gates. To improve conductivity of pillars and an adjacent semiconductor material, e.g., upon which they are formed, a conductive (e.g., conductively-doped) portion is typically formed in the hole at an interface with the adjacent semiconductor

[0050] Figures 4C-4D depict the ions 464 in a possible transient state, e.g., after establishing a negative body potential for a memory cell formed at the intersection of the word line 202 and semiconductor pillar 340. Figures 4C-4D might represent a possible transient state for a situation where the data storage structure 234 of the memory cell stores a data value corresponding to a high threshold voltage range, e.g., the highest threshold voltage range representing a data value of a plurality of possible data values stored by the memory cell. In such a situation, the number of electrons stored in the data storage structure 234 may assist movement of the ions 464 away from the semiconductor pillar 340. In this manner, the adverse effect on the effective threshold voltage of the memory cell of the stable state depicted in Figures 4A-4B may be mitigated.

[0051] Figures 4E-4F depict the ions 464 in a different possible transient state, e.g., after establishing a negative body potential for a memory cell formed at the intersection of the word line 202 and semiconductor pillar 340. Figures 4E-4F might represent a possible transient state for a situation where the data storage structure 234 of the memory cell stores a data value corresponding to a lower threshold voltage range than the example of Figures 4C-4D. In such a situation, with fewer electrons stored in the data storage structure 234, movement of the ions 464 away from the semiconductor pillar 340 may be less. However, the adverse effect on the effective threshold voltage of the memory cell of the stable state depicted in Figures 4A-4B may still be mitigated, albeit possibly to a lesser extent than the situation depicted in Figures 4C-4D.

[0052] Figures 5A-5B are timing diagrams depicting methods of operating a memory in accordance with embodiments. Figures 5A-5B depict two examples of method of establishing a negative potential in a body of a memory cell of a structure of the type depicted in Figure 3A. Similar results might be obtained for a structure of the type depicted in Figure 3B by applying a similar (e.g., the same) voltage level to the select line 217 as are shown for application to the select lines 214 and 215 in Figures 5A-5B. It is noted that the methods depicted in Figures 5A-5B may establish a negative potential on the bodies of memory cells formed at the intersection of the word lines 202 and a plurality of pillars 340, which might include all pillars 340 connected to the source 216.

[0053] In Figure 5A, the word lines 202 and the select lines 214 and 215 might maintain an initial voltage level. For example, the initial voltage level of the word lines 202 and the select lines 214 and 215 might be a reference potential, e.g., ground, 0V or Vss. The word

lines 202 and the select lines 214 and 215 might represent all word lines and select lines between a bit line 204 and the source 216. An initial voltage level of the source 216 is transitioned lower at time t0. For example, the initial voltage level of the source 216 might be the reference potential, e.g., ground, 0V or Vss. The voltage level 570 might be some negative voltage level. Higher magnitudes of a negative voltage level 570 may provide more movement of the mobile ions away from the body of the memory cells, but also come with increased power requirements. Although choice of the magnitude of a negative voltage level 570 may be a compromise between power usage and level of mitigation of threshold voltage effects of the mobile ions, a voltage level 570 of -2V to -3V may result in sufficient mobility of the ions for adequate mitigation within structures of the type described herein.

[0054] In response to the transition of the voltage level of the source 216 at time t0, the voltage level of the pillar 340 might be reduced from an initial voltage level (e.g., the reference potential) by a voltage difference 572 due to capacitive coupling. The voltage difference 572 might be some negative voltage level. The voltage difference 572 might further have a lesser magnitude than the voltage level 570, e.g., due to the p-n junction of a conductive portion 342 between a pillar 340 and the source 216. For polysilicon structures, this difference might be 0.7V, such that if the voltage level 570 is -2V to -3V, the voltage level 572 might be -1.2V to -2.3V. The method depicted in Figure 5A might be performed prior to sensing a memory cell selectively connected to the source 216, e.g., immediately prior to sensing that memory cell, or on a periodic basis. For some embodiments, sensing of a memory cell selectively connected to the source 216 is initiated while the voltage level of the pillar 340 is negative. While the example of Figure 5A applied the same voltage level to the word lines 202 and the select lines 214 and 215, differing voltage levels might be used provided a negative voltage difference 572 is maintained on the pillar 340 following transition of the voltage level of the source 216 at time t1, such as by removing the voltage level 570.

[0055] In Figure 5B, the source 216 and bit line 204 might maintain an initial voltage level. For example, the initial voltage level of the source 216 and bit line 204 might be a reference potential, e.g., ground, 0V or Vss. An initial voltage level of the word lines 202 and the select lines 214 and 215 is transitioned higher at time t0. For example, the initial voltage level of the word lines 202 and the select lines 214 and 215 might be the reference potential, e.g., ground, 0V or Vss. The voltage difference 574 might be some positive voltage level.