

WAFER PROCESSING METHOD

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a wafer processing method of processing a wafer to form a 5S molded package.

Description of the Related Art

As a structure for realizing miniaturization and higher density of various devices such as large-scale integrated circuits (LSIs) and NAND type flash memories, for example, a chip size package (CSP) in which device chips are packaged in chip size has been put to practical use and widely used for mobile phones, smart phones, and the like. Furthermore, in recent years, of the CSP, a CSP in which not only a front surface but also all side surfaces of a chip are sealed with a sealing material, that is, a so-called 5S molded package has been developed and put to practical use.

The conventional 5S molded package is manufactured by the following steps.

(1) Forming devices (circuits) and external connection terminals called bumps on a front surface of a semiconductor wafer (hereinafter sometimes referred to simply as a wafer).

(2) Cutting the wafer along division lines from a front surface side of the wafer to form cut grooves each having a depth corresponding to a finished thickness of each of the device chips.

(3) Sealing the front surface of the wafer with a carbon black-containing sealing material.

(4) Grinding a back surface side of the wafer to the finished thickness of each of the device chips to expose the sealing material in the cut grooves.

(5) Performing alignment in which, since the front surface of the wafer is sealed with the carbon black-containing sealing material, the sealing material at a peripheral portion of the front surface of the wafer is removed to expose alignment marks such as target patterns, and the division line to be cut is detected based on the alignment marks.

(6) Cutting the wafer along the division lines from the front surface side of the wafer based on the alignment, and dividing the wafer into 5S molded packages each of which has its front surface and all side surfaces sealed with the sealing material.

Since the front surface of the wafer is sealed with the carbon black-containing sealing material as described above, the devices and the like formed in the front

surface of the wafer are not at all visible to the naked eye. To enable alignment by solving this problem, the present inventor has developed a technique in which, as described in the above paragraph (5), the sealing material at the peripheral portion of the front surface of the wafer is removed to expose the alignment marks such as the target patterns, and based on these alignment marks, the division line to be cut is detected, so that alignment is performed (see Japanese Patent Laid-open No. 2013-074021 and Japanese Patent Laid-open No. 2016-015438).

SUMMARY OF THE INVENTION

However, according to the alignment method described in the above-mentioned patent documents, a step of removing the sealing material at the peripheral portion of the wafer with a large-width cutting blade for edge trimming mounted to a spindle in place of a cutting blade for dicing is needed, and it is laborious to replace the cutting blade and to remove the sealing material at the peripheral portion by edge trimming, thereby causing poor productivity.

It is therefore an object of the present invention to provide a wafer processing method in which an

alignment step can be performed through a carbon black-containing sealing material applied to coat a front surface of a wafer.

In accordance with an aspect of the present invention, there is provided a wafer processing method of processing a wafer in which each of devices having a plurality of bumps is formed in each of regions of a front surface partitioned by a plurality of division lines formed in an intersecting manner. The wafer processing method includes: a first cut groove forming step of forming first cut grooves each having a depth corresponding to a finished thickness of each of device chips by a first cutting blade having a first thickness along the division lines from a front surface side of the wafer; a sealing step of sealing the front surface of the wafer including the first cut grooves with a sealing material, after the first cut groove forming step is performed; a grinding step of grinding the wafer from a back surface side of the wafer to the finished thickness of each of the device chips to expose the sealing material in the first cut grooves, after the sealing step is performed; an alignment step of capturing the front surface side of the wafer through the sealing material by infrared imaging means from the front surface side of the

wafer, detecting an alignment mark, and detecting the division line to be cut based on the alignment mark, after the grinding step is performed; and a dividing step of cutting the sealing material in the first cut grooves by a second cutting blade having a second thickness smaller than the first thickness of the first cutting blade along the division lines from the front surface side of the wafer, and dividing the wafer into individual device chips each of which has its front surface and four side surfaces surrounded by the sealing material, after the alignment step is performed. In the sealing step, the front surface of the wafer is sealed with the sealing material having such a transmitting property that infrared rays to be received by the infrared imaging means pass through the sealing material.

Preferably, the infrared imaging means used in the alignment step includes an InGaAs imaging element.

According to the wafer processing method of the present invention, the front surface of the wafer is sealed with the sealing material through which the infrared rays to be received by the infrared imaging means pass, the alignment mark formed in the wafer is detected through the sealing material by the infrared imaging means, and alignment can be performed based on

the alignment mark. Therefore, the alignment step can be easily performed without removing the sealing material at the peripheral portion of the front surface of the wafer as in the related art. Accordingly, it is possible to cut the division lines by the cutting blade from the front surface side of the wafer, and divide the wafer into individual device chips.

The above and other objects, features and advantages of the present invention and the manner of realizing them will become more apparent, and the invention itself will best be understood from a study of the following description and appended claims with reference to the attached drawings showing a preferred embodiment of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective view of a semiconductor wafer;

FIG. 2 is a perspective view depicting a first cut groove forming step;

FIG. 3 is a perspective view depicting a sealing step;

FIG. 4 is a partly sectional side view depicting a grinding step;

FIG. 5 is a sectional view depicting an alignment step;

FIG. 6A is a sectional view depicting a dividing step; and

FIG. 6B is an enlarged sectional view depicting the dividing step.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

An embodiment of the present invention will be described in detail below with reference to the drawings. Referring to FIG. 1, there is depicted a perspective view of a front surface side of a semiconductor wafer (hereinafter sometimes referred to simply as a wafer) 11 suitable for being processed by a processing method of the present invention. In a front surface 11a of the semiconductor wafer 11, a plurality of division lines (streets) 13 are formed in a grid pattern, and a device 15 such as an integrated circuit (IC) or an LSI is formed in each of regions partitioned by the division lines 13 intersecting orthogonally.

Each device 15 has a plurality of electrode bumps (hereinafter sometimes referred to simply as bumps) 17 on its front surface, and the wafer 11 includes, on the front surface thereof, a device region 19 in which a

plurality of devices 15 each having the plurality of bumps 17 are formed and a peripheral marginal region 21 surrounding the device region 19.

In a wafer processing method according to an embodiment of the present invention, first, a first cut groove forming step of forming first cut grooves each having a depth corresponding to a finished thickness of each of device chips by a first cutting blade having a first thickness along the division lines 13 from the front surface side of the wafer 11 is performed as a first step. The first cut groove forming step will be described with reference to FIG. 2.

A cutting unit 10 includes a cutting blade 14 detachably mounted to a tip portion of a spindle 12, and an alignment unit 16 having imaging means (imaging unit) 18. The imaging unit 18 has not only a microscope and a camera which capture in visible light but also an infrared imaging element which captures an infrared image. In the present embodiment, an InGaAs imaging element has been adopted as the infrared imaging element.

Before performing the first cut groove forming step, alignment is performed in which the front surface of the wafer 11 is first captured in visible light by the imaging unit 18, alignment marks such as target patterns

formed in each device 15 are detected, and the division line 13 to be cut is detected based on the alignment marks.

After the alignment is performed, the first cut groove forming step is performed in which the cutting blade (first cutting blade) 14 rotated at high speed in a direction of an arrow R1 is made to cut into the wafer 11 to a depth corresponding to a finished thickness of each of device chips along the division line 13 from the front surface 11a side of the wafer 11, and a chuck table (not depicted) with the wafer 11 sucked and held thereon is fed for processing in a direction of an arrow X1, whereby a first cut groove 23 is formed along the division line 13.

The first cut groove forming step is performed sequentially along the division lines 13 extending in a first direction, while the cutting unit 10 is put into indexing feeding in a direction orthogonal to the direction X1 of feeding for processing by the pitch of the division lines 13. Next, the chuck table (not depicted) is rotated by 90°, and then, the same first cut groove forming step as above is performed sequentially along the division lines 13 extending in a second direction orthogonal to the first direction.

After the first cut groove forming step is performed, a sealing step is performed in which, as depicted in FIG. 3, a sealing material 20 is applied to the front surface 11a of the wafer 11 to seal the front surface 11a of the wafer 11 including the first cut grooves 23 with the sealing material. Since the sealing material 20 has fluidity, when the sealing step is performed, the first cut grooves 23 are filled with the sealing material 20.

As the sealing material 20, a composition containing 10.3% of epoxy resin or epoxy resin plus phenolic resin, 85.3% of silica filler, 0.1% to 0.2% of carbon black, and 4.2% to 4.3% of the other constituents in mass % is adopted. Examples of the other constituents include metal hydroxides, antimony trioxide, silicon dioxide, and the like.

When the front surface 11a of the wafer 11 is covered with the sealing material 20 having such a composition and sealed, the carbon black contained in an extremely small amount in the sealing material 20 makes the sealing material 20 black, and accordingly, it is normally difficult to see the front surface 11a of the wafer 11 through the sealing material 20.

Here, the carbon black is mixed in the sealing

material 20 mainly for preventing electrostatic breakdown of the device 15, and at present, no sealing material that does not contain carbon black is commercialized. The method of applying the sealing material 20 is not particularly limited; however, it is desirable to apply the sealing material 20 to a height of each of the bumps 17, and then, the sealing material 20 is subjected to etching to expose head portions of the bumps 17.

After the sealing step is performed, a grinding step is performed in which the wafer 11 is ground from a back surface 11b side of the wafer 11 to a finished thickness of each of the device chips to expose the sealing material 20 in the first cut grooves 23. This grinding step will be described with reference to FIG. 4. A surface protective tape 22 is adhered to the front surface 11a of the wafer 11, and the wafer 11 is sucked and held by a chuck table 24 of a grinding apparatus through the surface protective tape 22.

A grinding unit 26 includes a spindle 30 rotatably accommodated in a spindle housing 28 and rotationally driven by a motor which is not depicted, a wheel mount 32 fixed to a tip of the spindle 30, and a grinding wheel 34 detachably mounted to the wheel mount 32. The grinding wheel 34 is composed of an annular wheel base 36, and a

plurality of grindstones 38 secured to an outer periphery of a lower end of the wheel base 36.

In the grinding step, while the chuck table 24 is rotated in a direction of an arrow a at, for example, 300 rpm, the grinding wheel 34 is rotated in a direction of an arrow b at, for example, 6,000 rpm, and a grinding unit feeding mechanism (not depicted) is driven to bring the grindstones 38 of the grinding wheel 34 into contact with the back surface 11b of the wafer 11.

Then, the back surface 11b of the wafer 11 is ground while the grinding wheel 34 is put into grinding feeding by a predetermined amount downward at a predetermined grinding feeding speed. While a thickness of the wafer 11 is measured by a thickness measuring gauge of a contact type or non-contact type, the wafer 11 is ground to a predetermined thickness, for example, 100 μm , thereby exposing the sealing material 20 filled in the first cut grooves 23.

After the grinding step is performed, an alignment step is performed in which the front surface 11a of the wafer 11 is captured through the sealing material 20 by infrared imaging means from the front surface 11a side of the wafer 11, at least two alignment marks such as target patterns formed in the front surface 11a of the wafer 11

are detected, and the division line 13 to be cut is detected based on these alignment marks.

The alignment step will be described in detail with reference to FIG. 5. Before performing the alignment step, the back surface 11b side of the wafer 11 is adhered to a dicing tape T whose outer peripheral portion is attached to an annular frame F. In the alignment step, as depicted in FIG. 5, the wafer 11 is sucked and held by a chuck table 40 of a cutting apparatus through the dicing tape T, and the sealing material 20 sealing the front surface 11a of the wafer 11 is exposed upward. Then, the annular frame F is fixed by clamping it with clamps 42.

In the alignment step, the front surface 11a of the wafer 11 is captured by the infrared imaging element of the imaging unit 18. Since the sealing material 20 is composed of a sealing material through which the infrared rays to be received by the infrared imaging element of the imaging unit 18 pass, at least two alignment marks such as target patterns formed in the front surface 11a of the wafer 11 can be detected by the infrared imaging element. Preferably, an InGaAs imaging element having high sensitivity is adopted as the infrared imaging element. Preferably, the imaging unit 18 includes an exposure controller by which exposure time or the like

can be adjusted.

Next, the chuck table 40 is rotated by θ such that a straight line connecting these alignment marks will be parallel to the direction X1 of feeding for processing, and further, the cutting unit 10 depicted in FIG. 2 is moved in the direction orthogonal to the direction X1 of feeding for processing by a distance between the alignment mark and the center of the division line 13, whereby the division line 13 to be cut is detected.

After the alignment step is performed, a dividing step is performed in which, as depicted in FIG. 6A, the wafer 11 with its front surface 11a sealed with the sealing material 20 is cut by a second cutting blade 14A having a width smaller than a width of the first cutting blade 14 along the division lines 13 from the front surface 11a side of the wafer 11 until the second cutting blade 14A reaches the dicing tape T to form second cut grooves 25 depicted in FIG. 6B, whereby the wafer 11 is divided into individual device chips 27 each of which has its front surface 11a and four side surfaces surrounded by the sealing material 20.

This dividing step is performed sequentially along the division lines 13 extending in the first direction, after which the chuck table 40 is rotated by 90° , and the

dividing step is then performed sequentially along the division lines 13 extending in the second direction orthogonal to the first direction, whereby the wafer 11 can be divided into the individual device chips 27 each of which has its front surface 11a and four side surfaces sealed with the sealing material 20, as depicted in FIG. 6B.

Since the width of the cutting blade 14A used in the dividing step is smaller than the width of the cutting blade 14 used in the first cut groove forming step, the side surfaces of each of the device chips 27 are sealed with the sealing material 20 upon the formation of the second cut grooves 25 depicted in FIG. 6B.

The device chip 27 manufactured in this way can be mounted onto a mother board by flip chip bonding in which the device chip 27 is inverted upside down and the bumps 17 are respectively connected to conductive pads of the mother board.

The present invention is not limited to the details of the above described preferred embodiment. The scope of the invention is defined by the appended claims and all changes and modifications as fall within the equivalence of the scope of the claims are therefore to be embraced

by the invention.

WHAT IS CLAIMED IS:

1. A wafer processing method of processing a wafer in which each of devices having a plurality of bumps is formed in each of regions of a front surface partitioned by a plurality of division lines formed in an intersecting manner, the wafer processing method comprising:

a first cut groove forming step of forming first cut grooves each having a depth corresponding to a finished thickness of each of device chips by a first cutting blade having a first thickness along the division lines from a front surface side of the wafer;

a sealing step of sealing the front surface of the wafer including the first cut grooves with a sealing material, after the first cut groove forming step is performed;

a grinding step of grinding the wafer from a back surface side of the wafer to the finished thickness of each of the device chips to expose the sealing material in the first cut grooves, after the sealing step is performed;

an alignment step of capturing the front surface side of the wafer through the sealing material by infrared imaging means from the front surface side of the

wafer, detecting an alignment mark, and detecting the division line to be cut based on the alignment mark, after the grinding step is performed; and

a dividing step of cutting the sealing material in the first cut grooves by a second cutting blade having a second thickness smaller than the first thickness of the first cutting blade along the division lines from the front surface side of the wafer, and dividing the wafer into individual device chips each of which has its front surface and four side surfaces surrounded by the sealing material, after the alignment step is performed,

wherein, in the sealing step, the front surface of the wafer is sealed with the sealing material having such a transmitting property that infrared rays to be received by the infrared imaging means pass through the sealing material.

2. The wafer processing method according to claim 1, wherein the infrared imaging means used in the alignment step includes an InGaAs imaging element.