

**Process For Manufacturing A Piezoelectric Structure For A
Radiofrequency Device, Which Structure Can Be Used To Transfer A
Piezoelectric Layer, And Process For Transferring Such A Piezoelectric
Layer**

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FIELD OF THE INVENTION

The present invention relates to a process for manufacturing a piezoelectric structure for a radiofrequency device and which can be used to transfer a piezoelectric layer, and a process for transferring such a piezoelectric layer.

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PRIOR ART

It is known practice to manufacture a radiofrequency (RF) device, such as a resonator or filter, on a substrate comprising, successively, from its base to its surface, a carrier substrate, generally made of a material such as silicon or sapphire, an intermediate bonding layer and a piezoelectric layer.

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Surface acoustic wave (SAW) filters typically comprise a piezoelectric layer and two electrodes in the form of two interdigitated metal combs deposited on the surface of said piezoelectric layer. Depending on the operation of the SAW filter, the thickness of the piezoelectric layer may be of the order of a few tens of nanometers up to several tens of μm . For the latter, there are parasitic modes of propagation that extend into the thickness of the piezoelectric layer and are liable to be reflected at the interface with the carrier substrate beneath. This phenomenon is called "rattle". To avoid these parasitic modes, it is known practice to make the surface of the piezoelectric layer located at the interface with the intermediate bonding layer rough enough to allow the parasitic waves to be reflected in all directions. Given the contemplated operating wavelength of the resonator, the roughness of the rough surface of the piezoelectric layer is very high, of the order of the same magnitude as the operating wavelength (a few μm).

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The piezoelectric layer is typically obtained by transferring a thick substrate of a piezoelectric material (for example obtained by slicing an ingot) to a carrier substrate. The carrier substrate is for example a silicon substrate.

- 5 The transfer of the piezoelectric layer entails bonding the thick piezoelectric substrate to the carrier substrate, followed by thinning the thick piezoelectric substrate so as to leave only a thin piezoelectric layer on the carrier substrate, of the desired thickness for manufacturing the RF device.
- 10 To obtain good adhesion of the piezoelectric substrate to the carrier substrate, a layer of oxide (for example a silicon oxide SiO_2) is generally deposited on each of the two substrates, and said substrates are bonded by way of said oxide layers.
- 15 On the one hand, since the piezoelectric material and the material of the carrier substrate have very different coefficients of thermal expansion, implementing such an anneal causes the assembly to deform substantially.
- 20 On the other hand, depositing an oxide layer on the thick piezoelectric substrate causes said piezoelectric substrate to bow substantially, which is incompatible with the later steps of the process, which are designed for flat substrates.
- 25 Lastly, as mentioned above, the heterostructure cannot undergo the consolidating anneal because of the differences in coefficients of thermal expansion between the thick piezoelectric substrate and the handle substrate. However, in the absence of the consolidating anneal, the bonding energy of the oxide layers of the two substrates remains very low, such that the mechanical strength of the donor virtual substrate is insufficient.
- 30 Consequently, a break at the bonding interface may occur during the step of thinning the thick piezoelectric substrate.

To ensure good adhesion between the thick piezoelectric substrate and the carrier substrate, in particular when the thick piezoelectric substrate has a high level of roughness, the current process requires a large number of steps such as the deposition of multiple oxide layers followed by chemical mechanical polishing (CMP) of said oxide layers, said oxide layers deposited alternately on both faces of the thick piezoelectric substrate in order to avoid substantial bowing that makes bonding impossible.

DISCLOSURE OF THE INVENTION

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The present invention aims to overcome these limitations of the prior art by proposing a process for manufacturing a piezoelectric structure for a radiofrequency device, which can also be used to transfer a piezoelectric layer, and a process for transferring such a piezoelectric layer.

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The invention relates to a process for manufacturing a piezoelectric structure for a radiofrequency device, said process being characterized in that it comprises providing a substrate of piezoelectric material, providing a carrier substrate, providing a dielectric bonding layer on the substrate of piezoelectric material, a step of joining the substrate of piezoelectric material to the carrier substrate by way of the dielectric bonding layer, a thinning step to form the piezoelectric structure consisting of a layer of piezoelectric material joined to a carrier substrate by way of the dielectric bonding layer.

25 In some embodiments, the dielectric bonding layer comprises a layer of silicon oxide deposited on the substrate of piezoelectric material by plasma-assisted chemical vapor deposition.

In some embodiments, the joining step comprises a molecular bonding between the dielectric bonding layer and the carrier substrate.

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In some embodiments, the substrate of piezoelectric material has a rough surface designed to reflect a radiofrequency wave.

5 In some embodiments, the thickness of the dielectric bonding layer is between 200 nm and 500 nm.

In some embodiments, the carrier substrate further comprises a trapping layer intended to be joined to the dielectric bonding layer.

10 In some embodiments, the trapping layer is polycrystalline silicon.

In some embodiments, the trapping layer is obtained by implanting heavy species such as argon.

15 In some embodiments, the thinning step (2') comprises etching and/or chemical mechanical polishing.

The invention also relates to a process for transferring a piezoelectric layer to a final substrate, comprising providing a piezoelectric structure obtained by
20 implementing the manufacturing process as claimed in any one of the preceding claims, forming a weakened zone in the layer of piezoelectric material so as to delimit the piezoelectric layer to be transferred, providing the final substrate, a step of bonding together the layer of piezoelectric material and the final substrate, a detachment step comprising breaking and
25 separating the piezoelectric structure along the weakened zone.

In some embodiments, the weakened zone is formed by implanting atomic species in the layer of piezoelectric material.

30 In some embodiments, the final substrate and the carrier substrate have identical coefficients of expansion.

DESCRIPTION OF THE FIGURES

Other features and advantages of the invention will be better understood from reading the detailed description that follows, with reference to the appended
5 drawings, in which:

figure 1 shows a manufacturing process according to one embodiment of the invention and a substrate according to this embodiment of the invention;

10 figure 2 shows a transfer process according to one embodiment of the invention.

To improve the readability of the figures, the various layers are not necessarily shown to scale.

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DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

Figure 1 shows a carrier substrate 100, preferably of silicon material, to which is transferred a layer of piezoelectric material 200, preferably of
20 monocrystalline piezoelectric material, even more particularly of lithium tantalate or lithium niobate material. Other materials for the layer of piezoelectric material 200 may be envisaged. The active layer 200 to be transferred may also comprise a ferroelectric material, for example LiTaO_3 , LiNbO_3 , LiAlO_3 , BaTiO_3 , PbZrTiO_3 , KNbO_3 , BaZrO_3 , CaTiO_3 , PbTiO_3 or
25 KTaO_3 .

The donor substrate comprising this active layer may take the form of a circular wafer of standardized size, for example 150 mm or 200 mm in diameter. However, the invention is not in any way limited to these dimensions
30 or to this form. The donor substrate may have been taken from an ingot of ferroelectric materials in such a way that the donor substrate has a

predetermined crystal orientation, or the donor substrate may comprise a layer of ferroelectric material joined to a carrier substrate. The crystal orientation of the active layer of ferroelectric material to be transferred is chosen according to the intended application. Thus, as regards the material LiTaO_3 , it is customary to choose an orientation of between 30° and 60°XY , or between 40° and 50°XY , in particular when wanting to make use of the properties of the thin layer to form a SAW filter. As regards the material LiNbO_3 , it is customary to choose an orientation of about 128°XY . However, the invention is by no means limited to a particular crystal orientation.

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Whatever the crystal orientation of the ferroelectric material of the donor substrate, the process comprises for example introducing hydrogen and/or helium species (ions and/or atoms) into this donor substrate. This introduction may for example correspond to a hydrogen implantation, that is to say a hydrogen ion bombardment of the planar face of the donor substrate. As is known *per se*, the aim of the implanted ions is to form a weakened plane delimiting a first layer of ferroelectric material to be transferred, which layer is located on the face side, and another section forming the rest of the substrate. The nature, the dose of the implanted species and the type of ions implanted, and the implantation energy, are chosen depending on the thickness of the layer that it is desired to transfer and on the physicochemical properties of the donor substrate. In the case of a donor substrate made of LiTaO_3 , it will thus be possible to choose to implant a dose of hydrogen of between 1×10^{16} and 5×10^{17} at/cm² with an energy of between 30 and 300 keV in order to define a first layer of about 10 to 2000 nm.

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The carrier substrate 100 of silicon material may also be replaced by a carrier substrate 100 of sapphire material, polycrystalline aluminum nitride (AlN), glass, or any other material having a coefficient of thermal expansion below or opposite to the coefficient of thermal expansion of the piezoelectric material of the layer of piezoelectric material 200 (in the present invention it is the coefficient of thermal expansion in a plane parallel to the main surface of the

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substrates that is of interest). Thus, the carrier substrate 100 plays the role of a stiffener that limits the expansion of the piezoelectric structure 10 during temperature variations to which it is subjected, this making it possible to decrease the thermal frequency coefficient of the layer of piezoelectric material 200, that is to say the extent to which the frequency of a wave propagating through the layer of piezoelectric material 200 varies with temperature. Silicon is particularly preferred because it allows the addition of functionalities allowing electrical isolation for RF applications resulting from the addition of a surface trapping layer.

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The use of silicon has the advantage of not only opening up the field of application of films of piezoelectric material for 300 mm-type large-scale equipment, but also making it compatible with the microelectronics industry, for which the requirements in terms of acceptance on the production line for exotic material other than silicon, in particular lithium tantalate or lithium niobate, are high. It is thus also possible to envisage integrating components obtained or manufactured in the layer of ferroelectric or even piezoelectric material, such as SAW and/or BAW filters, with components obtained or formed in the silicon substrate, such as transistors, power amplifiers or even network switches, thus reducing the losses in the interconnections between different types of components and making such a system integrating multiple components more compact.

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Figure 1 schematically shows the joining step 1' for joining a substrate of piezoelectric material 20 to the carrier substrate 100, preferably of silicon material. The joining step 1' for joining the substrate of piezoelectric material 20 to the carrier substrate 100, preferably of silicon material, is preferably performed by means of a molecular adhesion step. This molecular adhesion step comprises a bonding step, preferably at room temperature, and may be followed by a consolidation anneal of the bonding interface.

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The formation of a dielectric bonding layer 1001 on the face of the substrate of piezoelectric material 20 intended to be joined to the carrier substrate 100 is also shown schematically. In a non-limiting manner, it is possible to envisage a deposition of such a dielectric bonding layer 1001 on a single face of the substrate of piezoelectric material 20. This deposition could thus be carried out at a temperature less than or equal to 300°C. In general, the deposition temperature of the dielectric bonding layer 1001 is chosen such that the bow caused by the difference in coefficient of thermal expansion between the substrate of piezoelectric material 20 and the dielectric bonding layer 1001 remains compatible with a molecular bonding step, the assembly composed of the substrate of piezoelectric material 20 and the dielectric bonding layer 1001 having bowing less than or equal to 100 µm. The thickness of the dielectric bonding layer 1001 should be considered. Over the envisaged thickness range varying between 200 nm and 500 nm, a deposition temperature less than or equal to 300°C shows good results. It was found that not only does the bowing (80 to 90 µm for a thickness of 500 nm of the dielectric bonding layer 1001) remain below the threshold value compatible with a molecular bonding (about 100 µm), but also the nature of the dielectric bonding layer 1001 is such that the bonding energy obtained between the dielectric bonding layer 1001 and the carrier substrate 100 is improved. Another embodiment may provide for dielectric bonding layers to be deposited on the two faces of the substrate of piezoelectric material, either simultaneously or successively, so that the bowing of the assembly composed of the two dielectric bonding layers and the substrate of piezoelectric material 20 remains compatible with a molecular bonding as mentioned above. It has been found, surprisingly, that the bonding energies have higher values when molecular bonding takes place directly between the dielectric bonding layer 1001 and the carrier substrate 100 without the presence of a dielectric bonding layer that is present on this carrier substrate 100 as is known from the prior art. The bonding energies may thus reach high values greater than 1J/m². These energies are high enough to allow a stable mechanical strength during subsequent steps such as the thinning step or a consolidation anneal step.

The molecular adhesion step is preferably carried out at room temperature, i.e. approximately 20°C. It is, however, possible to carry out this direct hot bonding at a temperature of between 20°C and 50°C. In addition, the bonding
5 step is advantageously carried out at low pressure, that is to say at a pressure less than or equal to 5 mTorr (1 Torr is exactly 101325/760 pascals, i.e. approximately 133.322 Pa), which allows desorption of the water from the surfaces forming the bonding interface. Carrying out the bonding step under vacuum allows the desorption of water at the bonding interface to be improved
10 further still.

In an advantageous embodiment, the substrate of piezoelectric material 20 has a rough surface designed to reflect a radiofrequency wave. In the present text, "rough surface" means a surface whose roughness is of the same order
15 of magnitude as the wavelength of the RF waves intended to propagate in the piezoelectric layer of the resonator or filter, so as to allow the reflection of parasitic waves in all directions so that they no longer contribute to the output signal of the resonator or filter in question. In the context of the present invention, the roughness of such a surface is between 1.0 and 1.8 µm
20 measured peak-to-valley. To fill this roughness, the dielectric bonding layer 1001 has a thickness greater than the roughness; flatness is obtained by means of a chemical and/or mechanical etching step.

Preferably, the dielectric bonding layer 1001 comprises a layer of silicon oxide
25 deposited on the substrate of piezoelectric material 20, preferably by plasma-assisted chemical vapor deposition.

According to another embodiment, the dielectric bonding layer 1001 is a layer of silicon oxide, or a layer of silicon nitride, or a layer comprising a combination
30 of silicon nitride and oxide, or a superposition of at least one layer of silicon oxide and one layer of silicon nitride, preferably obtained by plasma-assisted chemical vapor deposition.

In an advantageous embodiment, a bonding interface consolidation anneal is carried out in order to reinforce the mechanical strength of the piezoelectric structure. The consolidation anneal is normally performed at temperatures less than or equal to 300°C, for a period varying from a few minutes to a few hours. In the case where the dielectric bonding layer 1001 is formed by deposition at a low temperature, this anneal is carried out at a temperature below the deposition temperature of said dielectric bonding layer 1001, and thus makes it possible to increase the bonding energy without, however, producing a defect at the bonding interface due to the presence of any impurities (such as hydrogen) and their degassing and migration towards this interface during such an anneal.

As shown schematically in figure 1, there follows a thinning step 2' for thinning the substrate of piezoelectric material 20 after it has been joined to the carrier substrate 100. Figure 1 schematically shows the thinning step 2', which may be implemented for example by means of chemical and/or mechanical etching (polishing, grinding, milling, etc.). In this way, the layer of piezoelectric material 200 can be obtained. The thinning step may also consist of applying the SmartCut™ method. This method is shown schematically in figure 2 and involves forming a weakened zone in the layer to be transferred so as to delimit the layer to be transferred from the remaining layer of the substrate chosen for transfer, providing a receiving substrate to which the layer to be transferred is transferred, a step of joining the layer to be transferred to the receiving substrate, generally by means of molecular bonding, then a detachment step that comprises breaking and separating along the weakened zone, thus forming a heterostructure comprising the layer to be transferred to the receiving substrate. The thinning step is generally performed at a temperature below 300°C, more particularly at room temperature. In the case where the dielectric bonding layer 1001 is formed by deposition at a low temperature, the thinning step is generally performed at a temperature below the deposition temperature of said dielectric bonding layer 1001, which makes

it possible to avoid the presence of aforementioned defects at the bonding interface due to the presence of any impurities (such as hydrogen) and their degassing and migration towards this interface during such a thinning step.

- 5 Figure 2 schematically shows an embodiment of a process for transferring a piezoelectric layer 200' to a final substrate 300', comprising providing a piezoelectric structure 10' (obtained using the process shown schematically in figure 1 in the knowledge that the invention is not limited to this embodiment), forming a weakened zone 0'' in the layer of piezoelectric material 200 so as to
- 10 delimit the piezoelectric layer 200' to be transferred from the remaining layer 201 of the layer of piezoelectric material 200, providing the final substrate 300', a step of joining the layer of piezoelectric material 200 to the final substrate 300', a detachment step 2'' that comprises breaking and separating the piezoelectric structure 10' along the weakened zone, thus forming the
- 15 heterostructure 30' comprising the piezoelectric layer 200' on the final substrate 300'. The detachment step is preferably performed at a temperature less than 300°C or, in the case where the dielectric bonding layer 1001 is formed by deposition at a low temperature, less than or equal to the deposition temperature of the dielectric bonding layer 1001, preferably at a temperature
- 20 less than or equal to 300°C.

The joining step 1'' for joining the piezoelectric structure 10' to the final substrate 300', preferably of silicon material, is preferably performed by means of a molecular adhesion step. This molecular adhesion step comprises a

25 bonding step, preferably at room temperature, and may be followed by a consolidation anneal of the bonding interface.

For the transfer process shown schematically in figure 2, the weakened zone 0'' is formed by implanting atomic species in the layer of piezoelectric material 200. In general, the implantation step 0'' is performed using hydrogen ions.

30 One interesting alternative well known to those skilled in the art involves replacing all or some of the hydrogen ions with helium ions.

For a layer of piezoelectric material 200 of lithium tantalate, a hydrogen implantation dose will typically be between $6 \times 10^{16} \text{ cm}^{-2}$ and $1 \times 10^{17} \text{ cm}^{-2}$. The implantation energy will typically be between 50 and 170 keV. Thus, the
5 detaching is typically performed at temperatures of between 150°C and 300°C. Thicknesses of the piezoelectric layer 200' of the order of 10 nm to 500 nm are thus obtained.

The final substrate 300' and the carrier substrate 100 may advantageously
10 have an identical, or at least very close, coefficient of thermal expansion, which allows better mechanical strength and less deformation during bonding interface consolidation annealing. The two substrates may be of identical nature, substantially made of silicon apart from the dielectric bonding layers or a trapping layer that is possibly present. The latter do not have a sufficient
15 thickness to significantly influence the benefit of the "sandwich" structure having a final substrate 300' and a carrier substrate 100 of the same material.

Just after the detachment operation, additional technological steps are advantageously added with the aim of either strengthening the bonding
20 interface, or restoring a good level of roughness, or correcting any defects generated during the implantation step (or else to prepare the surface for the resumption of other process steps such as the formation of electrodes for the SAW-type device, for example). These steps are for example polishing, chemical etching (wet or dry), annealing, chemical cleaning. They may be
25 used alone or in combination, which those skilled in the art will be capable of adjusting.

In advantageous embodiments, the carrier substrate 100 and/or the final substrate 300' may be a silicon substrate having an electrical resistivity greater
30 than 1 k.ohm.cm. This carrier substrate 100 and/or final substrate 300' may also include a charge trapping layer placed on the surface of this silicon substrate intended to be joined. The trapping layer may comprise undoped

polysilicon. Under certain circumstances, and in particular when the trapping layer has a sufficient thickness, for example greater than 30 μm , the silicon base substrate may have a standard resistivity, less than 1 k. $\Omega\cdot\text{cm}$. In general, it is a non-crystalline layer having structural defects such as

5 dislocations, grain boundaries, amorphous zones, interstices, inclusions, pores, etc.. These structural defects form traps for the charges liable to flow through the material, for example at the site of incomplete or dangling chemical bonds. Conduction is thus prevented in the trapping layer, which consequently exhibits high resistivity. Advantageously, and for reasons of

10 simplicity of implementation, this trapping layer is formed by a layer of polysilicon. Its thickness, in particular when it is formed on an electrically resistive silicon base substrate, may be between 0.3 μm and 3 μm . But other thicknesses below or above this range are quite possible, depending on the expected level of RF performance. In order to seek to preserve the

15 polycrystalline quality of this layer during the heat treatments that the carrier substrate 100 or the final substrate 300' may undergo, an amorphous layer can advantageously be provided, made of silicon dioxide, for example, on this substrate before the deposition of the charge trapping layer. Alternatively, the trapping layer can be formed by implanting a heavy species, such as argon,

20 in a surface thickness of the substrate, in order to form therein the structural defects constituting the electrical traps. This layer can also be formed by porosifying a surface thickness of the substrate.

CLAIMS

1. A process for manufacturing a piezoelectric structure (10) for a radiofrequency device, said process being characterized in that it comprises providing a substrate of piezoelectric material (20), providing a carrier substrate (100), providing a dielectric bonding layer (1001) on the substrate of piezoelectric material (20), a step of joining (1') the substrate of piezoelectric material (20) to the carrier substrate (100) by way of the dielectric bonding layer (1001), a thinning step (2') to form the piezoelectric structure (10) consisting of a layer of piezoelectric material (200) joined to a carrier substrate (100) by way of the dielectric bonding layer (1001).
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2. The process as claimed in the preceding claim, wherein the dielectric bonding layer (1001) comprises a layer of silicon oxide deposited on the substrate of piezoelectric material (20) by plasma-assisted chemical vapor deposition.
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3. The process as claimed in either one of the preceding claims, wherein the joining step (1') comprises a molecular bonding between the dielectric bonding layer (1001) and the carrier substrate (100).
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4. The process as claimed in any one of the preceding claims, wherein the substrate of piezoelectric material (20) has a rough surface designed to reflect a radiofrequency wave.
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5. The process as claimed in any one of the preceding claims, wherein the thickness of the dielectric bonding layer (1001) is between 200 nm and 500 nm.
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6. The process as claimed in any one of the preceding claims, wherein the carrier substrate (100) further comprises a trapping layer intended to be joined to the dielectric bonding layer (1001).
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7. The process as claimed in the preceding claim, wherein the trapping layer is polycrystalline silicon.

8. The process as claimed in claim 6, wherein the trapping layer is obtained by implanting heavy species such as argon.
- 5 9. The process as claimed in any one of the preceding claims, wherein the thinning step (2') comprises etching and/or chemical mechanical polishing.
- 10 10. A process for transferring a piezoelectric layer (200') to a final substrate (300'), comprising providing a piezoelectric structure (10) obtained by implementing the manufacturing process as claimed in any one of the preceding claims, forming a weakened zone (0'') in the layer of piezoelectric material (200) so as to delimit the piezoelectric layer (200') to be transferred, providing the final substrate (300'), a step of bonding together (1'') the layer of piezoelectric material (200) and the final substrate (300'), a detachment step (2'') comprising breaking and separating the piezoelectric structure (10) along the weakened zone.
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11. The process as claimed in the preceding claim, wherein the weakened zone is formed by implanting atomic species in the layer of piezoelectric material (200).
- 20 12. The process as claimed in either of claims 10 and 11, wherein the final substrate (300') and the carrier substrate (100) have identical coefficients of expansion.