(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

162162

(43) International Publication Date
3 February 2005 (03.02.2005)

PCT

(10) International Publication Number
WO 2005/010997 A2

(51) International Patent Classification[7]: H01L 29/786, 29/423, 21/336, 29/10

(21) International Application Number:
PCT/US2003/039727

(22) International Filing Date:
12 December 2003 (12.12.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/607,632 27 June 2003 (27.06.2003) US

(71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

(72) Inventors: HARELAND, Scott; 378 Sioux Lookout, Lino Lakes, MN 55014 (US). CHAU, Robert; 8875 SW 171st Avenue, Beaverton, OR 97007 (US). DOYLE, Brian; 11156 NW Montreux Lane, Portland, OR 97229 (US). DATTA, Suman; 3028 NW Chapin Drive, Portland, OR 97229 (US). JIN, Been-Yih; 12872 Sierra Court, Lake Oswego, OR 97035 (US).

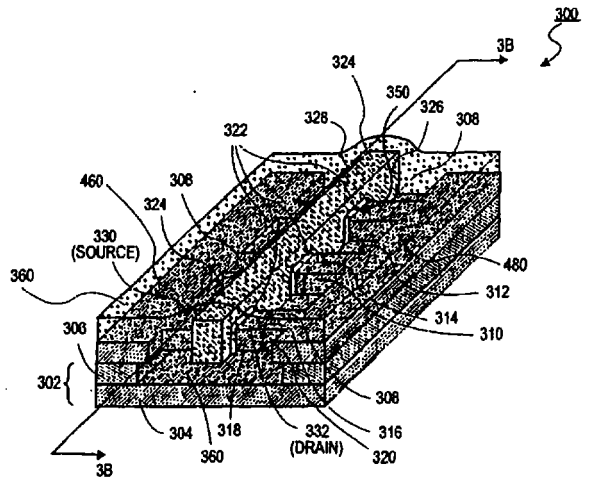
(74) Agents: MALLIE, Michael, J. et al.; Blakely, Sokoloff, Tayor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

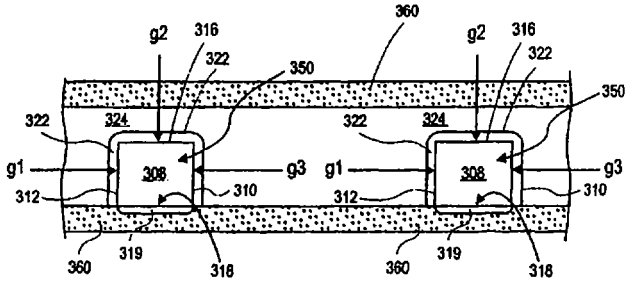
(84) Designated States *(regional)*: ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),

[Continued on next page]

(54) Title: NONPLANAR DEVICE WITH STRESS INCORPORATION LAYER AND METHOD OF FABRICATION



A



B

(57) Abstract: A semiconductor device comprising a semiconductor body having a top surface and laterally opposite sidewalls is formed on an insulating substrate. A gate dielectric layer is formed on the top surface of the semiconductor body and on the laterally opposite sidewalls of the semiconductor body. A gate electrode is formed on the gate dielectric on the top surface of the semiconductor body and is formed adjacent to the gate dielectric on the laterally opposite sidewalls of the semiconductor body. A thin film is then formed adjacent to the semiconductor body wherein the thin film produces a stress in the semiconductor body.

WO 2005/010997 A2

G00002

European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.