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DATA SAMPLING CIRCUIT AND PORTABLE RADIO TERMINAL DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to a data sampling circuit which deals with a radio signal, and to a portable radio terminal device such as a pager which incorporates the data sampling circuit. In particular, the present invention relates to a data sampling circuit for a decoder of a pager which receives a radio signal and detects a user specific number contained therein to initiate a given processing procedure.

A radio paging operation takes place with respect to a small size radio receiver such as a pager carried by a person who is off his or her office or desk to let him or her know the occurrence of a need of communication by a calling tone, a vibration or a displayed message.

A radio paging system in the pager includes POCSAG (Post Office Code Standardization Advisory Group) coding scheme. A code word used in the POCSAG coding scheme has four types including a synchronization (sync) code word, an address code word, a message code word and an idle code word, each consisting of 32 bit data.

In general, a conventional data sampling circuit includes a 32 bit shift register, namely, a shift register having 32 stages, and an output from each stage is connected to a preamble detector and a sync code word detector, respectively. When a thirty second bit data is sampled by the shift register in accordance with a receiving timing of the address code word or the message code word which consists of 32 bit data, the 32 bit data contained in the shift register is transferred in a serial manner to the error correction unit in synchronization with a system clock before the sampling of a next 32 bit data is started.

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However, with the above-mentioned conventional data sampling circuit as used in a digital portable radio terminal device, if the system clock has 32 clocks or less in an interval corresponding to a data length of a single bit of the radio signal, the sampling of a next 32 bit data will begin before the reception of the 32 bit data is completed. With the result that, there is a problem of a misalignment occurring in the data sampling in unit of 32 bits.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a data sampling circuit which enables an accurate data sampling operation in unit of a given number of bits without involving a misalignment in the sampling data, and a portable radio terminal device which incorporates this data sampling circuit.

According to the present invention, a data sampling circuit has a first shift register for sampling bit by bit a radio signal data which is constructed in unit of a given number of bits, thereby holding and shifting a sampling data; a data holding section for holding the sampling data; and a processor for receiving bit by bit the sampling data from the data holding section, thereby processing the sampling data in accordance with a given processing procedure. The data holding section completes a reception of the sampling data corresponding to the radio signal data of the given number of bits from the first shift register at least before a time when a sampling of a first bit data in a next radio signal data which is constructed in unit of a given number of bits subsequent to the radio signal data is initiated by the first shift register.

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BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, and wherein:

Fig. 1 is a block diagram showing a construction of a data sampling circuit and a portable radio terminal device according to one embodiment of the present invention;

Fig. 2 shows a series of timing charts illustrating the operation of the data sampling circuit of Fig. 1; and

Fig. 3 shows a series of timing charts enlarging a portion indicated in Fig. 2 which is delineated between broken lines.

DETAILED DESCRIPTION OF THE INVENTION

A preferred embodiment of the present invention will be described with reference to the accompanying drawings.

Referring to Fig. 1, a data sampling circuit 1 according to the present invention may be incorporated in a digital portable radio terminal device 2 such as a pager.

The data sampling circuit 1 includes a preamble pattern and sync code word detector 10, a 32 bit shift register 11 (hereinafter referred to as "shift register 11") for sampling a radio signal data, a data loadable 32 bit shift register 12 (hereinafter referred to as "data loadable shift register 12") for receiving the data sampled by the shift register 11, thereby holding and shifting the data sampled by the shift register 11, and an error correction unit 13 for receiving and processing

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the data held by the data loadable shift register 12 in accordance with a given processing procedure.

The preamble pattern and sync code word detector 10 detects a preamble (PR) which is used to achieve a bit synchronization between a transmitting system and a receiving system, and a sync code word (UW) which is used to distinguish between physical slots in a data train delivered from a modem, and then delivers the preamble and the sync code word to a controller (not shown).

The shift register 11 has 32 stages and performs a data sampling for a radio signal data A which is constructed in unit of 32 bits in synchronization with a sampling clock signal B.

As mentioned previously, a code word according to the POCSAG coding scheme is of four types including a sync code word, an address code word, a message code word and an idle code word, each consisting of 32 bit data. The shift register 11 samples data of each bit in synchronization with a sampling clock signal B (see Fig. 2), and delivers the sampling data corresponding to each bit to the preamble pattern and sync code word detector 10, and the data loadable shift register 12.

The data loadable shift register 12 is used for a data transfer from the shift register 11 to the error correction unit 13. When the thirty second bit data in the 32 bit radio signal data is sampled by the shift register 11, the data contained in each stage of the shift register 11 is directly loaded into a corresponding stage of the data loadable shift register 12. The data loadable shift register 12 completes a reception of the sampling data corresponding to the 32 bit radio signal data from the shift register 11 at least before a time when a sampling of a first bit data in a next 32 bit radio

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signal data subsequent to the 32 bit radio signal data is initiated by the shift register 11. In this embodiment, the data loadable shift register 12 holds the 32 bit data from the shift register 11 for delivery to the error correction unit 13 at least until the sampling of the next 32 bit radio signal data is started by the shift register 11.

Thus, it will be seen that even when the next sampling of the code word is started by the shift register 11, the data loadable shift register 12 holds a previous set of 32 bit data for the purpose of data transfer to the error correction unit 13.

The above-mentioned error correction unit 13 performs an error check of an output from the data loadable shift register 12 according to CRC (cyclic redundancy check) code, which is capable of detecting not only a random code, but also a burst error, and also enables a correction of an error.

In Fig. 1, various signals appearing at selected parts of the data sampling circuit are shown by characters A to I. A signal designated by A represents a radio signal data which is input to the shift register 11, a signal B represents a sampling clock signal which is used to sample the radio signal data by the shift register 11, a signal C represents a reset signal which resets the both the shift register 11 and the data loadable shift register 12, and signals D and E represent outputs from the individual stages of the 32 bit shift register 11. It will be noted that thirty two outputs are connected to both a data load input of the preamble pattern and sync code word detector 10 and a data load input of the data loadable shift register 12.

A signal F represents a data input to a flipflop which forms the first stage of the data loadable shift

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register 12, which voltage is normally fixed to a ground level or a power supply voltage level. A signal G represents a system clock signal used in the data loadable shift register 12, and a signal H represents a data load enable signal of the data loadable shift register 12. A signal I represents an output from a flipflop which is the final stage of the data loadable shift register 12, and is connected to the error correction unit 13.

As described above, the shift register 11 is devoted for the sampling of the radio signal data A, while the data loadable shift register 12 is devoted for data transfer to the error correction unit 13.

The operation of the data sampling circuit 1 in the portable radio terminal device 2 constructed in the manner mentioned above will now be described.

Fig. 2 is a timing chart illustrating the operation of the data sampling circuit of Fig. 1, and Fig. 3 is an enlarged view of a portion indicated in Fig. 2 which is delineated between broken lines. It is to be understood that a number appearing in the row of signal indicates a bit number of the data.

In synchronization with the sampling clock signal B, the radio signal data A which is constructed in unit of 32 bits is sampled bit by bit into the shift register 11. When the thirty second bit data, i.e., final bit data in the 32 bit radio signal data is sampled by the shift register 11, the data load enable signal H becomes active, as shown in Figs. 2 and 3. The data loadable shift register 12 therefore receives the sampling data which is constructed in unit of 32 bits between a time when a thirty second bit data in the 32 bit radio signal data is sampled by the shift register 11 and a time when a sampling of a first bit in a next 32 bit radio signal

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data subsequent to the 32 bit radio signal data is initiated by the shift register 11.

Subsequently, clocks G are used to transfer 32 bit data (output I) which are now stored in the data loadable shift register 12 to the error correction unit 13.

As described above, the radio signal data A is sampled into the shift register 11 using the sampling clock B. After the thirty second bit data in the radio signal data A is sampled, outputs from the respective stages of the shift register 11 is loaded into the corresponding stages of the data loadable shift register 12. Subsequently, before the shift register 11 begins to sample the next 32 bit radio signal data, the data loadable shift register 12 outputs the sampling data for data transfer held therein to the error correction unit 13.

The data loadable shift register 12 hold the 32 bit data which has been loaded thereinto from the shift register 11, even if the next sampling of code word is initiated in the shift register 11. Accordingly, even if there are 32 clocks or less in an interval corresponding to the data length of a single bit of the radio signal data (A in Fig. 2 or 3), a data sampling in unit of 32 bits can take place in an accurate manner.

Accordingly, when the data sampling circuit which exhibits an excellent feature is incorporated into a portable radio terminal device such as the pager which is destined to receive radio signal in order to detect a user specific number contained therein to initiate a given processing procedure, a reliable operation of the portable radio terminal device can be assured.

As described above, the data sampling circuit of this embodiment can be applied to a radio paging device

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such as the pager, but the application of the data sampling circuit is not limited thereto. The data sampling circuit of this embodiment is equally applicable to any arrangement in which a data sampling is made.

In the above-mentioned embodiment, the data loadable shift register 12 is used for transferring data to the error correction unit 13, but ,instead of the use of the data loadable shift register 12, a RAM, for example, may be used for transferring data to the error correction unit 13.

In the above-mentioned embodiment, an example of the processor is illustrated as the error correction unit 13, but it should be understood that any other processing procedure may be applied to data output from the data loadable shift register 13.

In addition, it should also be understood that the type of registers or the number of bits used to construct the data sampling circuit 1 are not limited to the specific example disclosed in the above-mentioned embodiment.

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WHAT IS CLAIMED IS:

1. A data sampling circuit comprising:

a first shift register (11) for sampling bit by bit a radio signal data which is constructed in unit of a given number of bits, thereby holding and shifting a sampling data;

a data holding section (12) for holding said sampling data; and

a processor (13) for receiving bit by bit said sampling data from said data holding section (12), thereby processing said sampling data in accordance with a given processing procedure;

wherein said data holding section (12) completes a reception of said sampling data corresponding to said radio signal data of said given number of bits from said first shift register at least before a time when a sampling of a first bit data in a next radio signal data which is constructed in unit of a given number of bits subsequent to said radio signal data is initiated by said first shift register (11).

2. A data sampling circuit of Claim 1, wherein said reception by said data holding section (12) is performed between a time when a final bit data in said radio signal data is sampled by said first shift register (11) and a time when said sampling of said first bit data in said next radio signal data is initiated by said first shift register (11).

3. A data sampling circuit of Claim 1, wherein said data holding section (12) holds said sampling data when said sampling of said first bit data in said next radio signal data is initiated by said first shift register

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(11).

4. A data sampling circuit of Claim 1, wherein said data holding section (12) includes a second shift register.

5. A data sampling circuit of Claim 1, wherein said first shift register (11) sampled said radio signal data in synchronization with a sampling clock signal which includes said given number of clocks in an interval corresponding to a length of said radio signal data.

6. A data sampling circuit of Claim 1, wherein said data holding section (12) receives said sampling data in synchronization with a data load enable signal which is generated between the time when said final bit data in said radio signal data is sampled by said first shift register (11) and the time when said sampling of said first bit data in said next radio signal data is initiated by said first shift register (11).

7. A data sampling circuit of Claim 1, wherein processor (13) receives said sampling data from said data holding section (12) in synchronization with a system clock signal which includes said given number of clocks or less in an interval corresponding to a length of a single bit of said radio signal data.

8. A data sampling circuit of Claim 1, wherein said given number of bits is 32 bits.

9. A data sampling circuit of Claim 1, wherein said processor (13) includes an error detecting unit for detecting presence or absence of an error in said

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sampling data transferred thereto.

10. A data sample circuit of Claim 9, wherein said error detecting unit detects an error in said sampling data according to a cyclic redundancy check code contained in said sampling data.

11. A portable radio terminal device which receives a radio signal data and detects a user specific number contained therein to perform a given processing procedure, comprising a data sampling circuit;

said data sampling circuit comprising:

a first shift register (11) for sampling bit by bit a radio signal data which is constructed in unit of a given number of bits, thereby holding and shifting a sampling data;

a data holding section (12) for holding said sampling data; and

a processor (13) for receiving bit by bit said sampling data from said data holding section (12), thereby processing said sampling data in accordance with a given processing procedure;

wherein said data holding section (12) completes a reception of said sampling data corresponding to said radio signal data of said given number of bits from said first shift register at least before a time when a sampling of a first bit data in a next radio signal data which is constructed in unit of a given number of bits subsequent to said radio signal data is initiated by said first shift register (11).

12. A portable radio terminal device of Claim 11, wherein said reception by said data holding section (12) is performed between a time when a final bit data in said

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radio signal data is sampled by said first shift register (11) and a time when said sampling of said first bit data in said next radio signal data is initiated by said first shift register (11).

13. A portable radio terminal device of Claim 11, wherein said data holding section (12) holds said sampling data when said sampling of said first bit data in said next radio signal data is initiated by said first shift register (11).

14. A portable radio terminal device of Claim 11, wherein said data holding section (12) includes a second shift register.

15. A portable radio terminal device of Claim 11, wherein said first shift register (11) sampled said radio signal data in synchronization with a sampling clock signal which includes said given number of clocks in an interval corresponding to a length of said radio signal data.

16. A portable radio terminal device of Claim 11, wherein said data holding section (12) receives said sampling data in synchronization with a data load enable signal which is generated between the time when said final bit data in said radio signal data is sampled by said first shift register (11) and the time when said sampling of said first bit data in said next radio signal data is initiated by said first shift register (11).

17. A portable radio terminal device of Claim 11, wherein processor (13) receives said sampling data from

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said data holding section (12) in synchronization with a system clock signal which includes said given number of clocks or less in an interval corresponding to a length of a single bit of said radio signal data.

18. A portable radio terminal device of Claim 11, wherein said given number of bits is 32 bits.

19. A portable radio terminal device of Claim 11, wherein said processor (13) includes an error detecting unit for detecting presence or absence of an error in said sampling data transferred thereto.

20. A portable radio terminal device of Claim 19, wherein said error detecting unit detects an error in said sampling data according to a cyclic redundancy check code contained in said sampling data.

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