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(71) Applicant *(for all designated States except US)*: **INTERNATIONAL BUSINESS MACHINES CORPORATION** [US/US]; New Orchard Road, Armonk, NY 10504 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **DORIS, Bruce, B.** [US/US]; 350 Lake Shore Drive, Brewster, NY 10509 (US). **CHIDAMBARRAO, Dureseti** [US/US]; 29 Old Mill Road, Weston, CT 06883 (US). **IEONG, Meikei** [PT/US]; 31 Summerlin Court, Wappingers Falls, NY 12590 (US). **MANDELMAN, Jack, A.** [US/US]; 11 Claremont Drive, Flat Rock, NC 28731 (US).

(74) Agent: **ABATE, Joseph, P.**; International Business Machines Corporation, Dept. 18G/Bldg. 300-482, 2070 Route 52, Hopewell Junction, NY 12533 (US).

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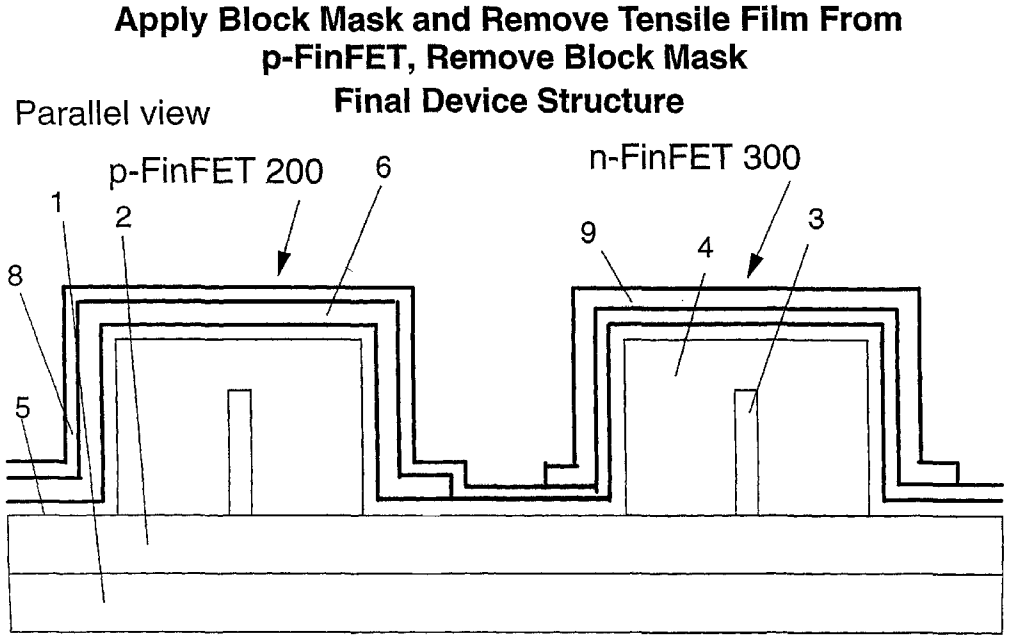
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(54) Title: STRAINED FINFET CMOS DEVICE STRUCTURES




(57) Abstract: A semiconductor device structure, includes a PMOS device (200) and an NMOS device (300) disposed on a substrate (1, 2) the PMOS device including a compressive layer (6) stressing an active region of the PMOS device, the NMOS device including a tensile layer (9) stressing an active region of the NMOS device, wherein the compressive layer includes a first dielectric material, the tensile layer includes a second dielectric material, and the PMOS and NMOS devices are FinFET devices (200, 300).

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*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*